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Design of a Quad-Channel Analog Data Acquisition System Based on FPGA

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Abstract

In order to implement the acquisition and processing of signals from imaging systems, a data acquisition system based on FPGA was designed with the requirements of multi-channel, high-resolution and compactness. The data acquisition (DAQ) system uses a quad-channel 12-bit analog-to-digital converter (ADC) AD9228-65 as the front-end core chip, and a series of signal conditioning circuits to form the front-end system. FPGA is used as the data acquisition, logic control, data readout and processing. After preliminary testing, the DAQ system has the advantages of low power, low cost, high-speed, small size.

Subject Areas

Big Data Search and Mining, Image Processing

Keywords

Multi-Channel, Data Acquisition, FPGA

1. Introduction

In applications of medical diagnosis, industrial nondestructive test and imaging (X/gamma-ray imaging), it often needs to collect raw signals and extract useful information from the array detectors to reconstruct the data distribution. With the development of modern computer science and automation, various data acquisition systems have been developed in different fields [1] [2] [3] [4]. However, the low sampling rate of the above DAQ systems cannot capture the fast signals from the photoelectric devices in imaging applications. The purpose of this study is to design a data acquisition system to satisfy the requirements of multi-channel, great resolution and fast sampling rates typically better than 40 mil-

lion samples per second (MSPS). In this paper, we design a quad-channel analog DAQ system based on the AD9228-65 ADC chip [5] and the spartan-6 FPGA to implement the data acquisition with the 65 MSPS sampling rate and 12-bit resolution.

2. Design of the Overall Scheme

The design of data acquisition system consists of four AD8056, four AD8138, four AD9228-65 and Spartan-6 FPGA. First, four AD8056 were used to adjust the amplitude of the input analog signals, and the AD8138 convert the single end output of AD8056 into differential signals. The differential signals were processed by the differential switched-capacitor circuit of the AD9228-65. By using a 1 V input voltage on the common-mode pin of the AD8138, the input signals were biased and provide a range from 0 to 2 V to the AD9228. The AD9228 outputs serial, low-voltage, differential signaling (LVDS) with a data clock output (DCO) for capturing data and a frame clock output (FCO) for signaling a new data frame. The digital outputs have the same frequency (390 MHz) with the DCO but with a 90˚ phase-shifted, and the double data rate (DDR) operation was supported. After extract the useful information of all the incoming signals, a parallel FIFO (first come, first out) was used to transmit to the GPIO of the MCU. After a ping-pong buffer processing, the final data was upload to the PC end via a USB port. The design of the overall scheme block diagram is shown in **Figure 1**.

3. Hardware Design

The system needs +5 V and −5 V voltage for the operational amplifier power supply, +3.3 V, +1.8 V and +1.2 V voltage for the AD9228 power supply. The +5 V and −5 V voltage are supplied by the external power supply. In order to reduce the system noise, all the power supplies of the ADC were obtained by using the low dropout linear regulator ADP3339 and LT3021ES8 from the +5 V. The circuit schematic diagram of the power supply of the system is shown in **Figure 2**. Meanwhile, all the power supply pins of the ADC and FPGA were applied the ceramic low ESR decoupling capacitors. These capacitors were placed close to the pins and on the same layer of the PCB. The ADP3339 internal uses a noninverting driver to enable the frequency compensation so that a small 1 μF output

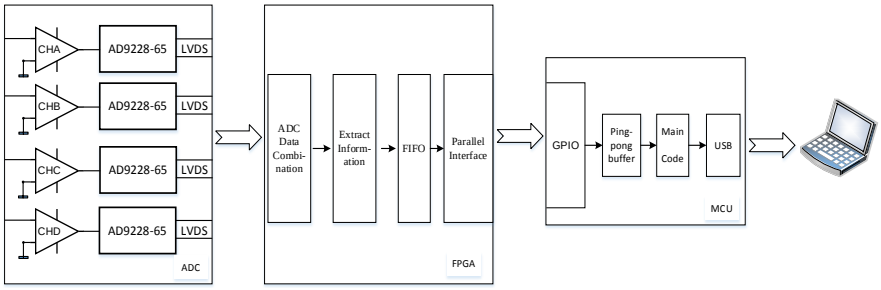

Figure 1. The design of overall scheme block diagram.

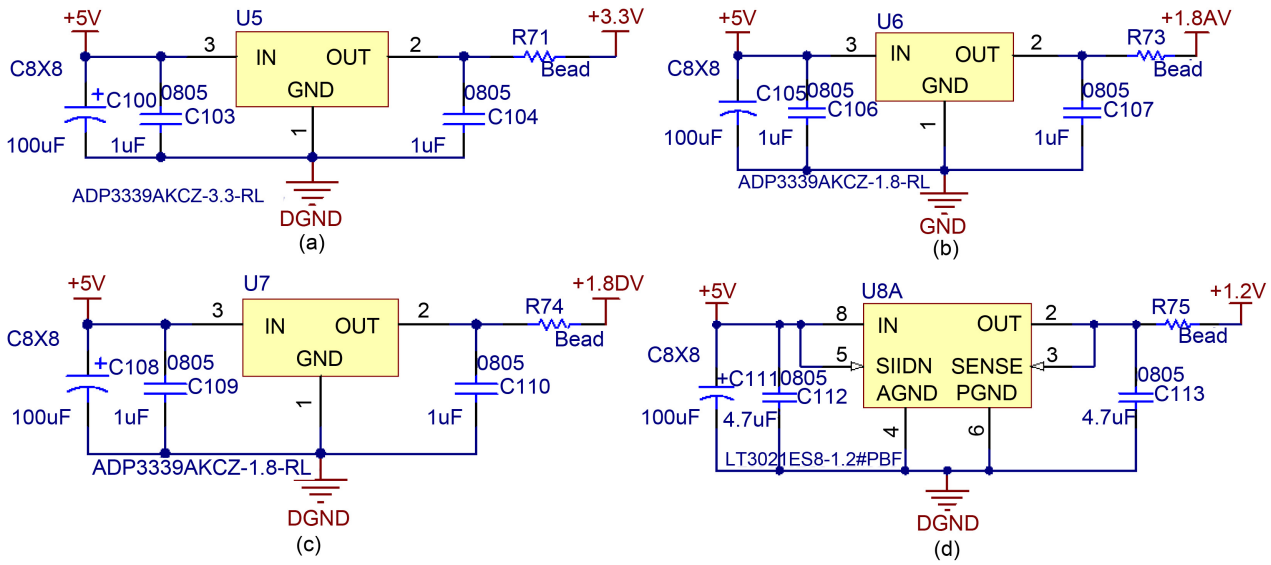

Figure 2. The circuit schematic diagram of the power supply of the system.

capacitor is enough to stable the circuit. A same capacitor combined with a 100 μF electrolytic capacitor was used to reduce the circuit's sensitive to PCB layout. The 4.7 μF capacitors were used to limit peak voltage transients of the LT3021.

The input clock of the ADC was provided by a 65 MHz crystal oscillator. And the differential transformer-coupled configuration was used to achieve a adequate noise performance for the AD9228. The circuit schematic diagram is shown in **Figure 3**.

The bit clock rate for a single ADC in DDR mode can be calculated as follows:

$$\text{Bit clock}\left(\text{MHz}\right)=\frac{\text{Re}\times\text{SR}}{2}\#\tag{1}$$

where the Re and SR are the resolution and the sampling rate of the ADC, respectively.

It means that the bit clock frequency of a 12-bit, 65 MSPS device is 390 MHz, corresponding to a 780 Mb/s bit rate for a single channel and a total of 3.12 Gb/s bit rate for the entire chip. The bit clock provided by the ADC has a 90˚ phase shift relative to the data and frame signals so that it can be positioned in the middle of a valid data eye. The design of the printed circuit board (PCB) must maintain this alignment with great PCB layout techniques so that it ensures the data capture occurs with enough hold windows. The PCB 2D and 3D layout circuit diagram is shown in **Figure 4** and **Figure 5**, respectively. The digital and analog ground were separated to prevent the noises transmission from the digital circuits.

The photographs of the PCB of the DAQ system and the test diagram are shown in **Figure 6** and **Figure 7**, respectively. A 600 kHz sinusoidal signal was produced from a signal generator, and the sampled result captured using the integrated logic analyzer (ILA) core is shown in **Figure 8**. The signal frequency and the sampling rate determine that 108 data points is needed to capture a

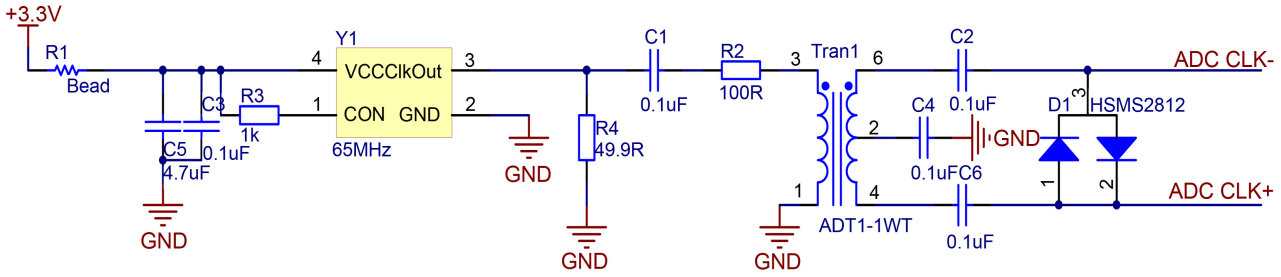

Figure 3. The circuit schematic diagram of the power supply of the system.

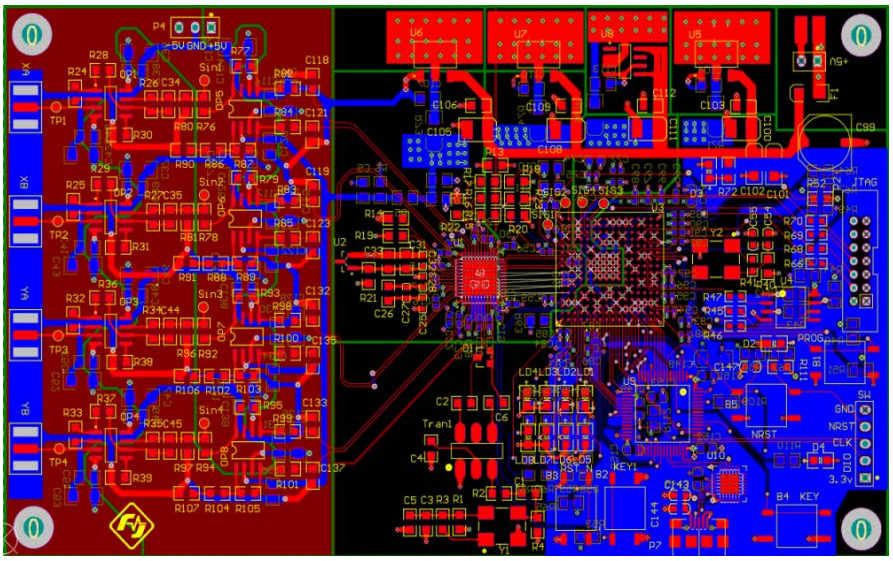

Figure 4. PCB 2D layout circuit diagram.

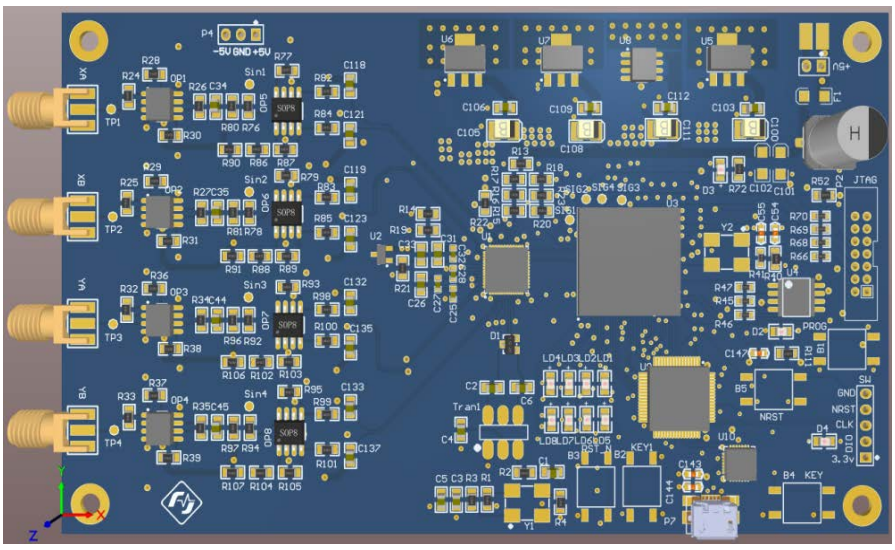

Figure 5. PCB 3D layout circuit diagram.

complete period. A total of 2048 points were sampled and around 19 periods sinusoidal signals were presented in the screen of ILA, which demonstrates that the acquisition result was correct.

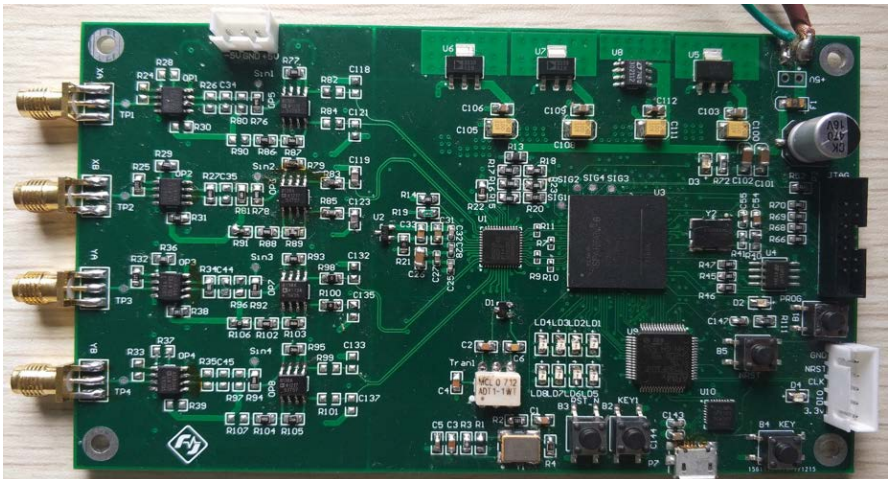

Figure 6. Photograph of the PCB of the DAQ system.

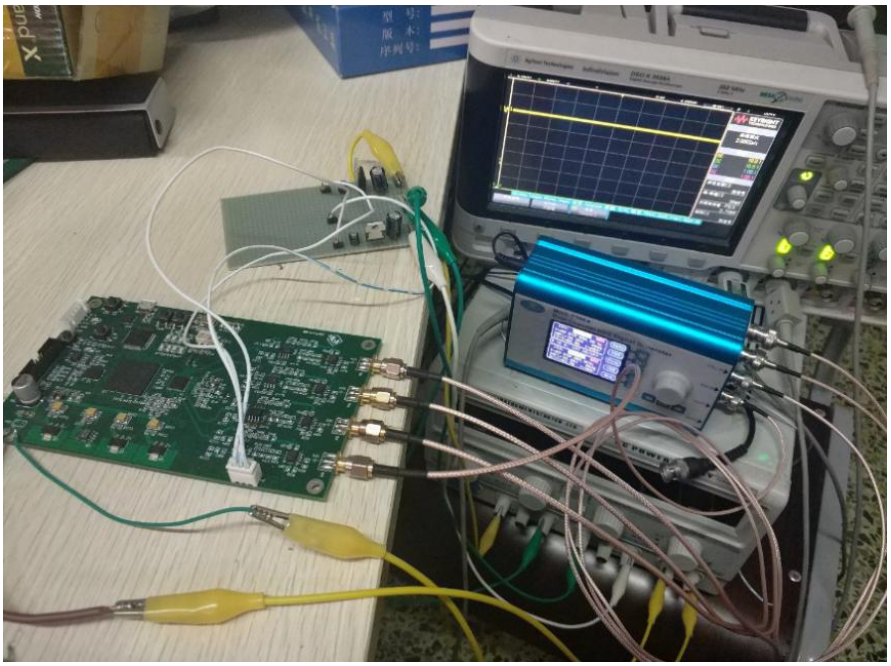

Figure 7. Photograph of the test diagram of the DAQ system.

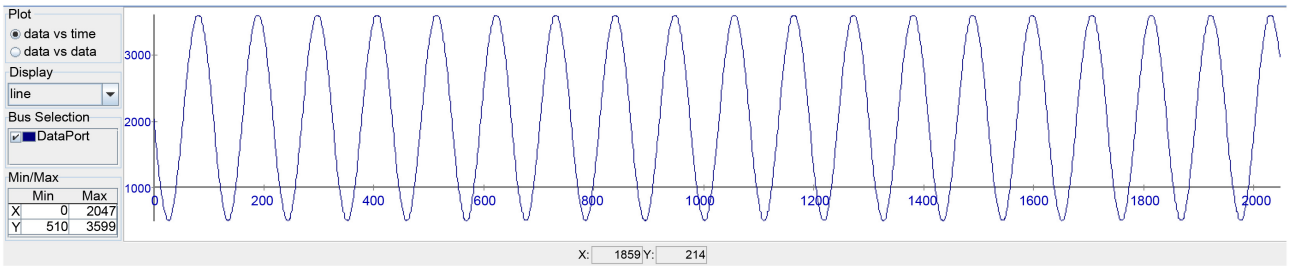

Figure 8. The integrated logic analyzer result of a 600 kHz sinusoidal signal.

4. Conclusion

The quad-channel data acquisition system based on AD9228 was designed to

implement the simultaneous acquisition of 4 input signals. The DAQ system has the advantages of high stability, high resolution, small size and low power consumption, which is suited for some imaging applications. The performance of the DAQ system in different applications need to be further studied.

Acknowledgements

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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[5] AD9228: Quad, 12-Bit, 40/65 MSPS Serial LVDS 1.8 V A/D Converter Data Sheet.