Scientific Research Publishing

Journal of Power and Energy Engineering, 2021, 9, 43-61
https://www.scirp.org/journal/jpee
ISSN Online: 2327-5901
ISSN Print: 2327-588X

Design and Control of an Alternative Buck PWM DC-to-DC Converter

Justin Simmons, Richard Tymerski

Department of Electrical & Computer Engineering, Portland State University, Portland, Oregon, USA
Email: tymerski@ee.pdx.edu

How to cite this paper: Simmons, J. and Tymerski, R. (2021) Design and Control of an Alternative Buck PWM DC-to-DC Converter. *Journal of Power and Energy Engineering*, **9**, 43-61.
https://doi.org/10.4236/jpee.2021.96004

Received: May 19, 2021
Accepted: June 25, 2021
Published: June 28, 2021

Abstract

The second order dc-to-dc buck converter with input LC filter is widely used in industry. An alternative 4th order converter which has advantages in terms of control design leading to better transient performance is presented. A complete DC (steady state average and ripple quantities) and AC small-signal analyses of this converter for both uncoupled and coupled inductor cases is provided. Conditions for achieving, in a lossless manner, a minimum phase control-to-output transfer function are found, which ameliorates regulator design while maximizing loop bandwidth. A closed loop regulator design procedure is presented and the performance of a design example is examined with a prototype. It is believed that this converter is a good alternative in applications where the second order buck converter augmented with an input filter has been traditionally utilized.

Keywords

DC-to-DC Converter, Buck Converter

1. Introduction

The second order (one inductor, one capacitor) PWM buck dc-to-dc switching converter is a widely used power processing circuit topology. This is partly due to its simple topology and good frequency domain control characteristics, in particular the lack of a non-minimum phase (right half plane) zero common to other topologies. This desirable feature permits a wide regulator loop bandwidth resulting in fast transient response to be achieved to both input voltage and load changes. The buck converter features a DC voltage conversion of $V_{out}/V_g = D$ where V_g, V_{out} and D, refer to the input voltage, output voltage and duty ratio, respectively. In this paper, converters that feature this conversion ratio are referred to generically as buck converters.

As the basic buck converter draws a pulsating current from the input, an input LC filter is often used to achieve compliance with regulations regarding electromagnetic interference (EMI). This increases the order of the system to four. This configuration is shown in **Figure 1**. In [1] [2] and [3], a large number of DC-to-DC converter topologies were derived which feature various conversion ratios. Of the fourth order, two switch (one active switch (transistor) and one passive switch (diode)) converters derived a total of seven feature the conversion ratio of a buck converter. The converter of **Figure 1**, *i.e.* the basic buck converter with input filter, is designated as converter D6. The naming convention used in [1] [2] and [3] was one where a converter's name is designated by its position in a matrix of generated converter topologies where a converter family grouping is designated by an alphabetical character and the following number indicates which of the possible six family members is being referred to.

In this paper, a design approach is presented for an alternative converter configuration, *i.e.* one of the other six, which has a number of advantages over the D6 converter. This converter is shown in **Figure 2** and is designated as converter C1 in [1] [2] and [3]. This converter was also presented in [4], but an analysis or design approach was not given. More recent work featuring the C1 converter has appeared in [5], which was used for a maximum power tracking photovoltaic application. In this paper, an extensive set of constraint equations is derived for use in converter design. Discussions of discontinuous conduction modes of operation, both inductor current and capacitor voltage, are presented here for the first time. Coupling of inductors to minimize output voltage ripple is also discussed. Note that C1 and D6 have exactly the same number and type of components but only the configuration is different. This configuration, under certain component constraints, results in the absence of a right half plane zero in the control to output transfer function thus allowing to achieve an improved dynamic performance with a simplified design approach. This situation will be contrasted with that of the D6 converter in Section 2.

In Section 3, an extensive quantitative analysis of the converter is given. This includes DC, ripple and dynamic small signal analyses and discussion on the

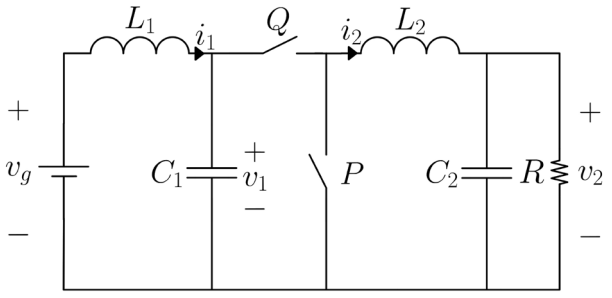

Figure 1. The second order buck converter augmented with an input LC filter. This converter is designated as converter D6 in [1] [2] and [3]. *Q* and *P* are the active (transistor) and passive (diode) switches, respectively.

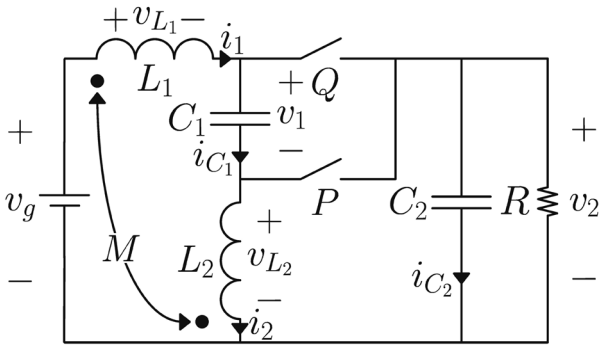

Figure 2. Converter C1 from [1] [2] and [3]. This converter is presented as a viable alternative to converter D6, *i.e.* the second order buck with input LC filter. *Q* and *P* are the active (transistor) and passive (diode) switches, respectively.

avoidance of certain undesirable operating modes, *i.e.* discontinuous conduction mode and discontinuous voltage mode. This results in the attainment of a set of constraint design equation. Section 4 considers the case of coupling the inductors in an effort to reduce output voltage ripple. A design example is given in Section 5 and performance of the constructed prototype is presented. Finally, in Section 6, the Conclusion, an overview of the paper is summarized.

2. Converters C1 and D6 Control Characteristics Compared

The second order (lossless) buck converter is known to not feature any (finite) zeros. However, when an LC filter precedes the power stage a set of complex right half plane zeros appear in the control (duty ratio) to output transfer function. Using the small-signal state space averaging model [6] the duty ratio to output voltage transfer function numerator polynomial is found to be:

$$n(s) = L_1 C_1 s^2 - \frac{D^2 L_1}{R} s + 1 \tag{1}$$

The presence of the right half plane zero severely restricts the bandwidth of the closed loop system thus limiting dynamic performance. In the presence of parasitic resistive losses in L_1 represented by ESR resistance r_{L_1} and under the condition $\frac{D^2 r_{L_1}}{R} \ll 1$ the numerator may be approximated by

$$n(s) = L_1 C_1 s^2 + \left(r_{L_1} C_1 - \frac{D^2 L_1}{R} \right) s + 1 \tag{2}$$

From this it can be seen that zeros can move to the left half plane if $r_{L_1} C_1 - \frac{D^2 L_1}{R} > 0$. Alternatively, input filter design for the buck converter has been approached in the past, see [7] and [8], by finding conditions such that it does not affect the control characteristics of second order buck converter where, as mentioned, no finite zeros are present. This is achieved by incorporation of lossless damping in the input filter, [7] and [8], which increases the number of components needed in the power stage.

In contrast, in a following section it is found that the lossless C1 converter with proper component scaling can feature left half plane zeros and furthermore with the design approach advocated here these zeros can be made to cancel second order poles resulting in an overall second order control to output transfer function.

3. Converter C1 Power Stage Design

3.1. Large-Signal Analysis

In the following a large signal analysis will be performed. This will allow us to determine the average (DC) values of the capacitor voltages and inductor currents. Also, ripple analysis will be performed which will allow us to determine the peak to peak values of the capacitor voltage and inductor current ripples. These analyses use state space models. Operation of the converter will be restricted to the CCM (continuous conduction mode) and CVM (continuous voltage mode). These modes of operation as pertaining to the C1 converter will be discussed subsequently.

Operation in CCM and CVM modes implies that there are two circuit configurations to analyze for the C1 converter. One is where the active switch (e.g. a MOSFET) is ON and the passive switch (e.g. a diode) is OFF, and the other when the reverse switch state occurs. These configurations will be associated with subinterval DT_s and $D'T_s$, respectively, where D is the duty ratio, $D' \triangleq 1-D$ and T_s is the switching period. Initially all parasitics will be ignored and the switches will be considered ideal for simplicity. The state-space model for large signal analysis is given as follows:

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx + Eu \end{aligned} \tag{3}$$

where

$$\begin{aligned} A &= DA_1 + D'A_2 \\ B &= DB_1 + D'B_2 \\ C &= DC_1 + D'C_2 \\ E &= DE_1 + D'E_2 \end{aligned}$$

and the state vector, $x = \left[i_1, i_2, v_1, v_2\right]^{\mathrm{T}}$, input, $u = v_g$ and $y = v_{out}$ $(= v_2$ in the absence of the equivalent series resistance of $C_2)$. The state-space matrices associated with the DT_s subinterval, where switch Q in ON and switch P is OFF, are:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} & \frac{1}{L_2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & -\frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}, \quad B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The state-space matrices associated with the $D'T_s$ subinterval, where switch Q in OFF and switch P is ON, are:

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & -\frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}, \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Using (3) the averaged state space matrices A and B are given by:

$$A = \begin{bmatrix} 0 & 0 & -\frac{D'}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & -\frac{D}{L_2} & \frac{1}{L_2} \\ \frac{D'}{C_1} & \frac{D}{C_1} & 0 & 0 \\ \frac{1}{C_2} & -\frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

With capacitor voltage v_2 as output results in:

$$C_1 = C_2 = C = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}, \quad E_1 = E_2 = E = \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}}$$

Given a constant input $U = V_g$, the DC input voltage, the steady state vector, X, can be determined as follows [7]:

$$X = -A^{-1}BU = \begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{V_g D^2}{R} \\ -\frac{V_g DD'}{R} \\ V_g \\ V_g D \end{bmatrix} \tag{4}$$

The first-order peak-to-peak ripple of the state, Δx, can be evaluated as shown in [9] as:

$$\Delta x = \left(A_1 X + B_1 V_g \right) DT_s = \begin{bmatrix} \Delta i_1 \\ \Delta i_2 \\ \Delta v_1 \\ \Delta v_2 \end{bmatrix} = \begin{bmatrix} \frac{V_g DD'T_s}{L_1} \\ -\frac{V_g DD'T_s}{L_2} \\ -\frac{V_g D^2 D'T_s}{RC_1} \\ 0 \end{bmatrix} \tag{5}$$

Since Δv_2 is zero, it is necessary to calculate the second-order peak-to-peak ripple of the state, $\Delta^2 x$. This is given by [9]:

$$\Delta^2 x = \begin{bmatrix} \Delta^2 i_1 \\ \Delta^2 i_2 \\ \Delta^2 v_1 \\ \Delta^2 v_2 \end{bmatrix} = \frac{A\Delta x T_s}{8} = \begin{bmatrix} \dfrac{V_g (DD')^2 T_s^2}{8RL_1C_1} \\ \dfrac{V_g D^3 D' T_s^2}{8RL_2C_1} \\ \dfrac{V_g DD' T_s^2}{8C_1}\left[\dfrac{D'}{L_1}+\dfrac{D}{L_2}\right] \\ \dfrac{V_g DD' T_s^2}{8C_2}\left[\dfrac{1}{L_1}+\dfrac{1}{L_2}\right] \end{bmatrix} \tag{6}$$

With the exception of v_2, the first-order ripple components are much greater than the second-order components. Therefore, the second-order ripples will be neglected for the inductor currents i_1 and i_2 and capacitor voltage v_1, but not for the output capacitor voltage v_2.

3.2. Small-Signal Analysis

The dynamic performance of the converter will be examined by developing a small signal model. In particular the duty ratio control to output transfer function will be derived. This transfer function is important as it forms part of the loop gain of a closed loop system. Particular attention to the presence of any right half plane (RHP) zeros is paid as these zeros will restrict control loop bandwidth thus compromising transient performance. Fortunately constraints can be formulated such that a RHP zero is avoided. Furthermore, other constraints will be given such as a factorization of the denominator polynomial which simplifies the control design process. Initially for simplicity, all elements will be considered as ideal. The state-space equations for the small-signal model are:

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + B\hat{u} + \left[(A_1 - A_2)X + (B_1 - B_2)U\right]\hat{d} \\ \hat{y} &= C\hat{x} + E\hat{u} + \left[(C_1 - C_2)X + (E_1 - E_2)U\right]\hat{d} \end{aligned} \tag{7}$$

where $\hat{x} = \left[\hat{i}_1, \hat{i}_2, \hat{v}_1, \hat{v}_2\right]^{\mathrm{T}}$, $\hat{u} = \hat{v}_g$ and $\hat{y} = \hat{v}_{out}$,

From (7), the control-to-output transfer function, $G_{vd}(s) \triangleq \hat{v}_{out} / \hat{d}(s)$, can subsequently be determined, with $\hat{u} = 0$:

$$\frac{\hat{v}_{out}}{\hat{d}}(s) = C(sI - A)^{-1}\left[(A_1 - A_2)X + (B_1 - B_2)U\right] + \left[(C_1 - C_2)X + (E_1 - E_2)U\right]$$

This is evaluated to be:

$$\frac{\hat{v}_{out}}{\hat{d}}(s) = V_g \frac{s^2(L_1 + L_2)C_1 + s\dfrac{D(D'L_2 - DL_1)}{R} + 1}{s^4 L_1 L_2 C_1 C_2 + s^3 \dfrac{L_1 L_2 C_1}{R} + s^2\left[(L_1 + L_2)C_1 + (D^2 L_1 + D'^2 L_2)C_2\right] + s\dfrac{D^2 L_1 + D'^2 L_2}{R} + 1} \tag{8}$$

3.3. Design Constraints

A number of design constraints will now be determined. These arise by considering the following: 1) the conditions to keep the converter in CCM and CVM

mode (these are synonymous with the avoidance of discontinuous conduction mode (DCM) or discontinuous voltage mode (DVM) respectively), 2) the maximum inductor current ripples, 3) the maximum output voltage ripple, 4) the avoidance of a RHP zero, and 5) the conditions that make a factorization of the control-to-output transfer function denominator a good approximation. (This factorization is provided as it is convenient in the loop gain design process). To obtain these constraints the results from the large-signal and small-signal analyses will be utilized.

3.3.1. Avoidance of DCM

When switch P is implemented as a diode, the DCM mode may occur. DCM operation arises when the diode current during $D'T_s$ drops to zero. Such a condition would shut off the diode, resulting in a third topology and therefore a third subinterval which would invalidate the small- and large-signal analyses carried out previously. When the diode is ON it carries the sum of the two inductor currents which is given by $i_1 - i_2$. Note that current i_2 is summed negatively as a consequence of the current direction shown in **Figure 2**. To avoid entering DCM, the average-to-peak ripple of the summed currents must be lesser in magnitude than their summed DC values.

$$I_1 - I_2 \geq \left| \frac{\Delta i_1 - \Delta i_2}{2} \right|$$

Using results obtained from (4) and (5) leads to the constraint:

$$L_1 \parallel L_2 \geq \frac{RD'T_s}{2} \tag{9}$$

3.3.2. Avoidance of DVM

DVM arises when the voltage across C_1 drops below zero during DT_s turning the diode ON. Having zero voltage across C_1 results in a third topology, characteristic of the DVM mode. DVM is avoided when the average-to-peak voltage ripple of capacitor C_1, *i.e.* $\frac{\Delta v_1}{2}$, is less than the average capacitor voltage, V_1. That is

$$V_1 \geq \left| \frac{\Delta v_1}{2} \right|$$

Substituting results from (4) and (5) and rearranging gives the constraint:

$$C_1 \geq \frac{D^2 D'T_s}{2R} \tag{10}$$

3.3.3. Acceptable Inductor Current Ripple

Limiting the peak to peak inductor current ripples to 20% of their steady state values results in:

$$\left|\Delta i_1\right| \leq 20\% \left|I_1\right|$$

and:

$$\left|\Delta i_2\right| \le 20\%\left|I_2\right|$$

Substituting from (4) and (5) and rearranging leads to the following constraints on the inductors:

$$L_1 \ge \frac{RD'T_s}{0.2D} \tag{11}$$

$$L_2 \ge \frac{RT_s}{0.2} \tag{12}$$

3.3.4. Acceptable Output Voltage Ripple

For voltage regulators it is desirable to have minimal output voltage ripple. In the absence of ESRs the output voltage v_{out} is equal to the v_2, the voltage across C_2. Limiting the output voltage ripple to 5% of the DC value gives:

$$\left|\Delta^2 v_2\right| \le 5\%\left|V_2\right|$$

Substituting from (4) and (6) and rearranging gives the constraint:

$$\left(L_1 \| L_2\right)C_2 > \frac{D'T_s^2}{4} \tag{13}$$

3.3.5. Avoidance of the Right Half Plane Zero

From the numerator of the control-to-output transfer function it can be seen that a RHP zero will exist if the coefficient of s is negative. Thus avoiding the RHP zero requires that:

$$D'L_2 > DL_1 \tag{14}$$

3.3.6. Symbolic Denominator Factorization

The Bode plot of the control-to-output transfer function will be utilized in a later section to design the feedback loop frequency loop compensation of the C1 converter. Factoring the fourth order polynomial in the denominator of the transfer function into two second order polynomials will make the design of the feedback loop frequency loop compensation conceptually easier as pole-zero cancellation is readily seen. The factorization (given later in Section 5) can be shown to be accurate when the following component constraints apply:

$$C_1 \gg D'^2 C_2 \tag{15}$$

$$C_2 \gg \frac{D'^2 L_2}{R^2} \tag{16}$$

$$L_1 \ll D'^2 L_2 \tag{17}$$

Note however, there is not a strict requirement to size components to achieve accurate factorization.

4. Inductor Coupling

Coupling the inductors L_1 and L_2 has the potential of reducing the output voltage ripple $\Delta^2 v_2$. Analysis is provided in the **Appendix** which shows that the optimum value of M, M_{opt}, is given by:

$$M_{opt} = L_1 \tag{18}$$

Using the optimum M_{opt} reduces $\Delta^2 v_2$ by a factor of:

$$\frac{\Delta^2 v_2}{\Delta^2 v_{2M}} = \frac{L_1 + L_2}{L_2} \tag{19}$$

from the uncoupled case. Therefore, coupling the inductors has the potential to reduce the output voltage ripple by as much as 50% for $L_1 \approx L_2$ or by a negligible percentage if the ratio of inductor values, (defined by parameter α in the Appendix), is large.

5. Design Example

A voltage regulator design example utilizing the C1 converter is presented in this section. The block diagram of this system is shown in Figure 3. The values of the parameters used in this design are listed in Table 1. In the constructed prototype a TL5001 PWM controller IC is used. This device internally provides a triangular waveform with peak-to-peak amplitude of approximately 600 mV which is used as input to the internal PWM comparator. Also provided in this IC is a 1 V reference voltage.

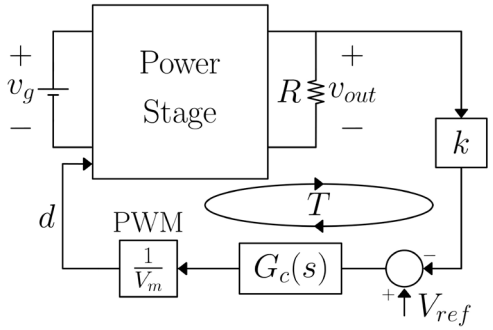

Figure 3. Block diagram of the voltage regulator system with a feedback loop $T(s)$ consisting of the C1 converter power stage characterized by its control to output transfer function $G_{vd} = \hat{v}_{out}/\hat{d}$, resistive divider gain k, compensator transfer function $G_c(s)$, and PWM gain $F_M = 1/V_M$.

Table 1. Parameter values used in the prototype design.

Nominal input voltage, V_g	10 V
Output voltage, V_{out}	5 V
Load resistance, R	5 Ω
PWM ramp amplitude, V_M	0.6 V
Switching frequency, f_s	100 kHz
Voltage reference, V_{ref}	1 V
Feedback gain, k	$\frac{1}{5}$

5.1. Power Stage Component Values

Taking into account the previously derived constraints and considering reasonable component ranges, the values shown in (20) were chosen:

$$\begin{aligned} L_1 &= 330\ \mu\text{H} \\ L_2 &= 680\ \mu\text{H} \\ C_1 &= 10\ \mu\text{F} \\ C_2 &= 10\ \mu\text{F} \end{aligned} \tag{20}$$

Note that for the values chosen, constraints (16) and (17) are not satisfied indicating that the factorization is approximate. However, as previously mentioned, an accurate factorization is not strictly required to achieve an effective design, as will be demonstrated below.

5.2. Frequency Compensation

Frequency compensation is employed to enhance transient performance and provide adequate stability margins. A compensator will be designed by employing asymptotic gain plots. To account for the effects of equivalent series resistance (ESR) of the power stage components on the frequency response, these will need to be introduced into our model given by (8). However, first a factored form of the denominator will be introduced. Equation (21) is a more convenient and factorized form of (8):

$$G_{vd}(s) = \frac{V_g\left[s^2(L_1+L_2)C_1 + s\dfrac{D(D'L_2 - DL_1)}{R} + 1\right]}{\left[(L_1+L_2)C_1 s^2 + \dfrac{D'^2 L_2}{R}s + 1\right]\left[(L_1 \parallel L_2)C_2 s^2 + \dfrac{L_1}{R}s + 1\right]} \tag{21}$$

Note that with this factorization, the pole and zero cancellation, which effectively reduces the transfer function to second order, can easily be seen.

To add in the ESRs, the transformations (5.2) are applied to (21).

$$sL_i \Rightarrow sL_i + r_{Li}, \quad i = 1,2 \tag{22}$$

$$sC_i \Rightarrow \frac{sC_i}{1 + sr_{ci}C_i}, \quad i = 1,2 \tag{23}$$

The resulting terms may be simplified by using the following approximations:

$$r_{Li} \ll R, \quad i = 1,2 \tag{24}$$

$$r_{Ci} \ll R, \quad i = 1,2 \tag{25}$$

This results in the transfer function:

$$G_{vd}(s) \approx \frac{V_g(1 + sr_{C2}C_2)\left[s^2 L_2 C_1 + s\left((r_{L1} + r_{L2})C_1 + \dfrac{D(D'L_2 - DL_1)}{R} + r_{C1}C_1\right) + 1\right]}{\left[s^2 L_2 C_1 + s\left(\dfrac{D'^2 L_2}{R} + (r_{L1} + r_{C1})C_1 + r_{L2}C_2\right) + 1\right]\left[s^2 L_1 C_2 + s\left(\dfrac{L_1}{R} + (r_{L1} + r_{C2})C_2\right) + 1\right]} \tag{26}$$

From (26) it can be seen that the only break frequency introduced by adding

parasitics is a zero due to the ESR of C_2, which occurs at the frequency ω_{ESR} where:

$$\omega_{ESR} = \frac{1}{r_{C2} C_2} \tag{27}$$

The uncancelled second order complex double pole is denoted as ω_P where:

$$\omega_P = \frac{1}{\sqrt{L_1 C_2}} \tag{28}$$

Loop frequency compensation is provided using an "integrator plus lead-lag" compensator. The schematic for which is shown in **Figure 4**.

The transfer function $G_c(s)$ of this compensator is given by:

$$G_c(s) = -\frac{\omega_0}{s} \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{29}$$

where

$$\begin{aligned}
\omega_0 &= \frac{1}{R_{1c}\left(C_{2c}+C_{3c}\right)} \\
\omega_{z1} &= \frac{1}{R_{2c} C_{2c}} \\
\omega_{z2} &= \frac{1}{C_{1c}\left(R_{1c}+R_{3c}\right)} \\
\omega_{p1} &= \frac{1}{R_{3c} C_{1c}} \\
\omega_{p2} &= \frac{1}{R_{2c}\frac{C_{2c} C_{3c}}{C_{2c}+C_{3c}}}
\end{aligned} \tag{30}$$

Generally one can separately place the two compensator zeros: one somewhat before ω_P and the other at ω_P, as is shown in **Figure 5**. These zeros serve to correct the phase shift from the integrator and ω_P, trading a reduced response time for an increase in the loop phase margin. However, for this design both zeros are placed at ω_P as a good phase margin is still achieved. The two compensator poles are then placed, one at ω_{ESR} to cancel it out and the other before the switching frequency to improve high frequency roll off. The chosen compensator pole and zero frequencies, in Hertz, are:

$$\begin{aligned}
f_{z1} &= 2.77 \text{ kHz} \\
f_{z2} &= 2.77 \text{ kHz} \\
f_{p1} &= 60 \text{ kHz} \\
f_{p2} &= 90 \text{ kHz}
\end{aligned} \tag{31}$$

From **Figure 3**, it can be seen that the loop gain is given by:

$$T(s) = kG_c(s) F_M G_{vd}(s) \tag{32}$$

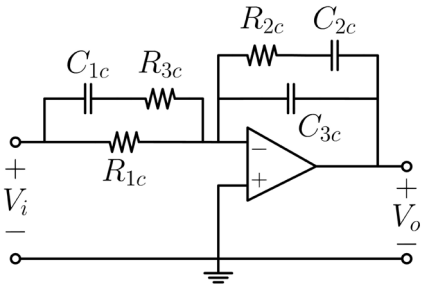

Figure 4. Integrator plus lead-lag compensator.

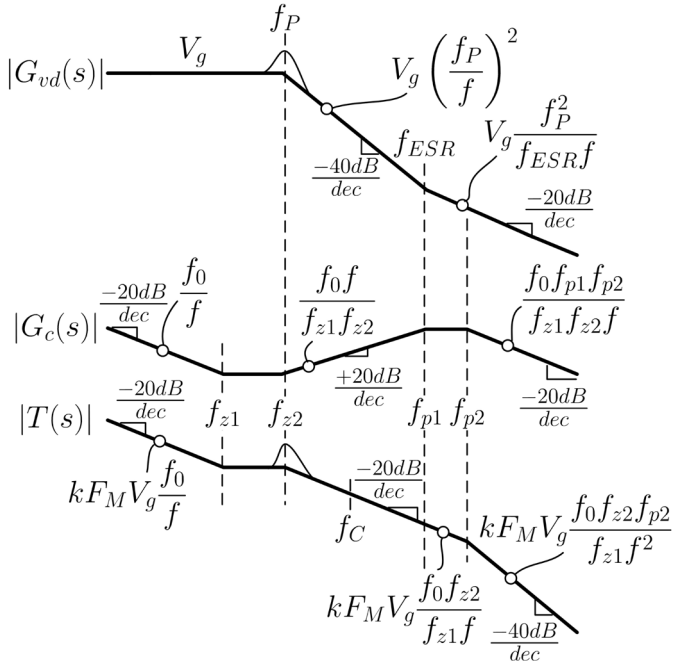

Figure 5. Bode magnitude asymptotes for the control-to-output transfer function $G_{vd}(s)$, the integrator with lead-lag compensator gain $G_c(s)$, and the loop gain $T(s)$. The horizontal axis frequency in Hz. on a log scale and the vertical axis is magnitude of the appropriate transfer function on a dB scale. The magnitude annotations represent absolute gain values varying with frequency f along the various straight line segments.

where the modulator gain $F_M \triangleq \frac{1}{V_M}$. The asymptotic gains of $G_{vd}(s)$, $G_c(s)$, and $T(s)$ are given in Figure 5. These plots have been annotated by the absolute gains that appear along each straight line segment. In particular, in the vicinity of the desirable unity gain crossover frequency f_C of the loop gain $T(s)$, that is, in the frequency interval $f \in \left[f_P, f_{p2}\right]$, the gain is given by:

$$\left|T(j2\pi f)\right|_{f\in\left[f_P,f_{p2}\right]} = kF_MV_g\frac{f_0 f_{z2}}{f_{z1}f} \tag{33}$$

Setting $f = f_C$ in (33) and making $f_0\left(=\frac{\omega_0}{2\pi}\right)$ the subject of the expression

gives

$$f_0 = \frac{f_{z1} f_C}{k F_M V_g f_{z2}} \tag{34}$$

Choosing a crossover frequency f_C of 10 kHz results in:

$$f_0 = 3 \text{ kHz} \tag{35}$$

The chosen component values for the compensator which satisfy the determined gain and zero and pole locations are:

$$\begin{aligned} R_{1c} &= 47 \text{ k}\Omega \\ R_{2c} &= 56 \text{ k}\Omega \\ R_{3c} &= 2.2 \text{ k}\Omega \\ C_{1c} &= 1.2 \text{ nF} \\ C_{2c} &= 1 \text{ nF} \\ C_{3c} &= 33 \text{ pF} \end{aligned} \tag{36}$$

Figure 6 shows the Bode plot of the loop gain evaluated by MATLAB using the exact transfer function expression of G_{vd}. The achieved unity gain crossover frequency is seen to be 16 kHz, which is slightly greater than the 10 kHz specified due the approximate formulas used. The phase margin is seen to be 56.4˚. Thus, with a switching frequency of 100 kHz, a wide loop bandwidth can be seen to be achieved with a good level of stability margin.

A constructed prototype of a closed loop voltage regulator featuring a C1 converter is shown in Figure 7. This schematic also shows a voltage switching circuit by which the input voltage to the converter, v_g, can be switched between two levels. Furthermore, the schematic also shows an output load switching circuit by which the load resistance is switched between two values.

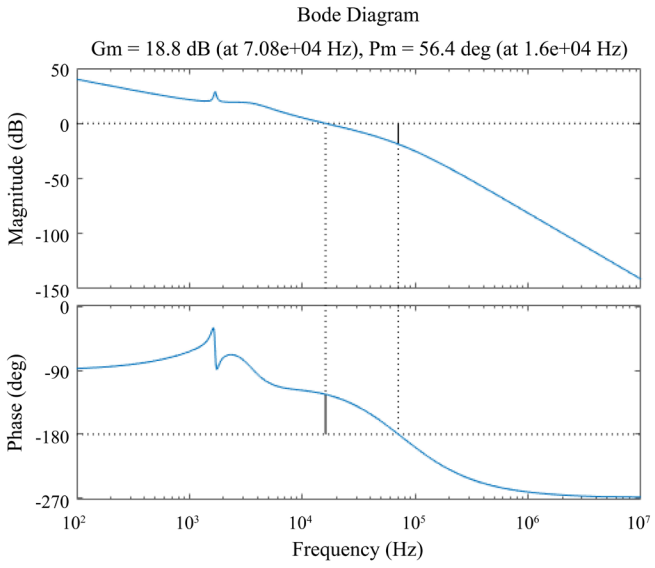

Figure 6. Loop gain of the voltage regulator system using the C1 converter power stage. The unity gain crossover frequency is confirmed to be 16 kHz and the phase margin is 56.4˚. The converter switching frequency is 100 kHz.

Figure 8 shows the converter output voltage transient response when the converter input voltage v_g is stepped from 10 V to 11 V and then back to 10 V. Figure 9 shows the output voltage response to a step load change. The load changes from 5 ohms to 5 ohms in parallel with 10 ohms, *i.e.* 3.3 ohms. These responses confirm the wide bandwidth and stability margin achieved. (Note: not shown in the schematic is a series connection of a 10 ohm resistor and 47 μF capacitor that was placed across the capacitor which is between the two converter inductors. This dampened the slight oscillation that appeared in the output responses. However, this damping network is not seen as essential.)

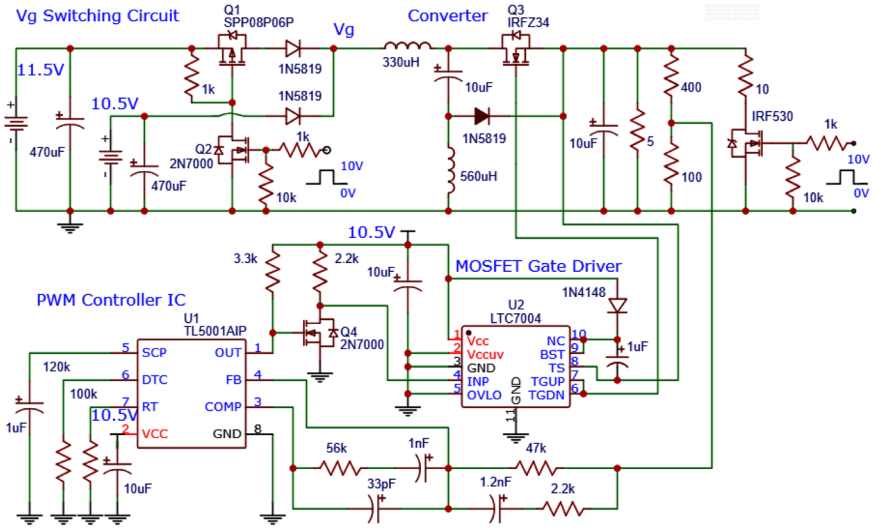

Figure 7. Constructed prototype of the C1 converter in closed loop, together with an input voltage switching circuit and also an output load switching circuit.

Figure 8. Output voltage response due to step input voltage change. Input voltage V_g is stepped from 10 V to 11 V and then back to 10 V. Top curve: gate drive signal to the 2N7000 Mosfet of the voltage stepping circuit, vertical scale: 5 V/div. Middle curve: input voltage to the C1 converter, showing the step changes between 10 V and 11 V, vertical scale: 2 V/div. Bottom curve: output voltage changes, vertical scale: 50 mV/div.

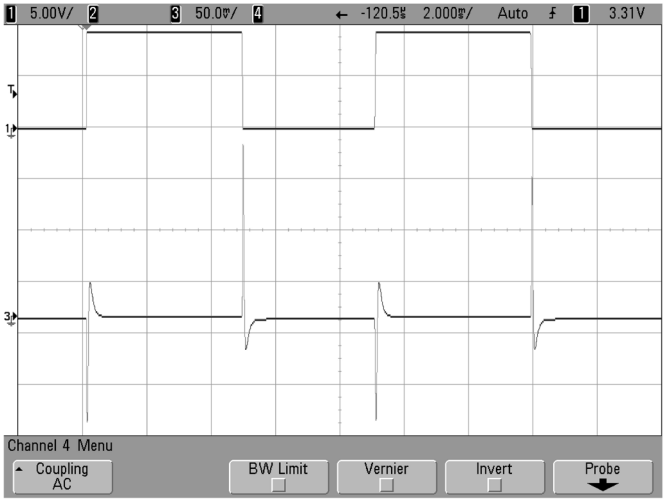

Figure 9. Output voltage response due to step load changes. The load changes from 5 ohms to 5 ohms in parallel with 10 ohms. Top curve: gate drive signal to the IRF530 Mosfet of the load stepping circuit, vertical scale: 5 V/div. Bottom curve: output voltage changes, vertical scale: 50 mV/div.

5.3. Inductor Coupling Consideration

Although not adopted in our design it is possible to couple the inductors which can enhance ripple performance. For the present design with the component values of L_1 and L_2 as determined previously, the output voltage ripple can be reduced by:

$$\frac{\Delta^2 v_2 - \Delta^2 v_{2M}}{\Delta^2 v_2} = \frac{L_1}{L_1 + L_2} = 11.5\% \tag{37}$$

6. Conclusions

Complete DC (steady state average and peak-to-peak ripple values) and small-signal AC analyses of the C1 converter have been presented. Furthermore, a design approach has been elucidated. The process for determining reasonable component values from constraints avoiding DCM and DVM operation, avoiding a RHP zero, and ensuring the validity of a denominator factorization of the control-to-output transfer function has been outlined and carried out along with the design of a feedback loop frequency compensator using asymptotic gain plots, improving transient step response and system stability. The denominator factorization of the control-to-output transfer function and corresponding constraints allow the C1 converter to behave similar to a second-order converter, with a second-order complex double zero canceling a second-order complex double pole. The impact of introducing mutual inductance M between the two inductors in the power stage of the C1 converter was also investigated, yielding an expression for the optimum mutual inductance M_{opt}, the benefits of an avoided RHP zero, and a simple equation to determine the decrease in output voltage ripple.

In summary, the benefits of the C1 converter, primarily in terms of favorable control characteristics, have been examined. Furthermore, a number of constraints have been derived which can be used in the design process to optimize both steady state and small signal performance. A design example was presented which validated the approach. It is believed that the C1 converter is a viable alternative in applications where the second order buck converter augmented with an input filter has been traditionally utilized.

Acknowledgements

The following former students in the Electrical and Computer Engineering Department at Portland State University are acknowledged for prototype construction and for providing the oscillograms shown in this paper: Dawei Che, Midrar Adham, Gordon Hoffman and Ali Sheikly.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

References

[1] Tymerski, R. (1988) Topology and Analysis in Power Conversion and Inversion. Ph.D. dissertation, Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA.

[2] Tymerski, R. and Vorperian, V. (1986) Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells. *IEEE International Telecommunications Energy Conference*, (*INTELEC* '86), Toronto, October 1986, 181-195. https://doi.org/10.1109/INTLEC.1986.4794425

[3] Tymerski, R. and Vorperian, V. (1988) Generation and Classification of Switched-Mode DC-to-DC Converters. *IEEE Transactions on Aerospace and Electronic Systems*, **24**, 743-754. https://doi.org/10.1109/7.18641

[4] White, J.L. and Muldoon, W.J. (1987) Two Inductor Boost and Buck Converters. *IEEE Power Electronics Specialist Conference*, Blacksburg, VA, June 1987, 387-392. https://doi.org/10.1109/PESC.1987.7077206

[5] Veerachary, M. (2011) Fourth-Order Buck Converter for Maximum Power Point Tracking Applications. *IEEE Transactions on Aerospace and Electronic Systems*, **47**, 896-911. https://doi.org/10.1109/TAES.2011.5751233

[6] Middlebrook, R.D. and Cuk, S. (1977) A General Unified Approach to Modelling Switch-Converter Power Stages. *International Journal of Electronics*, **42**, 521-550. https://doi.org/10.1080/00207217708900678

[7] Middlebrook, R.D. (1976) Input Filter Considerations in Design and Application of Switching Regulators. *IEEE Industry Applications Society Annual Meeting*, Chicago, IL, October 1976, 366-382.

[8] Middlebrook, R.D. (1978) Design Techniques for Preventing Input Filter Oscillations in Switched-Mode Regulators. *Proceedings of Powercon* 5, San Francisco, CA, May 1978, A3.1-A3.16.

[9] Tymerski, R. and Li, D. (1993) Extended Ripple Analysis of PWM DC-to-DC Converters. *IEEE Transactions on Power Electronics*, **8**, 588-595. https://doi.org/10.1109/63.261031

Appendix A

Inductor Coupling

Coupling the inductors L_1 and L_2 has the potential of reducing the output voltage ripple $\Delta^2 v_2$. The output voltage ripple with a nonzero mutual inductance M will be denoted $\Delta^2 v_{2M}$. For some switched power converters output voltage ripple v_2 can be completely nulled with inductor coupling, however for the C1 converter only reduction is possible. An optimum value of M, denoted M_{opt}, will first be derived for the C1 converter based on the expressions $\Delta^2 v_2$ and $\Delta^2 v_{2M}$. The effect of M on $G_{vd}(s)$ will then be investigated to determine whether M_{opt} is practical and to point out any advantages or disadvantages to inductor coupling.

1) Optimum value for M

The mutual inductance M between two inductors L_1 and L_2 can be expressed as:

$$M = k\sqrt{L_1 L_2} \tag{38}$$

where the constant k is the coefficient of coupling that is restricted to $-1 \le k \le 1$. Defining α to be the ratio between L_1 and L_2 such that:

$$\alpha \triangleq \frac{L_2}{L_1} \Rightarrow L_2 = \alpha L_1 \tag{39}$$

Substituting (39) into (38) gives a new expression for M:

$$M = L_1 k\sqrt{\alpha} \tag{40}$$

Obtaining an expression for $\Delta^2 v_{2M}$ is accomplished by utilizing the procedure in [4] as was done with the uncoupled case. Introducing M affects the inductor voltages such that:

$$v_{L_1} = L_1 \frac{\mathrm{d}i_1}{\mathrm{d}t} + M \frac{\mathrm{d}i_2}{\mathrm{d}t} \tag{41}$$

$$-v_{L_2} = M \frac{\mathrm{d}i_1}{\mathrm{d}t} + L_2 \frac{\mathrm{d}i_2}{\mathrm{d}t} \tag{42}$$

With (7.1) considered an expression for $\Delta^2 v_{2M}$ is found:

$$\Delta^2 v_{2M} = \frac{V_g DD' T_s^2}{8C_2} \cdot \frac{L_1 + L_2 - 2M}{L_1 L_2 - M^2} \tag{43}$$

Equation (43) reduces to the result in (6) for $M = 0$. Comparing (6) to (43) to consider the effect of M means that only the factor containing M is of interest, which will be treated as a function f, where:

$$f(M) = \frac{L_1 + L_2 - 2M}{L_1 L_2 - M^2} \tag{44}$$

It can be seen from (44) that the denominator is only affected by the magnitude of M and is independent of the sign while the numerator clearly reduces with a positive M and increases with a negative M, so that a negative M actually increases the output ripple, $\Delta^2 v_{2M}$ from the uncoupled case. Substituting (39)

and (40) into (44) and dropping factors that are not affected by *M*:

$$f(M)=\frac{L_1+L_2-2M}{L_1L_2-M^2}=\frac{1+\alpha-2k\sqrt{\alpha}}{L_1\alpha\left(1-k^2\right)}=f(\alpha,k) \tag{45}$$

Differentiating (45) with respect to α and *k*:

$$\frac{\partial f}{\partial \alpha}=\frac{1-k\sqrt{\alpha}}{L_1\alpha^2\left(k^2-1\right)} \tag{46}$$

$$\frac{\partial f}{\partial k}=\frac{-2\left(k^2\sqrt{\alpha}-k(\alpha+1)+\sqrt{\alpha}\right)}{L_1\left(k^2-1\right)^2\alpha} \tag{47}$$

reveals that both $\frac{\partial f}{\partial \alpha}$ and $\frac{\partial f}{\partial k}$ go to zero when:

$$k\sqrt{\alpha}=1 \tag{48}$$

This means that *f* is at its minimum when (48) is satisfied. Substituting (48) into (40) we find the optimum value of *M*:

$$M_{opt}=L_1 \tag{49}$$

2) Effect of Mutual Inductance

The $G_{vd}(s)$ with a nonzero *M* becomes:

$$G_{vd}(s)=\frac{V_g\left(s^2N_2+sN_1+1\right)}{s^4D_4+s^3D_3+s^2D_2+sD_1+1} \tag{50}$$

where

$$\begin{aligned}
N_1&=\frac{D}{R}\left[-DL_1+D'L_2+(2D-1)M\right]\\
N_2&=(L_1+L_2-2M)C_1\\
D_1&=\frac{D^2L_1+D'^2L_2+2DD'M}{R}\\
D_2&=(L_1+L_2-2M)C_1+\left(D^2L_1+D'^2L_2+2DD'M\right)C_2\\
D_3&=\frac{\left(L_1L_2-M^2\right)C_1}{R}\\
D_4&=\left(L_1L_2-M^2\right)C_1C_2
\end{aligned} \tag{51}$$

The RHP zero is avoided when coefficient N_1 is positive. Substituting the optimum value of *M*, *i.e.* $M_{opt}=L_1$, into N_1 leads to:

$$N_1=\frac{DD'}{R}(L_2-L_1) \tag{52}$$

so the RHP zero is avoided when $L_2>L_1$, a condition which is already satisfied by the denominator factorization constraint $D'L_2\gg L_1$. The complex second order zero and pole locations are contained in the coefficients N_2 and D_4, respectively. Substituting M_{opt} into N_2 and applying the aforementioned constraint leads to:

$$N_2=(L_2-L_1)C_1\approx L_2C_1 \tag{53}$$

which is the same coefficient used in the uncoupled case, therefore the zero location used in the compensator design is still valid. Now substituting M_{opt} into D_4 and also applying the denominator factorization constraint gives:

$$D_4 = L_1\left(L_2 - L_1\right)C_1C_2 \approx L_1L_2C_1C_2 \tag{54}$$

It is evident that the approximate pole locations determined by the denominator factorization are also still valid. Taking a look at D_3 in a similar fashion shows that it is also unchanged:

$$D_3 = \frac{\left(L_1L_2 - M^2\right)C_1}{R} \approx \frac{L_1L_2C_1}{R} \tag{55}$$

suggesting that there is a negligible change in the Q factors of the complex second order double poles as well.

With the RHP zero avoided and the complex second order zero and pole locations still valid, coupling L_1 and L_2 only has the disadvantages associated with physical implementation. Using the optimum M reduces $\Delta^2 v_2$ by a factor of:

$$\frac{\Delta^2 v_2}{\Delta^2 v_{2M}} = \frac{L_1 + L_2}{L_2} \tag{56}$$

from the uncoupled case, thus coupling the inductors can either reduce the output voltage ripple by as much as 50% for $L_1 \approx L_2$ or by a negligible percentage for a very large α.