

Model Design of Electrically Erasable EEPROM Memory Cell

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Abstract

This article introduces an EEPROM memory cell model that is different from the equivalent capacitance model. This model uses high-frequency components in circuit design, including MOS transistors, zener diodes, resistors, capacitors, etc., and builds a model that can be used in most analog environments. The simulation of the transient process of write and read operations helps designers understand the working principle of EEPROM, and it can also be applied to the overall circuit design. According to the structure and working principle of the EEPROM cell device, a model of its equivalent circuit is established, and the read, write, and erase operations of the EEPROM cell are transiently simulated using this model. The simulation results verify the correctness of the model.

Keywords

EEPROM Memory, Circuit Design, Circuit Simulation

1. Introduction

Flash Memory is gradually becoming the mainstream of mobile information equipment with high requirements on size, power consumption and flexibility due to its sturdy and compact integrated structure, low power consumption, and fast reading and writing [1]. The field still has huge advantages. Its biggest advantages are its ease of use, flexible working methods and low cost. At present, EEPROM is used in many fields, such as embedded data storage systems and mobile communication equipment. Among them, there is also a huge market in various types of smart cards that are rapidly developing around the world [2]. The performance of EEPROM memory has a direct impact on the stability of the system or device in which it is used. Therefore, how to design a circuit with high speed, low power consumption, high stability, and strong reusability has become

the key [3]. Although EEPROM is called Electrically Erasable Programmable Read-Only Memory, it is more than just a read operation. It has the characteristics of both RAM and ROM. It can read and write data randomly like RAM. At the same time, it can maintain the data stored before power-off when it is not powered. This is the same characteristic as ROM. After years of development, in recent years, the EEPROM has reached 100,000 times of re-erasable, and the stored data has been reliably maintained for more than 10 years [4].

Although EEPROM is slightly slower in reading and writing compared with the rapidly developing Flash (Flash Memory), its process is more mature and stable, and its cost is lower, so it is still the mainstream application [5] [6]. Every aspect of people's daily life must be exposed to EEPROM, in the field of smart cards such as identity cards, bank cards, medical insurance cards, transportation cards, etc., which are related to personal and financial matters [7] [8]. In the field of communication systems that are closely related to communicating with others, and other consumer electronics products such as PDAs and digital cameras, EEPROMs are used [9]. In instruments and other embedded systems (such as smart flow meters), it is usually necessary to store some setting parameters, field data, and other information. These information requirements are not lost when the system is powered off, and the original settings can be restored next time. Therefore, a certain amount of EEPROM is also required. In addition, EEPROMs are classified according to the number of programmable times as MTP (Multiple Time Memory). Traditional multi-time programmable memory uses a standard CMOS process, also known as pure logic NVM. Its biggest advantage is that it is fully compatible with standard CMOS processes, no additional process steps are required, and the technology is simple, reliable and mature. The voltage required for pure logic NVM programming is about 10 V, which is much lower than the programming voltage of EEPROM, and the power consumption of the circuit is low. However, because the memory cells using the standard CMOS process are implemented in a differential form, the number of MOS transistors is large, resulting in a large increase in chip size and an increase in cost [10].

Based on the above analysis, it is undeniable that EEPROM is the preferred position of RFID tag chip memory. The research on reliable low-power EEPROM suitable for UHF RFID is of practical significance and practical value. This article strives to design the model of EEPROM cell and its simulation analysis. It also analyzes and discusses various failure mechanisms and parasitic effects that may occur. According to the structure and working principle of the EEPROM cell device, a model of its equivalent circuit is established, and the read, write, and erase operations of the EEPROM cell are transiently simulated using this model. The simulation results verify the correctness of the model. It's very important for EEPROM, directly related to the success of its design.

2. Methods

2.1. EEPROM Cell Structure

The floating gate type EEPROM memory cell uses two tube cells, one is an

NMOS selection tube, and the address selection of the cell is used [10]. The gate is connected to the Word Line (WL) and its drain Bit Line (BL). When performing a read operation, add a level of about 2.5 V to the control grid of the FLOTOX tube. Due to the previous erase and write operations, the turn-on voltage of the storage tube on the selected byte is different, some are cut off, and some are turned on. From this, it can be discriminated whether the unit stores “1” or “0”.

2.2. Design of the Storage Unit Model

Many circuit design model libraries do not provide usable memory cell models, so designers need to build a suitable cell model. The simplest model uses the equivalent capacitance model, that is, equivalent capacitance is used between the double gates and between the floating gate and the drain-source, and then the coupling current is used to calculate the tunnel current, charge accumulation, and threshold voltage changes.

The capacitance equivalent model is currently the simplest and most convenient model, but there are huge flaws that make it impossible to accurately simulate device operation. First, the specific situation of current generation cannot be obtained. Second, because the actual situation is far more complicated than the charging and discharging process of several capacitors, and also includes various channel effects and charge trap defects, the overall working process is prone to deviations.

Based on the above reasons, this article introduces an EEPROM memory cell model that is different from the equivalent capacitance model. This model uses high-frequency components in circuit design, including MOS transistors, zener diodes, resistors, capacitors, etc., and builds a model that can be used in most analog environments. The simulation of the transient process of write and read operations helps designers understand the working principle of EEPROM, and it can also be applied to the overall circuit design.

The flashing process of the EEPROM unit changes the threshold voltage of the FLOTOX tube. When the model is established, the charge and discharge characteristics of the capacitor can be used to simulate this change. An NMOS tube with a variable threshold voltage is equivalent to a common NMOS tube and a voltage-controlled voltage source in series, so that the transistor has different threshold voltages in different states. The size of the voltage source is determined by the voltage of the capacitor. The capacitor records Erase process. **Figure 1** is the equivalent circuit diagram of the model. This equivalent circuit uses devices such as NMOS tubes, capacitors, resistors, zener diodes, and voltage-controlled voltage sources.

Model equivalent circuit diagram of EEPROM cell is shown in **Figure 1**, the erase, write, and read operations of the EEPROM memory cell and the conversion between the three can be achieved. The transistors from left to right are NM0, NM2, NM3, NM4, and NM1. The two resistors from left to right are R_e and R_w . The two Zener tubes are D0 and D3. It works as described below.

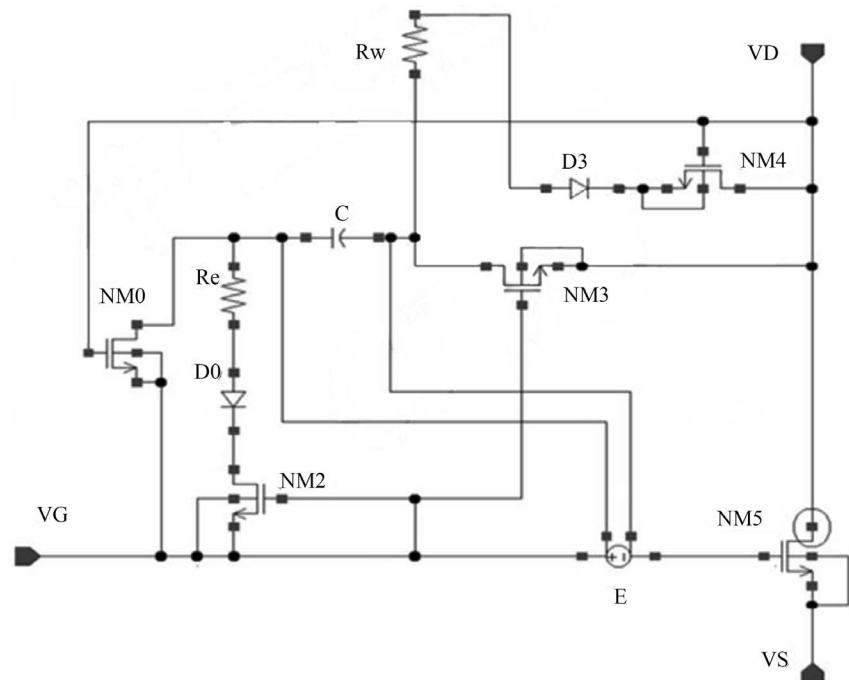


Figure 1. Model equivalent circuit diagram of EEPROM cell.

When erasing, the gate input is high level and the drain terminal is low level. If the high level is large enough to make D0 breakdown, the capacitor C is charged so that it can affect the voltage source E and make E with a reverse voltage, point D reads high.

When writing, the gate is at a low potential and the drain is at a high potential. When the potential of VD is greater than the breakdown voltage of $D3$, $D3$ breaks down, charges capacitor C , and V_c acts on E again, causing E to generate a positive voltage. $NM1$ is on, and point D is read as low level.

2.3. Storage Model Parameter Setting

Model parameters have a lot to do with the process used. First, the capacitance is calculated from Equation (1):

$$C = \frac{\epsilon\epsilon_{SiO_2}S}{d} \quad (1)$$

where ϵ —vacuum dielectric constant; ϵ_{SiO_2} —the relative permittivity of silicon dioxide to vacuum; S —Tunnel hole area (μm^2); d —thickness of gate oxide layer (nm).

In our work, we use a $0.5 \mu m$ CMOS process. According to the model file, the gate oxide layer thickness is 15.8 nm , and S is set to $0.5 \mu m^2$. Therefore, the calculated capacitance is 0.055 pF .

The voltage regulation value of $D0$ should be smaller than the breakdown voltage of the floating gate window during erasing, and the voltage regulation value of $D3$ should also be smaller than the breakdown voltage during writing. In the case of symmetrical writing and erasure, the voltage regulation values of $D0$ and

D_3 Can be the same. Because the erasure high voltage V_b of this article is 20 V and the breakdown voltage is 11 V, assuming that the erasure is symmetrical, the voltage regulation value can be taken as 10 V.

The voltage-controlled voltage source E0 needs to set the voltage gain α , and its calculation formula is: $\alpha = (V_{th} - V_{thn}) / (V_{hw} - V_Z)$. α represents the ratio of the change in the threshold voltage of the MOS tube after the voltage is wiped to the voltage on both sides of the capacitor (that is, the difference between the applied high voltage and the voltage drop of the zener diode). After calculation, we get $\alpha = 0.3$.

R_e and R_w are erasing and writing time control resistors, respectively. During the work process, the operating time cannot be infinite, so the following time relationships exist: $R_e C < T_{e_{max}}$ and $R_w C < T_{w_{max}}$. In the circuit designed in this article, the erasing time is required to be less than 1 ms, so two ranges of resistance can be obtained, and then a suitable value is selected according to the overall situation. Based on the above analysis, the model parameter values shown in **Table 1** can be obtained.

Using the circuit design software Cadence Virtuoso Schematic Composer to simulate and analyze the floating-gate EEPROM device model designed in this paper, we can get its electrical characteristics. Set the initial write condition VS = 0, VG rises linearly from 10 V to 20 V, time $t = 0.15$ ms, according to the simulation results, we can get the following observations:

1) The threshold voltage of the floating gate device in the initial state is 0.6 V. This is based on the drain current I_{ds} and the control gate voltage V_{gs} . The characteristic curve is obtained in **Figure 2**. The I_{ds} - V_{gs} characteristic curve rises rapidly first, and then does not change after reaching a maximum value. Make a tangent at the maximum slope of the I_{ds} - V_{gs} curve. After the tangent is properly extended, it will produce an intersection with V_{gs} . The value of this point is the threshold voltage. It can be concluded that the threshold voltage in the initial state is 0.6 V.

2) Relation between threshold voltage with operating time and control gate voltage. **Figure 3** shows the change of the threshold voltage. It can be seen from the figure that the threshold voltage varies with the control gate voltage. When the value of VG increases, the change value of the threshold voltage ΔVT also

Table 1. Model equivalent component values.

parameters	Values
Erase capacitor	0.055 pf
D1, D2 voltage regulation value	10 V
NMOS threshold voltage V_{th}	0.75 V
Erase time resistance R_e	7.9×10^9
Write time resistance R_w	7.9×10^9
Voltage controlled voltage source gain α	0.3

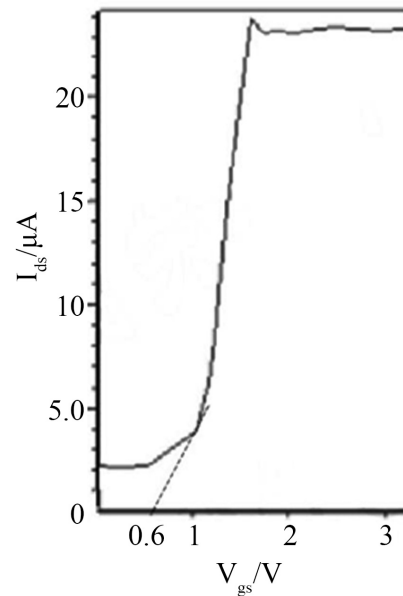


Figure 2. Ids-Vgs relationship diagram of EEPROM.

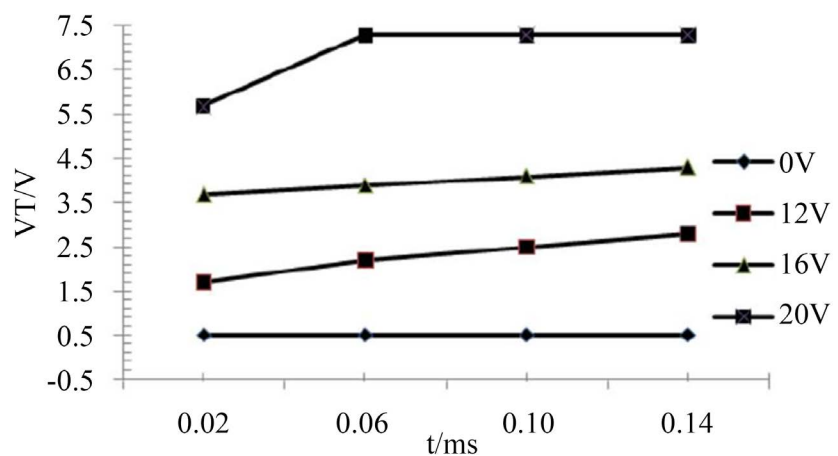


Figure 3. Variation of threshold voltage with time and gate voltage.

increases. The larger the ΔV_T , the better the anti-interference ability of the storage unit. Therefore, within a proper range, the larger the applied voltage, the better the performance of the memory cell. Beyond this appropriate range, the probability of the tunnel oxide layer being penetrated will increase, which will make the system unstable and even damage the device. In addition, it will easily cause other series of problems, such as increased time delay and increased difficulty in boosting as well as high power consumption. The high voltage required for this article is 20 V, which is determined on the basis of experience with reference to the EEPROM use voltage values that exist on the market. It can also be seen from **Figure 4** that the threshold voltage changes with time. As the writing time increases, ΔV_T also increases. However, when the write time is greater than 0.06 ms, the increase of the threshold voltage becomes small and very slow, so a value between 0.06 ms and 0.1 ms can be selected.

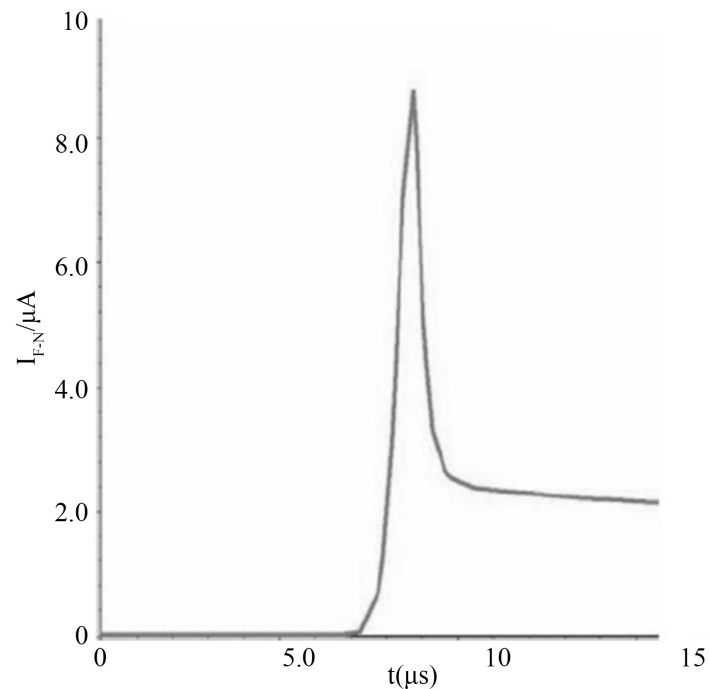


Figure 4. Relationship between floating gate current and time.

3) The relationship between the voltage on the control gate and the floating gate current (F-N current) and the write time. In a short period of time, the high voltage level can reach its maximum. When the voltage reaches its maximum value, it no longer changes with time. As can be seen from the relationship between current and time in **Figure 4**, the F-N current reached its maximum value at $t = 0.08$ ms. That is to say, it can write or erase to the units quickly. It is synchronized with threshold voltage changes. Therefore, it can be judged that the change of the current is synchronized with the control gate voltage. This is because although the voltage increases rapidly, it sometimes reaches saturation. However, the electric field still exists, and it continues to attract electrons to the floating gate. As the electric charge continues to accumulate, a part of the electric field is canceled, causing the phenomenon of the electric field strength to continue to decrease. Until it is less than a specific value (10^7 V/cm), the electron terminates tunneling, The tunneling current disappears. Therefore, when the voltage reaches the maximum value and is constant, the F-N current decreases rapidly with the increase of time. Ideally, it should be reduced to 0. In this paper, due to the static current in the model, a small current still exists. It can be seen that when designing the cell structure, how to make the capacitor voltage between the floating gate and the drain region rise rapidly is also a factor to be considered.

3. Conclusions and Discussion

We mainly introduce the design of the timing circuit, address decoding circuit and register circuit of the digital module part in EEPROM IP. The row address

decoding uses a two-stage decoding method, which can reduce the delay problem in the information transmission process and optimize the circuit area. At the same time, a model of the memory cell was built and simulated. The effects of the control gate voltage and write time on the performance of the floating gate EEPROM device were analyzed through the simulation results, which provided a basis for the model parameter verification. Combining the three conclusions for an overall analysis, factors such as gate voltage and write time will play a significant role in the performance of the EEPROM memory. According to the simulation results, combined with the 0.5 μm COMS process technology, when the write voltage is 20 V and the write time is about 0.1 ms, the voltage rise time is sufficiently small. This conclusion is in line with the preceding statement: when the write time is greater than 0.06 ms, the increase of the threshold voltage becomes small and very slow, so a value between 0.06 ms and 0.1 ms can be selected. The EEPROM device model designed in this paper can work well and achieve better memory functions, higher work efficiency and lower power consumption.

In the future, we need to solve the problem of its reliability, the most important of which is endurance and data retention. In addition, we will research the interference generated in programming and erasure, which is also a factor affecting reliability.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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