Journal of Applied Mathematics and Physics, 2020, 8, 218-228
https://www.scirp.org/journal/jamp
ISSN Online: 2327-4379
ISSN Print: 2327-4352

Design and Simulation of Improved SOI SiGe Hetero-Junction Bipolar Transistor Architecture with Strain Engineering

Naidan Miao[1], Peipei Liu[1], Jianhao Wen[1], Jinxi Wei[1], Baichuan Zhang[1], Shiqi Wang[1], Ruwen Zeng[1], Guanyu Wang[1*], Chunyu Zhou[2*]

[1]College of Electronic Engineering, Chongqing University of Posts and Telecommunications, Chongqing, China
[2]Key Lab. for Microstruc. Mater. Phys. of Hebei Province, Yanshan University, Qinhuangdao, China
Email: *wangguanyu@cqupt.edu.cn, *zhouchunyu@ysu.edu.cn

How to cite this paper: Miao, N.D., Liu, P.P., Wen, J.H., Wei, J.X., Zhang, B.C., Wang, S.Q., Zeng, R.W., Wang, G.Y. and Zhou, C.Y. (2020) Design and Simulation of Improved SOI SiGe Hetero-Junction Bipolar Transistor Architecture with Strain Engineering. *Journal of Applied Mathematics and Physics*, **8**, 218-228.
https://doi.org/10.4236/jamp.2020.82017

Received: December 26, 2019
Accepted: January 17, 2020
Published: January 20, 2020

Abstract

In order to improve the electrical and frequency characteristics of SiGe heterojunction bipolar transistors (HBTs), a novel structure of SOI SiGe heterojunction bipolar transistor is designed in this work. Compared with traditional SOI SiGe HBT, the proposed device structure has smaller window widths of emitter and collector areas. Under the act of additional uniaxial stress induced by $Si_{0.85}Ge_{0.15}$, all the collector region, base region and emitter region are strained, which is beneficial to improve the performance of SiGe HBTs. Employing the SILVACO® TCAD tools, the numerical simulation results show that the maximum current gain β_{max}, the Earley voltage V_A are achieved for 1062 and 186 V, respectively, the product of β and V_A, *i.e.*, $\beta \times V_A$, is 1.975×10^5 V and, the peak cutoff frequency f_T is 419 GHz when the Ge component in the base has configured to be a trapezoidal distribution. The proposed SOI SiGe HBT architecture has a 52.9% improvement in cutoff frequency f_T compared to the conventional SOI SiGe HBTs.

Keywords

Uniaxial Strain, SOI SiGe HBT, Electrical Performance, Frequency Performance

1. Introduction

Recently, there has been increased interest in SiGe HBT technology for microwave RF circuits because of its high-frequency and compatibility with silicon technology [1]. Several works have been reported on optimizing the high-frequency of SiGe HBT that can be found from the refs. [2] [3] [4] [5]. Also, the ref. [6] has

been proved that reducing the width of the emitter can greatly improve the frequency of SiGe HBT. In addition, the band structure of silicon can be changed by introducing global strain or local strain to improve carrier mobility has been reported [7] [8]. Scholars have improved the performance of SiGe HBT by using stacked metal interconnect structures or introducing mechanical stress [9] [10]. But the reliability is poor, and the process is not easy to control. A SiGe HBT device structure with a virtual substrate was proposed in ref. [11], which effectively improved the current gain. However, the improvement of frequency characteristics is limited, and the self-heating effect of the substrate is significant. Therefore, the introduction of strain engineering can reduce the transit time of carriers in the collector, and effectively improve the frequency characteristics of the device.

In this paper, the proposed device improves the frequency characteristics by introducing stress, and uses SOI substrate structure with buried oxygen layer is used to reduce the self-heating effect brought by virtual substrate. First, the SOI technology and strain silicon technology are combined to introduce uniaxial stress into the SOI collector with N^+ buried layer to form a new SOI SiGe HBT device structure. Then, the effects of Ge component on the current gain, Early voltage and cut-off frequency are briefly described. Finally, the structure has been proved to be able to achieve breakthroughs in the key frequency characteristics, *i.e.* $f_T > 400$ GHz.

2. Device Model and Process Simulation Flow

In this paper, a two-dimensional device model is established by using SILVACO® TCAD tools and the ATHENA module is then employed to simulate the process flow. The proposed device architecture is shown in **Figure 1**.

The widths of the emitter window and the collector window are 120 nm and 400 nm, respectively, which are following the size-reduction roadmap mentioned in ref. [6]. The characteristics of the device structure are mainly reflected in the stress distribution. Firstly, the strain engineering of "embedded" $Si_{1-y}Ge_y$ source and drain that commonly used in 90 nm, 65 nm and 45 nm CMOS process nodes, is now introduced in the collector region, where uniaxial compressive stress is consequently applied in the horizontal direction. Then, the $Si_{1-x}Ge_x$ base is grown upon the strained collector. Due to the different lattice constants of Si and SiGe, the base region is subject to biaxial compressive stress [12]. According to the principle of elasticity, the collector is uniaxial compressive stressed, and the base is therefore with the act of both the uniaxial and the biaxial stresses. Also, an uniaxial tensile strained cap-layer is sandwiched between poly-silicon and $Si_{1-x}Ge_x$ base to build a double-layer "composite" emitter architecture [13]. The device model parameters are listed in **Table 1**.

The manufacture process simulation of the proposed SOI SiGe HBT mainly includes the following 6 steps: 1) Initialize (100) p-Si substrate; 2) Buried Oxide layer (BOX) is grown at 850˚C, then n^+ buried layer and n^- collector are sequentially grown upon the BOX layer; 3) Two grooves are etched into the n^- collector

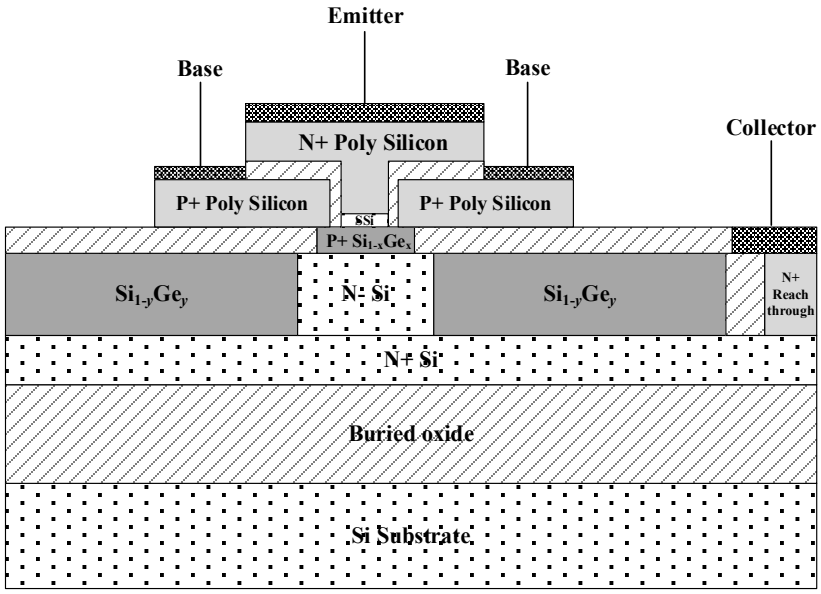

Figure 1. Structure of proposed SOI SiGe HBT device.

Table 1. Structural parameters of SOI SiGe HBT.

Region	Parameters			
	Material	Thickness (nm)	Doping (cm^{-3})	Ge component
Strain silicon in Emitter	Si	12	1×10^{18}	0
Polysilicon in Emitter	Poly Si	88	1×10^{20}	0
Base	$Si_{1-x}Ge_x$	20	1×10^{19}	15 - 30
Collector	Si	60	5×10^{17}	0
Collector stress region	$Si_{1-y}Ge_y$	60	0	15
N^+ silicon	Si	20	1×10^{20}	0
Buried oxide	Oxide	100	0	0
Silicon substrate	Si	200	1×10^{15}	0

layer where uniaxial stress generates or applies, and $Si_{1-y}Ge_y$ is deposited in the etched grooves by selective epitaxy growth (SEG); 4) Electrode area of the collector is etched, and heavily-doped poly-silicon as the reach-through area of the collector is deposited; 5) P-type $Si_{1-x}Ge_x$ base, heavily-doped P-type poly-silicon extrinsic base, and multi-layer emitter are successively deposited, and thin oxide films and poly-silicon are deposited by low-pressure chemical vapor deposition (LPCVD); 6) Aluminum (Al) film is finally produced on the whole surface by vacuum evaporation, any metal regions exterior to the electrodes are then removed by photolithography.

3. The Effect of Germanium (Ge) Profile on Current Gain and Early Voltage

The design of the base region is mainly considered from two aspects, one is the

boron doping concentration, the other is the distribution of Ge profile. This paper mainly studies the influence of different Ge profile according to the uniform boron doping concentration in the base region on device performance. The Ge profile in the base region can be classified into three types: box, triangle and trapezoid. Different Ge profile will affect the bandgap of the $Si_{1-x}Ge_x$ base. The bandgap near to the emitter is reasonably configured to be larger than that near to the collector, so the built-in electric field is introduced to accelerate the transport of electrons [14]. The gradient Ge profile generates the acceleration field in the base, and reduces the base transition time, base recombination and increase the current.

Ge profile commonly used in the base of SiGe HBT, X_0 is the boundary of the base near the emitter, X_{WB} is the boundary of the base near the collector, $\Delta E_g(X_0)$ is the band narrowing caused by Ge mole-fraction at X_0, and $\Delta E_g(X_{WB})$ the band narrowing caused by Ge mole-fraction at X_{WB}. The relationship between the graded Ge fraction in the base and the current gain β is obtained by Equation (1) [15].

$$\frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}} \propto \frac{\left[\Delta E_{g,grade}/kT\right]\exp\left[\Delta E_g\left(X_0\right)/kT\right]}{1-\exp\left[-\Delta E_{g,grade}/kT\right]} \tag{1}$$

$$\Delta E_{g,grade} = \Delta E_g\left(X_{W_B}\right) - \Delta E_g\left(X_0\right) \tag{2}$$

The ratio of the current gain of SiGe HBT to that of Si BJT $\beta_{\max}/\beta_{\mathrm{Si}}$ has an exponential relationship with $\Delta E_g(X_0)$. As shown as Equation (2), it is linear with the bandgap difference $\Delta E_{g,\,grade}$ caused by the graded Ge profile in the base. It can be seen that the Ge mole-fraction near the emitter has a significant effect on the current gain. The current gain with trapezoidal Ge distribution is larger than that with triangular Ge distribution when the content of Ge component in the base.

According to Equation (3) [15], the relationship between the Early voltage and the Ge component in the base region is proportional to the bandgap difference $\Delta E_{g,\,grade}$.

$$\frac{V_{\mathrm{A,SiGe}}}{V_{\mathrm{A,Si}}} \propto \frac{\exp\left[-\Delta E_{g,grade}/kT\right]-1}{\Delta E_{g,grade}} \tag{3}$$

The relationship between the current gain and the optimal value of the Early voltage can be obtained [15].

$$\frac{\beta_{\mathrm{SiGe}}\cdot V_{\mathrm{A,SiGe}}}{\beta_{\mathrm{Si}}\cdot V_{\mathrm{A,Si}}} \propto \exp\left[\frac{\Delta E_g\left(X_0\right)}{kT}\right]\cdot\exp\left[\frac{\Delta E_{g,grade}}{kT}\right] \tag{4}$$

According to the above equations, the product of current gain and Early voltage of box Ge profile is smaller than that of Ge component gradient under the base Ge profile is constant.

In the device simulation, V_{CE} was 1.2 V and V_{BE} was varied from 0.1 to 1.2 V. The current gain is obtained and compared as shown in **Figure 2**. Based on the

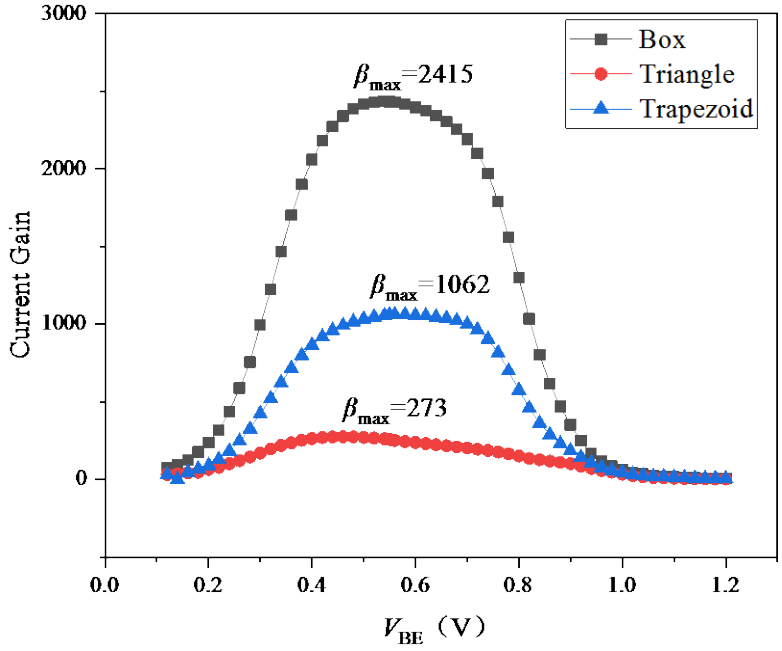

Figure 2. Relationship between β_{max} and V_{BE} with three different distributions of Ge components in the base.

above device structural model, the effects of three base Ge component distributions on current gain are obtained. It can be seen from the β- V_{BE} curve exhibited in Figure 2 that, for the Ge profile in the base, the current gains with box and trapezoid distribution are greater than that with the same distribution of conventional SiGe HBTs. Among them, the maximum gain β_{max} of the box distribution of Ge component in the base is calculated as high as 2415, that of the trapezoid distribution β_{max} is 1062, and that of the triangle distribution β_{max} is 273. Therefore, the current gain of box type is the highest, which is following the above theoretical analysis.

Early voltage is one of the important parameters to characterize the electrical characteristics of devices. When the value of the Early voltage is larger, the width modulation effect in the base is smaller, and the concentration gradient of minority carrier in the base increases, hence the current gain β is naturally increased. The extraction of the value of the Early voltage is through the I_C- V_{CE} curve when I_B is set to be different constant and V_{CE} is close to zero, the tangent intersects the abscissa value, which corresponds to V_A. Therefore, the smoother the I_C- V_{CE} curve, the larger the V_A, and the better output characteristics of the device. When the base Ge component of SOI SiGe HBT is trapezoid-distributed, the output characteristic of the device is shown in Figure 3. The I_C- V_{CE} curves with I_B = 0.05 μA, 0.5 μA, 1 μA and 1.5 μA are selected. The curve is relatively smooth, and the calculated Early voltage V_A is about 186 V.

Figure 4 shows the output characteristic of three different base Ge component distributions when the base current I_B is a fixed value of 1.5 μA, which the influence of Ge component distribution on the output characteristic curve. It can be

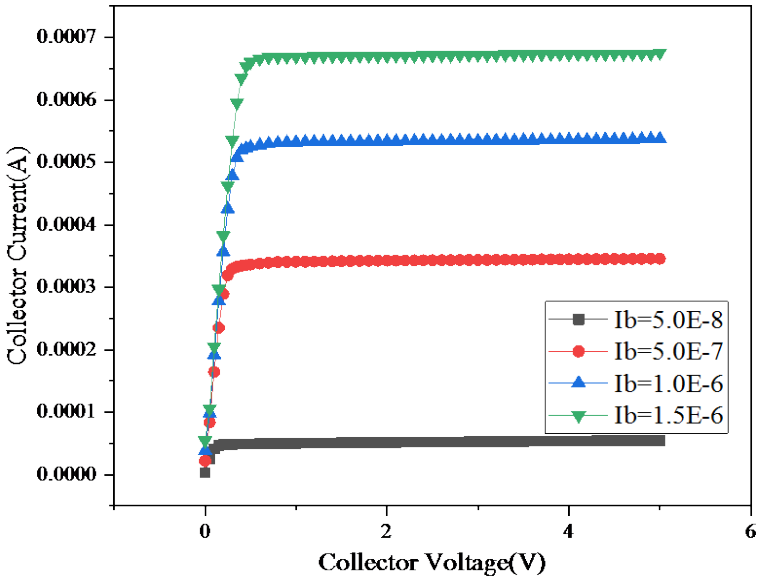

Figure 3. Output characteristics of the device when the Ge component of the base region is trapezoidal.

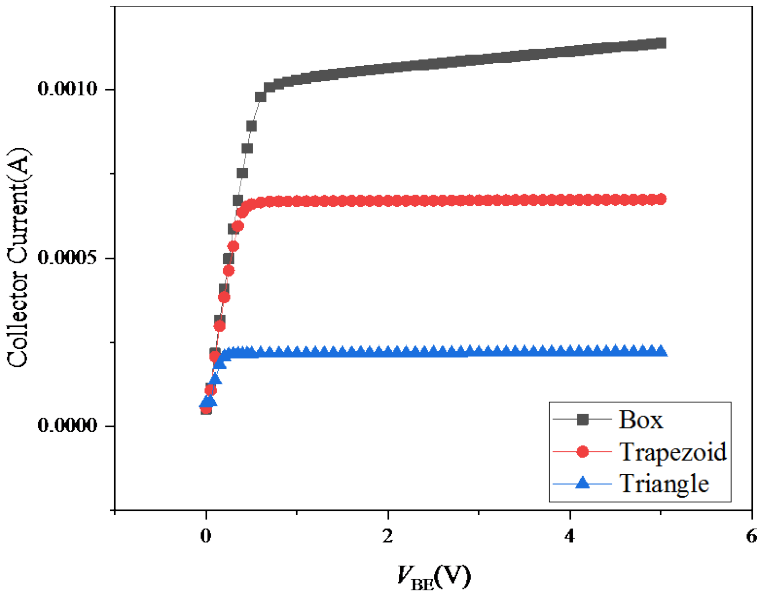

Figure 4. *I- V* characteristics of the three base Ge component distributions @ I_B = 1.5 μA.

seen from the figure that the curve of triangle distribution and trapezoid distribution is relatively smooth, while the curve of box distribution has the largest gradient and the Early voltage is the smallest. The results show that the Early voltage of trapezoid distribution is about 186 V, that of triangle distribution is about 224 V, and that of box distribution is 43 V.

From the simulation results, the maximum values of $\beta \times V_A$ of three Ge component distributions are summarized in Table 2.

It can be concluded that the optimal values of current gain and Early voltage $\beta \times V_A$ are the highest when the base Ge component is trapezoidal.

Table 2. The maximum values of $\beta \times V_A$ of three Ge component distributions.

	Ge component distributions		
	box	trapezoid	triangle
$\beta \times V_A$	1.038×10^5 V	1.975×10^5 V	6.115×10^4 V

4. The Effect of Base Ge Component Distribution on Cut-Off Frequency f_T

One of the key parameters to measure the electrical characteristics of devices is the cut-off frequency f_T, the change of Ge composition in the base mainly affects the transition time τ_B and the transition time τ_E in the emission region. Reducing these two-time constants can effectively improve the frequency characteristics of the device. According to Equation (5), when the base Ge component of SiGe HBT is slowly changing, the relationship between base transition time and emitter transition time and base Ge component respectively.

$$\frac{\tau_{\mathrm{B,SiGe}}}{\tau_{\mathrm{B,Si}}} \propto \frac{\left[1 - kT/\Delta E_{g,grade}\right] \exp^{-\Delta E_{g,grade}/kT}}{\Delta E_{g,grade}} \tag{5}$$

$$\frac{\tau_{\mathrm{E,SiGe}}}{\tau_{\mathrm{E,Si}}} \propto \frac{1 - \exp^{-\Delta E_{g,grade}/kT}}{\Delta E_{g,grade} \exp^{\Delta E_g(X_0)/kT}} \tag{6}$$

Among them, the $\Delta E_{g,\,grade}$ is bandgap differences caused by gradient difference with insignificant Ge component variation. From Equation (5) that $\tau_{\mathrm{B,\,SiGe}}$ is smaller than $\tau_{\mathrm{B,\,Si}}$ due to the existence of bandgap difference. Therefore, the slow change of Ge component in the base region causes the gradual change of energy band to form a built-in electric field to accelerate the electron drift, which shortens the time of minority carrier crossing the base region. According to the formula, when the gradient of Ge component in the base increases, the cutoff frequency f_T will increase. From Equation (6), it can be obviously seen that the ratio of $\tau_{\mathrm{E,\,SiGe}}/\tau_{\mathrm{E,\,Si}}$ is inversely proportional to the narrowing of the bandgap $\Delta E_g(X_0)$ caused by the Ge component on the side near the emission, and is linear with $\Delta E_{g,\,grade}$. Therefore, the key variable affecting the transit time $\tau_{\mathrm{e,\,SiGe}}$ of the emitter is $\Delta E_g(X_0)$. When the base Ge component is trapezoid distributed and the concentration of Ge component close to the emitter is not 0, the $\Delta E_g(X_0)$ and $\Delta E_{g,\,grade}$ increase at the same time. It can effectively reduce the transit time of the emitter, thus increasing the cut-off frequency f_T.

The frequency characteristics of SOI SiGe HBT with different base Ge component distribution are obtained by the ATLAS simulation module as shown in Figure 5. The transit frequency f_T and the maximum oscillation frequency f_{max} were extracted from s-parameter measurements extrapolating current gain h21 and unilateral gain U. The cut-off frequency f_T is the largest, up to 419 GHz, when V_{CE} = 4 V and the Ge component in the base is trapezoidal distribution; the cut-off frequency f_T is simulated as the value of 403 GHz when the Ge component is triangular distribution; the cut-off frequency f_T is 398 GHz when the

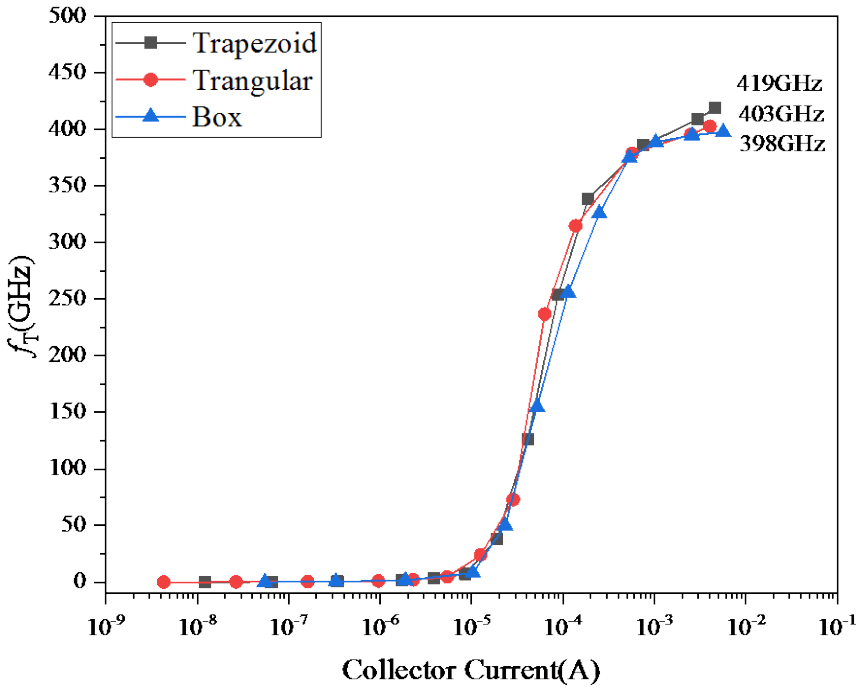

Figure 5. f_T versus I_c curve for Ge component SOI SiGe HBT in different base regions.

Ge component is box distribution. In conclusion, the best choice of Ge components in the base for the improvement of SOI SiGe HBT performance is an exactly trapezoidal distribution.

5. The Effect of Uniaxial Stress on Frequency Characteristics f_T

The simulation of the electrical characteristics of the small-size SOI SiGe HBT uses the ATLAS two-dimensional device simulation module. The main physical models used in the numerical simulation are concentration-dependent mobility model, parallel electric field dependence model, auger recombination model, Shockley-Read-Hall (SRH) recombination model, Band narrowing model, Stress model, energy balance transmission model and Fermi-Dirac statistical model. Newton iterative method and the Gummel iterative method are also used for numerical calculation.

The collector of SOI SiGe HBT also affects the frequency characteristics of the device, the smaller the delay time τ_c in the collector, the greater the cut-off frequency. This paper innovatively introduces the embedded $Si_{1-y}Ge_y$ source drain strain technology in the collector (as shown in **Figure 6**). When a stress is applied to the collector, the electrons velocity vertical passing through the collector region increased due to the existence of compressive stress, so the delay time of the collector region will be further reduced. The f_T curves as a function of the collector for HBT device with stress and without stress are shown in **Figure 7**. The simulation results show that the cut-off frequency f_T of the traditional SOI SiGe HBT (without stress) is 197 GHz, while the improved SOI SiGe HBT (with

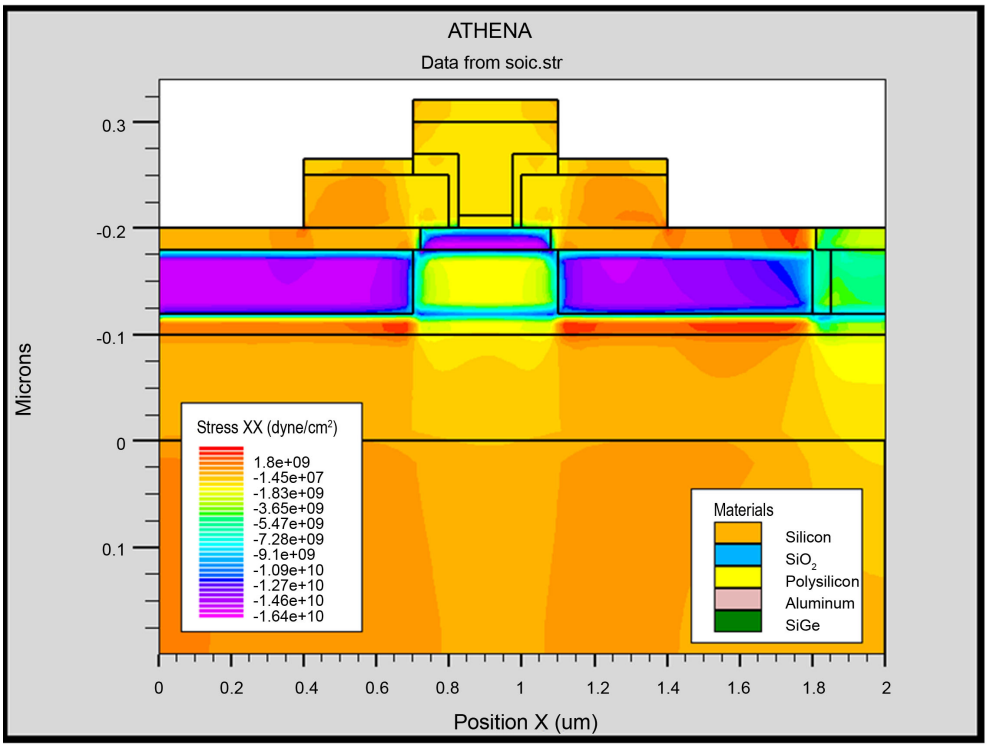

Figure 6. SOI SiGe HBT stress distribution.

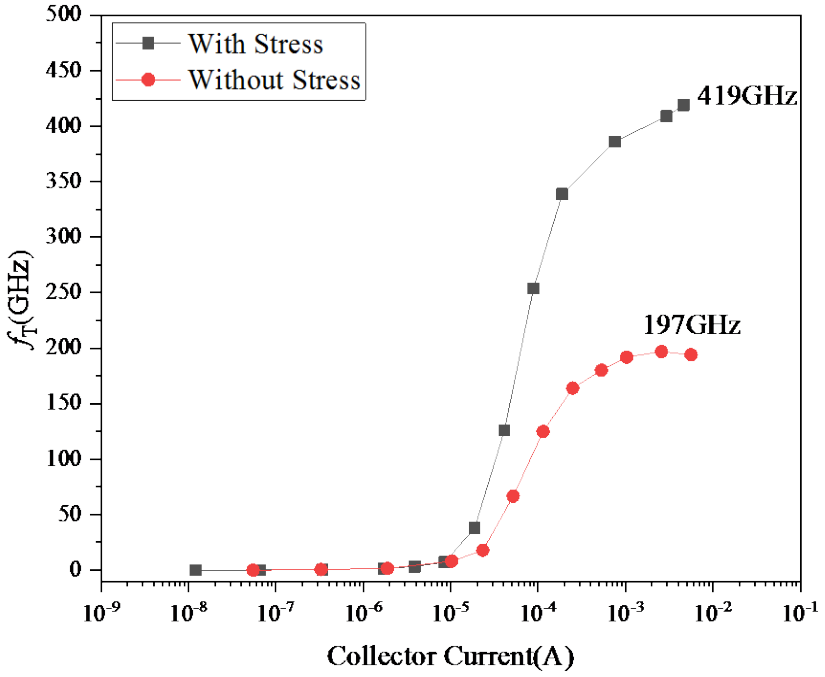

Figure 7. Comparison of cutoff frequency f_T between traditional and proposed SOI SiGe HBT.

stress) is 419 GHz. The cut-off frequency f_T is increased by 52.9%. The improvement of collector optimization frequency is greater than that of base optimization frequency because the base is very thin and the transition time τ_B of the

base is limited.

6. Conclusion

The simulation study of SiGe SOI HBT with strain into the collector. When the base Ge component distribution is a trapezoid, the influence of different base Ge component distribution on the SiGe HBT's characteristics has been simulation and analysis. The maximum value of the current gain β_{max} is 1062, the value of the Early voltage V_A is 186 V, the product of the Early voltage and the current gain is 1.975×10^5 V, and the maximum value of the cut-off frequency f_T is 419 GHz. The cut-off frequency is increased by 52.9% compared with the device structure without stress. The proposed novel SOI SiGe HBT device is compatible with the CMOS technology and has certain theoretical significance and reference value for the circuit design and process integration of commercial terahertz Si/SiGe BiCMOS in the future.

Acknowledgements

This work was financially supported by the National Natural Science Foundation of China (61704147, 61404019).

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

References

[1] Schröter, M., Rosenbaum, T., Chevalier, P., Heinemann, B., Voinigescu, S.P., Preisler, E., *et al.* (2016) SiGe HBT Technology: Future Trends and TCAD-Based Roadmap. *Proceedings of the IEEE*, **105**, 1068-1086. https://doi.org/10.1109/JPROC.2015.2500024

[2] Heinemann, B., Rücker, H., Barth, R., Bärwolf, F., Drews, J., Fischer, G.G., *et al.* (2016) SiGe HBT with fx/fmax of 505 GHz/720 GHz. 2016 *IEEE International Electron Devices Meeting* (*IEDM*), San Francisco, 3-7 December 2016, 3.1.1-3.1.4. https://doi.org/10.1109/IEDM.2016.7838335

[3] Böck, J., Aufinger, K., Boguth, S., Dahl, C., Knapp, H., Liebl, W., *et al.* (2015) SiGe HBT and BiCMOS Process Integration Optimization within the DOTSEVEN Project. 2015 *IEEE Bipolar/BiCMOS Circuits and Technology Meeting—BCTM*, Boston, 26-28 October 2015, 121-124. https://doi.org/10.1109/BCTM.2015.7340549

[4] Chevalier, P., Schröter, M., Bolognesi, C.R., d'Alessandro, V., Alexandrova, M., Böck, J., *et al.* (2017) Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications. *Proceedings of the IEEE*, **105**, 1035-1050. https://doi.org/10.1109/JPROC.2017.2669087

[5] Voinigescu, S.P., Shopov, S., Bateman, J., Farooq, H., Hoffman, J. and Vasilakopoulos, K. (2017) Silicon Millimeter-Wave, Terahertz, and High-Speed Fiber-Optic Device and Benchmark Circuit Scaling through the 2030 ITRS Horizon. *Proceedings of the IEEE*, **105**, 1087-1104. https://doi.org/10.1109/JPROC.2017.2672721

[6] Yuan, J., Cressler, J.D., Krithivasan, R., Thrivikraman, T., Khater, M.H., Ahlgren, D. C., *et al.* (2009) On the Performance Limits of Cryogenically Operated SiGe HBTs

and Its Relation to Scaling for Terahertz Speeds. *IEEE Transactions on Electron Devices*, **56**, 1007-1019. https://doi.org/10.1109/TED.2009.2016017

[7] Misra, P.K. and Qureshi, S. (2014) Epilayer Optimization of NPN SiGe HBT with n+ Buried Layer Compatible with Fully Depleted SOICMOS Technology. *Journal of Semiconductor Technology and Science*, **14**, 274-283. http://dx.doi.org/10.5573/JSTS.2014.14.3.274

[8] Misra, P.K. and Qureshi, S. (2013) A Technique to Improve the Performance of an NPN HBT on Thin-Film SOI. *IEEE Journal of the Electron Devices Society*, **1**, 92-98. https://doi.org/10.1109/JEDS.2013.2253597

[9] Baykan, M.O., Thompson, S.E. and Nishida, T. (2010) Strain Effects on Three-Dimensional, Two-Dimensional, and One-Dimensional Silicon Logic Devices: Predicting the Future of Strained Silicon. *Journal of Applied Physics*, **108**, Article ID: 093716. https://doi.org/10.1063/1.3488635

[10] Canderle, E., Chevalier, P., Avenier, G., Derrier, N., Céli, D. and Gaquière, C. (2013) Impact of BEOL Stress on BiCMOS9MW HBTs. 2013 *IEEE Bipolar/BiCMOS Circuits and Technology Meeting* (*BCTM*), Bordeaux, 30 September-3 October 2013, 223-226. https://doi.org/10.1109/BCTM.2013.6798181

[11] Jin, D., Wang, Z., Guo, Y., Zhang, W., Zhao, X. and Wang, Q. (2015) Design of a Novel Strained-SI HBT with Virtual Substrate for High Current Gain-Breakdown Voltage Product. 2015 *IEEE* 16*th International Conference on Communication Technology* (*ICCT*), Hangzhou, 18-20 October 2015, 357-360. https://doi.org/10.1109/ICCT.2015.7399858

[12] Liu, W., Lin, C., Di, Z., Song, Z. and Chu, P.K. (2006) Investigation of Relaxed SiGe on Insulator and Strained Si. 2006 *International Workshop on Junction Technology*, Shanghai, 15-16 May 2006, 210-213. https://doi.org/10.1109/IWJT.2006.220894

[13] Jin, H.-Y., Zhang, L.-C., Gao, Y.-Z. and Ye, H.-F. (2003) An Equivalent Heterojunction-Like Model for Polysilicon Emitter Bipolar Transistor. *Solid-State Electronics*, **47**, 1719-1727. https://doi.org/10.1016/S0038-1101(03)00153-9

[14] Khanduri, G. and Panwar, B. (2015) A Novel Approach for Justification of Box-Triangular Germanium Profile in SiGe HBTs. *Journal of Semiconductors*, **36**, Article ID: 024002. https://doi.org/10.1088/1674-4926/36/2/024002

[15] Harame, D.L., Comfort, J.H., Cressler, J.D., Crabbe, E., Sun, J.C., Meyerson, B.S. and Tice, T. (1995) Si/SiGe Epitaxial-Base Transistors. I. Materials, Physics, and circuits. *IEEE Transactions on Electron Devices*, **42**, 455-468. https://doi.org/10.1109/16.368039