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New Model for Drain and Gate Current of Single-Electron Transistor at High Temperature

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ABSTRACT

We propose a novel analytical model to describe the drain-source current as well as gate-source of single-electron transistors (SETs) at high temperature. Our model consists on summing the tunnel current and thermionic contribution. This model will be compared with another model.

Keywords: Single-Electron Transistor (SET); Master Equation; Orthodox Theory; Tunnel Current; Thermionic Current; SIMON

1. Introduction

The phenomenal success of semiconductor electronics during the past three decades was based on the scaling down of silicon field effect transistors (MOSFET). The most authoritative industrial forecast, the International Technology Roadmap for Semiconductors (ITRS) [1] predicts that this exponential progress of silicon MOSFETs and integrated circuits will continue at least for the next 15 years ("Moore's Law") [2]. However, prospects to continue the Moore law, a very important device: the single-electron transistor was first suggested in 1985 and first implemented two years later. This device attracted much attention because of their nano feature size and less power consumption. Moreover SETs are suitable for several applications such as memories, multiple-valued logic (MVL)… due to the discrete number of electrons in a coulomb island.

SETs characteristics are very different from those of MOSFETs. In both of them, electrostatic effects are dominant, but, due to the existence of Coulomb blockade; electrons are not so free to move from source to drain, due to of tunnel junctions. The Coulomb blockade effect: that is the electrostatic repulsion experienced by an electron approaching a small negatively charged region, limits the number of electrons in the island. As a result, for given values of gate and drain voltages, only a range of charge is possible for tunneling.

Our day extensive research has been conducted on fabrication, design, and modeling of SET, that has also been an active area. Monte Carlo simulation has been widely used to model SETs. SIMON [3] and MOSES [4] are two most popular SET simulators for circuit analysis and systems containing more than a few SETs but validated in ambient temperature range. Several SET analytical models, each of them based on the orthodox theory, can notably name the models proposed for metallic SETs by the following:

- Uchida *et al.* [5] proposed an analytical SET model for resistively symmetric devices ($R_S = R_D$) and valid for $|V_{DS}| < e/C_\Sigma$, later Inokawa *et al.* [6] extended this model to asymmetric SETs but does not account for the background charges effect.
- Recently a compact analytical model (named MIB) [7] for SET device, which is applicable for $|V_{DS}| < 3e/C_\Sigma$ and wide-range of temperature, and valid for single/multiple gate symmetric/asymmetric device, is taken that the only one direction flow to minimize the number of exponential terms. MIB model can be used for both digital and analog SET circuit design and for both pure SET and hybrid CMOS-SET circuit simulation.

C_Σ represents the total capacitance of the SET-island:

$$C_\Sigma = C_S + C_D + C_{G1} + C_{G2} \qquad (1)$$

C_{G1}, C_{G2}, C_D and C_S represent the capacitances of first gate, second gate (when exists), tunnel drain and tunnel source junctions respectively.

Two conditions ensure that the transport of charges through the metallic island is governed by:

1) Charging the island with an additional charge takes the time $\Delta t = R_T C$, which is the RC-time constant of the quantum dot.

2) The charging energy required to add a single electron with charge e to the quantum dot is: $\Delta E_C = e^2/C_\Sigma$. The system will respect Heisenberg's uncertainty relation:

$\Delta E_C \Delta t > h$, which leads to: $R_T > h/e^2 \approx 26$ kΩ. Where e is electronic charge and h is Planck's constant. This condition is needed to make the charge on the island a well-defined quantity.

3) Another necessary criterion to observe in single-charge-tunneling effects, the charging energy $E_C = e^2/C_\Sigma$, must be much greater than the thermal fluctuations energy $E_{th} = k_B T \approx 25$ meV, to add an electron to the island. Where k_B is Boltzmann's constant and T is the temperature.

2. Model Description

2.1. Tunnel Current Calculation

In this section, we will only consider a system with a double-junction that is made of normal metals for which the free energy will be determined. The energetic considerations are important because, if one knows how to calculate the change in the system's free energy ΔF for a tunneling event, then one can calculate the rate at which this particular process occurs. When the leads and the island are normal metals, and once all of the tunneling rates are known, the tunneling current through the device can be determined. For the case of electron transport through the SET, let us consider the tunneling between two electrodes separated by a barrier. The Fermi energies of the two electrodes are offset from each other by an amount $V_{DS} = eV$.

With some approximations the calculation allows us to obtain the rate from the source state to the drain state According to the orthodox theory [8-10], can also write the tunneling rate in a more general form: the free energy $\Delta F = -eV$, that is:

$$\Gamma(\Delta F) = \frac{\Delta F}{R_T e^2 \left[1 - \exp(-\beta \Delta F)\right]} \tag{2}$$

where $\beta^{-1} = k_B T$ is the thermal energy.

The tunneling rate in the reverse direction is simply obtained by reversing the sign of the bias voltage.

The current in the device is due to the sequential tunneling of electrons through the source and drain junctions simultaneously. The cotunneling phenomenon is ignored.

Assuming no charge accumulation on the island at steady state, one can determine the probability $p(n)$ by requiring the total probability of tunneling into a state to be equal to the total probability of tunneling out of it. The master Equations (8)-(10) to determine $p(n)$ is:

$$\frac{\partial p_n}{\partial t} = \Gamma_{n,n+1} p_{n+1} + \Gamma_{n,n-1} p_{n-1} - \left(\Gamma_{n+1,n} + \Gamma_{n-1,n}\right) p_n \tag{3}$$

where $\Gamma_{n+1,n} = \overrightarrow{\Gamma_S}(n) + \overleftarrow{\Gamma_D}(n)$

$\Gamma_{n+1,n}$ is the tunneling rates from the state (n) to the state (n + 1) and **Figure 1** describes the electron transition between different states of SET and illustrates the concepts of the tunneling rates.

Here we assume that the electron tunneling rate toward the positive potential is much higher than the electron tunneling rate in the opposite direction.

Allows to find the probability $p(n)$, the idea is to consider the location of the translated point inside the stable zone, set of states [$-N$, N] are needed to determine the current depending on the values of V_{DS}, and take advantage of the periodicity of V_{GS}, then we calculate $p(n)$ for n ∈ [$-N$, N]. The approach simply consists in calculating the number N and how much the point is translated along V_{GS} direction:

$$N = 1 + \left\lfloor \frac{|V_{DS}|}{2e/C_\Sigma} \right\rfloor \tag{4}$$

where C is the floor function. If $|V_{DS}| < 3e/C_\Sigma$, the calculated N is then 2 and the current expression is:

$$I_{DS,\text{tunnel}} = e\left\{\begin{aligned} & p_{-1}\overrightarrow{\Gamma_S}(-1) + p_0\left[\overrightarrow{\Gamma_S}(0) - \overleftarrow{\Gamma_S}(0)\right] \\ & + p_1\left[\overrightarrow{\Gamma_S}(1) - \overleftarrow{\Gamma_S}(1)\right] \end{aligned}\right\} \tag{5}$$

To determine p_0 (and then calculate all the probabilities) can be solved subject to the normalization condition:

$$\sum_n p(n) = 1 \tag{6}$$

2.2. Thermionic Contribution

Now we will add the contribution of the thermionic current [11] and the total current between drain and source electrodes; where the source is connected to ground; is given by:

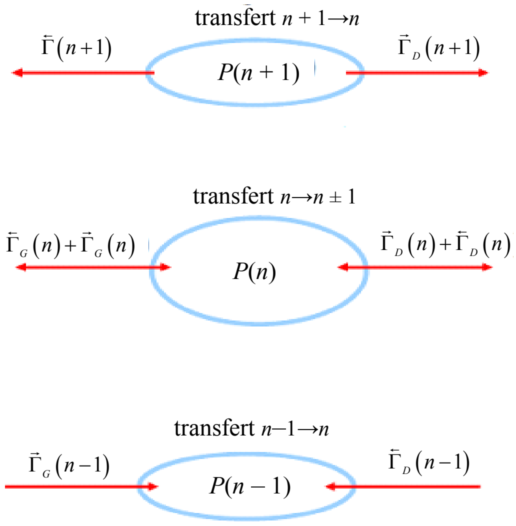


Figure 1. The inflow and outflow electron through the island with suitable concepts of tunneling rates between left electrode (*G*) and right electrode (*D*).

$$I_{DS}(V) = I_{DS,\text{tunnel}}(V) + I_{DS,\text{thermionic}}(V) \tag{7}$$

with:

$$\begin{aligned} I_{DS,\text{thermionic}} &= S \times J_{\text{thermionic}} \\ &= AS\frac{m_{ox}}{m_0}T^2\exp\left[\frac{-e\left(\varphi_0 - \sqrt{\dfrac{eV_{DS}}{4\pi l\varepsilon_0\varepsilon_r}}\right)}{k_BT}\right] \end{aligned} \tag{8}$$

where:

- A: is the Richardson constant;
- k_B: is the Boltzmann's constant;
- h: is the Planck's constant;
- S: is the area of the junction;
- m_0: is the free electron mass;
- m_{ox}: is the mass of the electron in the oxide;
- φ_0: is the height of the potential barrier;
- l: is the thickness of the oxide;
- ε_0: is the vacuum permittivity;
- ε_r: is the relative permittivity of the dielectric.

3. Results and Discussion

3.1. Verification with Dubuc *et al.* Model

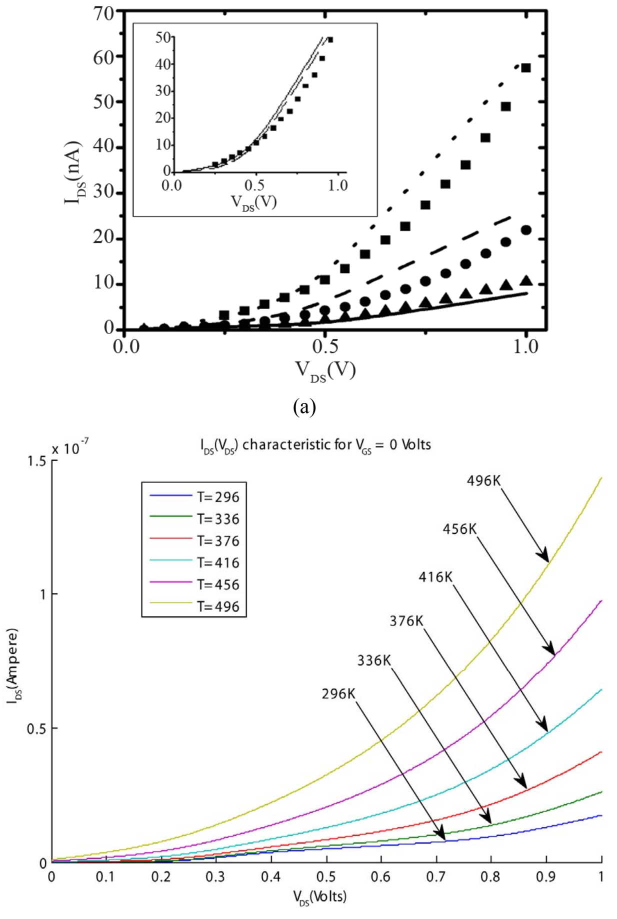
In order to validate our model, the I-V, we have taken as a benchmark, the same conditions and parameters of the SET realized at the University of Sherbrook [12,13], described in **Table 1** such metallic devices which are made with Ti and TiO_X tunnel junctions can run at relatively higher temperature.

From **Table 1** we can deduce that $C_\Sigma = 0.35$ aF, $T_{max} = 530$ K and $-1.37\ \text{V} \le V_{DS} \le 1.37$ V. For $T = 300$ K the charging energy $E_C = e^2/2C_\Sigma \approx 0.45\ \text{eV} > 10\ k_BT$. The comparison was established between our model and the model of Dubuc *et al.* [14]. **Figure 2** shows the evolution of the I_{DS} *vs.* V_{DS} of Dubuc model with our model, the two results are in good agreement with the experiment data with a shifting.

For $V_{DS} \ge 0.6$ V the transport of electron is still by thermionic effect, so the electrons have sufficient energy to blow up the energy barrier was created by the tunnel junction. On the other hand the Coulomb staircase is transformed to an, practically, continuous regime in this field the transfer become by flow and not by packet.

Table 1. Electronic parameters description of the SET, manufactured from titanium and its oxide [12,13].

Description	Value
Junction area	10 nm × 2 nm
Dielectric thickness	8 nm
Ti/TiO_X barrier height	0.35 eV
Effective electron mass in TiO_X	0.40^*m_0
TiO_X dielectric constant	3.5
SET drain capacitance, C_D	0.06 aF
SET source capacitance, C_S	0.06 aF
SET gate capacitance, C_G	0.23 aF
SET drain resistance, R_D	4.5×10^7 Ohms
SET source resistance, R_S	1.5×10^7 Ohms



(a)

(b)

Figure 2. I_{DS}-V_{DS} curve simulated with: (a) The Dubuc model at 296 K (▲), 336 K (●) and 430 K (■). V_{GS} = 0 V. The thermionic contribution (dashed line) to the total drain current model at 433 K (continuous line) is shown in the inset graph and [14]; (b) I_{DS}-V_{DS} verification of our model.

The increase is observed indicating a switch of the dominant transport mechanism. For $V_{DS} \le 0.6$ V the tunneling current is predominant. Since this value, the thermionic emission can be assumed as the dominant transport mechanism, and suppresses tunneling effects. The temperature is one of the de-coherence factors, as it usually tends to reduce the impact of the quantization of the energy. Also note that as the temperature increases, so does the current amplitude.

We have also simulated the V_{GS} vs. I_{DS} curves of single electron transistor with ours model at 336 K for different V_{DS} values **Figure 3**. The result of simulation is shown as **Figure 3**. The Coulomb blockade phenomenon persists at high temperature. The effect of V_{DS} voltage is to modulate the depth of quantum well that is describe, in the

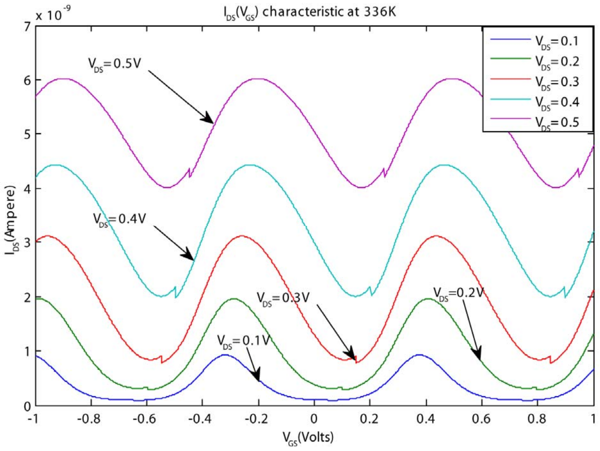


Figure 3. Coulomb oscillations of SET obtained by our model with the parameters in Table 1 at T = 336 K for different V_{DS} voltages.

curve by a non-zero current for V_{GS} = 0 V and the gate starts to lose control over the drain current. Contrariwise, in the Dubuc model, the gate-current was not established.

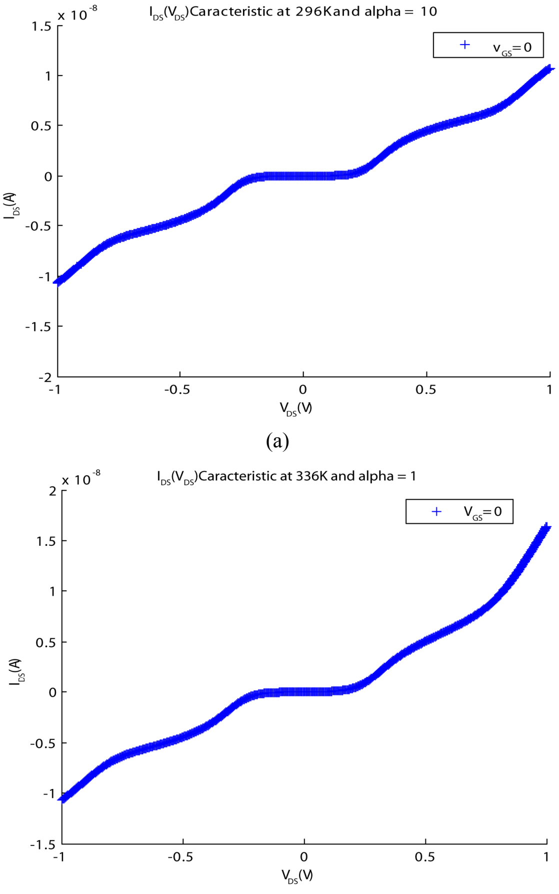
4. Experiment Results

Because of the wave nature of electrons, some of the outgoing electrons are reflected when they reach the drain, which reduces the density of emission current; this may explain the shifting between the theoretical curves and the experiment curves. We can compensate this by introducing a new physical term that introduce acceptable physical effects and associated directly to the structure of the transistor.

But recent models for thermionic emission assume a spatial distribution of the barrier height to take the inhomogeneities of the charges in the interface into account; the barrier height will have a temperature dependence which can be described by an effective potential barrier φ^* [15]. However, the effect of temperature on device-size must also be taken into account; then area S in Equation (9) will defined a newly effective area 1 *i.e.* impact of the dot size dispersion on the thickness. At high temperature dependence on I_{DS} is hypothesized as the reason why thermionic emission was observed only for $T > 300$ K.

Figure 4 reproduces the Coulomb staircase, and shows results for our two empirical values of α (α = 1 and α = 10) for T = 296 K and 336 K.

Now, is clearly, our model gives an accurate result when compared the experiments ones. It is clear that the rates outside the range of validity of model have to be modified for negative bias. Since the model considers only that the two most-probable charging states and the probabilities of taking these states $p(n)$ and $p(n + 1)$ are already know and one direction flow. The difference is more clear in the reverse bias region, ($I_{DS,min}$ for the two curves plotted in **Figure 4** are the same 10 nA) demonstrating the excess current that can be attributed to image force lowering to tunneling currents through the barrier.



(a)

(b)

Figure 4. I_{DS}-V_{DS} empirical model validation (a) for T = 296 K we have chosen α = 10; and (b) for T = 336 K we have chosen α = 1.

5. Conclusion

A physically based analytical SET model within the orthodox theory is developed for to describe the phenomena at high temperature. This new model can reproduce not only the transport property in low and high temperature but also the effects of structure parameters with good agreement for wide gate and drain bias. Modeling and simulation of SET are very important to understand behavior, and characteristic before start fabricating the device.

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