**Wireless Engineering and Technology, 2015, 6, 61-77**
Published Online July 2015 in SciRes. http://www.scirp.org/journal/wet
http://dx.doi.org/10.4236/wet.2015.63007

# Systematic Approaches of UWB Low-Power CMOS LNA with Body Biased Technique

**Meng-Ting Hsu*, Kun-Long Wu, Wen-Chen Chiu**

Microwave Communication and Radio Frequency Integrated Circuit Lab, Department and Institute of Engineering, National Yunlin University of Science and Technology, Taiwan
Email: *hsumt@yuntech.edu.tw, g9813738@yuntech.edu.tw, g9913738@yuntech.edu.tw

Received 3 June 2015; accepted 25 July 2015; published 28 July 2015



## Abstract

**This paper presents research on a low power CMOS UWB LNA based on a cascoded common source and current-reused topology. A systematic approach for the design procedure from narrow band to UWB is developed and discussed in detail. The power reduction can be achieved by using body biased technique and current-reused topology. The optimum width of the major transistor device $M_1$ is determined by the power-constraint noise optimization with inner parasitic capacitance between the gate and source terminal. The derivation of the signal amplification $S_{21}$ by high frequency small signal model is displayed in the paper. The optimum design of the complete circuit was studied in a step by step analysis. The measurements results show that the proposed circuit has superior $S_{11}$, gain, noise figure, and power consumption. From the measured results, $S_{11}$ is lower than −12 dB, $S_{22}$ is lower than −10 dB and forward gain $S_{21}$ has an average value with 12 dB. The noise figure is from 4 to 5.7 dB within the whole band. The total power consumption of the proposed circuit including the output buffer is 4.6 mW with a supply voltage of 1 V. This work is implemented in a standard TSMC 0.18 μm CMOS process technology.**

## Keywords

**Body Bias, Common Source, Low Noise Amplifier (LNA), Low Power, RFCMOS, Ultra-Wideband (UWB)**

## 1. Introduction

Ultra wide band (UWB) systems are a new wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates. Among the possible applications, UWB technology may be used for imaging systems, vehicular and ground-penetrating radars, and communication systems.

*Corresponding author.

**How to cite this paper:** Hsu, M.-T., Wu, K.-L. and Chiu, W.-C. (2015) Systematic Approaches of UWB Low-Power CMOS LNA with Body Biased Technique. *Wireless Engineering and Technology*, **6**, 61-77. http://dx.doi.org/10.4236/wet.2015.63007

In particular, it is envisioned that almost every cable at home or in an office will be replaced with a wireless connection that features hundreds of megabits of data per second [1]. Although the UWB standard (IEEE 802.15.3a [2]) has not been completely defined, most of the proposed applications are allowed to transmit in a band between 3.1 - 10.6 GHz. Two possible approaches have emerged to exploit the allocated spectrum.

One is the Direct-sequence UWB (DS-UWB) proposal. The DS-UWB proposal divides the whole band into two discontinuous bands with the lower band from 3.1 - 4.85 GHz and the upper band from 6.2 - 9.7 GHZ. The other is a proposal for a multiband orthogonal frequency-division multiplexing UWB (MB-OFDM UWB). The latter UWB proposal divides the whole band into 14 sub-bands 528 MHz that are grouped into five main bands [3]. A low noise amplifier (LNA) is a critical building block of the receiver. For the full UWB LNA design goal, there are some factors that are required: sufficient gain and flatness, input/output matching, and most importantly, a low noise figure with a high signal to noise ratio (SNR) to enforce the sensitivity of the receiver. Low chip area and low power consumption are also desired for the LNA. In the past decade, many UWB LNAs with different topologies have been reported. Distributed amplifiers were popular circuits that had wideband characteristics [4]-[7]. Since a distributed amplifier is a little more than cascaded stages, it requires large power consumption to add a common source amplifier [6]. Of course, large chip size with extra inductors is another problem.

The resistive feedback topology with a narrowband inductively degenerated common-source amplifier is an area-saving solution for good input matching in the 3 - 5 GHz UWB band [8]. The feedback resistor $R_f$ may be lowered to reduce additional noise. If the $g_m$ of the transistor is raised, the Miller effect on $R_f$ will also be increased. Therefore, a higher current dissipation and larger MOS area are required [9]-[12]. In recent years, the transformer as reactive feedback has been adopted for implementation of UWB application [13] [14]. Moreover, low power CMOS LNA with transformer multicascode topology has been developed and reported for V-band and Q-band application [15].

Some papers reporting on the common-gate amplifier have been suggested using wideband input matching as a solution by setting the input-transistor transconductance $g_m$ equal to the reciprocal of the source resistance [16]-[21]. For this topology, high value of the transconductance contrasts with low-current dissipation. If the current-reused structure is added with this topology, lower power of the core circuit can be achieved under 5 mW without an output buffer [22]. If the cascade stages are used in the circuit, it needs larger amounts of power for the ultra wideband RF receiver [23]. However, with a common-gate configuration, it is hard to attain a 50 Ω real impedance for input matching and noise performance is also an area that requires improvement.

A common-source amplifier with a source degeneration inductor is one of the best approaches for narrowband application in terms of gain and noise performance [24]. A common rule of this circuit for broadband matching application is obtained by replacing the gate inductance with a LC ladder network [14] [25] [26]. A drawback of this approach for UWB is the large group-delay variation which means that the signal can experience several resonances in the input-matching network. If a series-peaking inductor is used with the gate of the second transistor, then the inductor $L_{g2}$ can reduce the noise figure in the cascode structure with current-reuse topology [27].

The proposed circuit of a common-source amplifier with low power UWB LNA has been demonstrated [28]. Additional analysis and discussion which emphasize the low power UWB are provided. Based on the effect of the body-biased technique and the current reused cascode structure, the low power consumption of our work can achieve lower than 5 mW including the output buffer. The analysis and design approach of the circuit is addressed in Section 2. The design procedure and body biased technique are also discussed in this Section 2. The measurement results are presented in Section 3. The conclusion is given in Section 4.

## 2. Proposed LNA Design Approach

The proposed low power LNA is shown in **Figure 1**. There are two stages including the core circuit of the first stage with common source (CS) amplifier $M_1$ and the buffer of the second stage. The first stage consists of the LC input matching network, body biased technique, and the cascode common source amplifiers $M_1$ and $M_2$ using the current-reused technique for low power design. The T-type LC filter is used for 50 Ω input matching and provides resonant frequency at 3 GHz for the high pass filter function. There are two transistors, $M_1$ and $M_2$ and both share the same drain current in a single path which saves power. The inductors $L_3$ and $L_5$ are used as the RF choke to avoid RF signal through the DC supply. A large value with $L_3$ = 9 nH and $L_5$ = 4 nH, respectively, is required. Inductor $L_4$ is used as the peaking inductor. Capacitor $C_2$ serves as the DC block capacitor and also builds up a RF signal path from transistor $M_1$ to transistor $M_2$. Capacitor $C_3$ serves as the bypass capacitor and

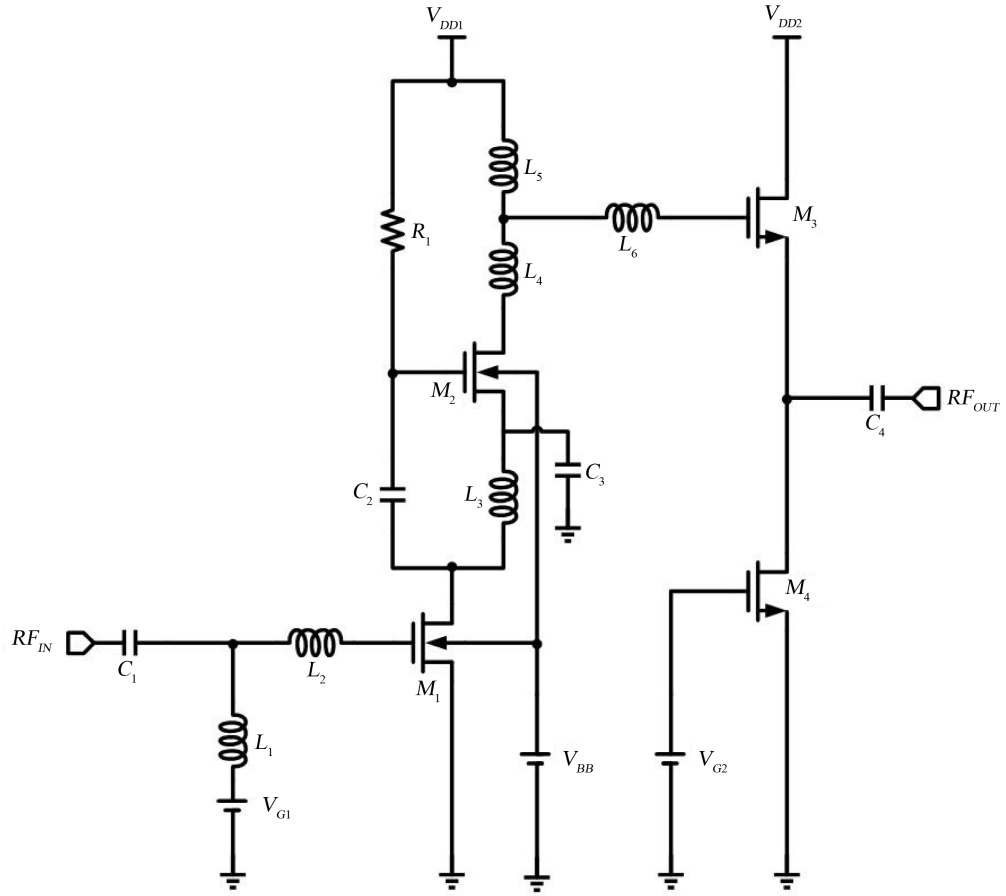



**Figure 1.** Proposed UWB LNA with boday bias technique.

functions to make transistor $M_3$ as the ground state at the source node. The value for $C_2$ and $C_3$ are assumed to be $C_2$ = 2 pF and $C_3$ = 6 pF, respectively [29]. In addition, using the body biased technique, the threshold voltage $V_T$ can be decreased by adjusting body voltage $V_B$ to reduce the power consumption, and enhance the gain performance during the cascode stage. To improve the gain flatness, a couple inductor $L_6$ is used. Finally, the source follower $M_3$ and the current source $M_4$ are used to as the output buffers. From the simulation, the measurements of our proposed circuit including the buffer are 4 mW and 4.6 mW, respectively.

We can develop a LNA design procedure of the common source with source inductor degeneration for narrowband application [30].

From the derivation of the power-constrained noise optimization, there are five steps necessary to complete the LNA design.

1) Determine the width of the optimum device $M_1$ from the equation that follows:

$$W_{optp} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_s Q_{sp}} \tag{1}$$

where $L$ is the length of transistor, $R_S$ is the resistance of source stage, $Q_{SP}$ is the quality factor of input stage and $\omega$ is the center frequency for which the design is made.

2) Bias the device with the amount of current allowed by the power constraint.

3) Select the value of source degenerating inductance to provide the desired input match.

4) Compute the expected noise from the following equation:

$$F_{\min} = 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right) \tag{2}$$

where $\gamma$ is the thermal noise coefficient of transistor and $\alpha$ is the ratio of $g_m$ ($\alpha = g_m/g_{d0}$), $g_{d0}$ is the transconductance at zero bias voltage.

5) Add sufficient inductance in the series with the gate to bring the input loop into resonance at the desired operating frequency.

From the former procedure, we can develop the optimum design for the UWB in a power constraint noise matching condition.

## 2.1. Determination of Transistor $M_1$ and Input Matching

In the narrowband LNA circuit design, the optimum width of transistor $M_1$ can be calculated by Equation (1) under power constraint noise optimization. In the UWB LNA circuit design, if the bias drain current $I_D$ of the MOS device is initially set according to the power consumption requirement, then the noise can be estimated by Equation (2), and transistor $M_1$ also can be determined. For NMOS devices, the drain current at the saturated region can be indicated [31]

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{3}$$

where $\mu_n$ is the mobility of electrons, $C_{ox}W$ is the total capacitance per unit length, $L$ is the effective channel length and $V_{GS} - V_{TH}$ is the overdrive voltage. From Equation (3), if channel length $L$ and the overdrive voltage are kept at the constant, then the drain current is proportional to the capacitance. Since a MOSFET operating in saturation produces a current in response to its gate-source overdrive voltage, the transconductance gm can be expressed as the following:

$$g_m = \mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right) \tag{4}$$

$$= \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{5}$$

$$= \frac{2I_D}{V_{GS} - V_{TH}} \tag{6}$$

From Equation (6), $g_m$ represents the transconductance of the device, for a high $g_m$, a small change in $V_{GS}$ results in a large change in $I_D$. And it can be seen that $g_m$ decreases with the overdrive if $I_D$ is constant. The above descriptions from Equation (1) to Equation (6), the size of transistor $M_1$ is located at some range in the low noise figure from the power constraint. This phenomenon has been reporeted in the following papers [25] [32] [33] [34]. However, these papers did not mention how to determine the size of transistor $M_1$ during the first stage which is an important factor to control the total noise figure of the circuit. Here, we adopted the power constraint noise optimization that accompanies with parasitic $C_{gs}$ of transistor $M_1$ to deal with the dimension of the size. In the circuit design, the multi fingers for layout profile are used for transistor to reduce the gate resistance ($R_g$) and noise figure for good behavior.

It is known that the parasitic capacitance is varied by the device size in the high frequency region. If gate resistance $R_g$ is considered and $C_{gd1} \ll C_{gs1}$ is assumed, then the input impedance $Z_{in}$ can be obtained as the following Equation (7):

$$Z_{in}(s) = \left\{\left[\frac{1}{sCgs_1} + \left(sL_2 + R_{L2} + R_g\right)\right] // \left(sL_1 + R_{L1}\right)\right\} + \frac{1}{sC_1} \tag{7}$$

where $s$ is equal to $j2\pi f$. As described above, if the budget of power consumption is determined, then the noise figure and the range of the $M_1$ device size are also obtained as shown in **Figure 2**.

Based on the power constraint noise matching, the noise figure is raised with drain current being decreased as shown in **Figure 2**. If the noise figure is properly chosen by an average value of 3.5 dB in the whole band, then a transistor size from 75 μm to 150 μm is preferred. If the parasitic capacitance of transistor $M_1$ is viewed as a part of the input for the impedance matching network, then the transistor size can be optimized for input matching in the whole band. **Figure 3** shows the $S_{11}$ of the input impedance matching with different transistor sizes. If

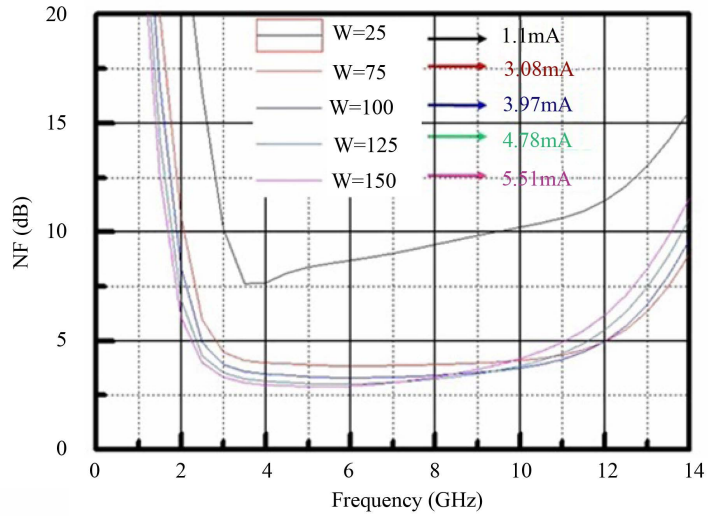



**Figure 2.** Relation between noise figure and drain current of transistor $M_1$.

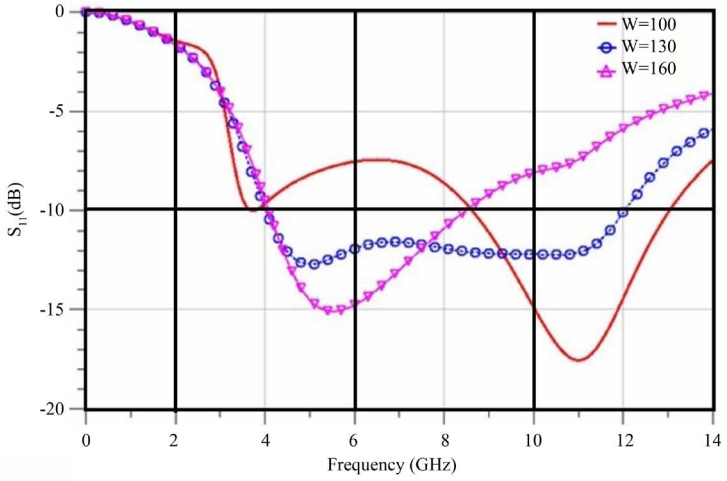



**Figure 3.** Relation coefficient $S_{11}$ with different width.

the width of the device is 100 μm, the locus of $S_{11}$ must be improved in the low band. On the contrary, if the width of the device is larger than 160 μm, then the locus of $S_{11}$ must be improved in the high band. Therefore, the better transistor width is close to 130 μm as shown in **Figure 3** and also is the width chosen for our proposed circui.

## 2.2. Analysis of Source Inductor Degeneration

In the single band or narrow band low noise amplifier, the $S_{11}$ of a common source with inductive degeneration is better than without inductive degeneration. This principle is also fitted to ultra wideband LNA.

The input impedance of the common source inductor $L_s$ included in the circuit can be modified from Equation (7) as follows:

$$Z_{in} = \frac{1}{sC_1} + \left[ \left( R_{L1} + sL_1 \right) // \left( R_g + R_{L2} + \frac{g_{m1}L_s}{C_{gs1}} + sL_2 + sL_s + \frac{1}{sC_{gs1}} \right) \right] \tag{8}$$

Here $g_{m1}$ is the transconductance of transistor $M_1$, then, owing to the contribution of $L_2$, the locus of $S_{11}$ is different from the one in which we omitted $L_s$ in the circuit for input matching. This phenomenon can be seen in **Figure 4**. With or without inductor $L_s$, they both have good $S_{11}$ lower than −10 dB in the whole band. Of course,

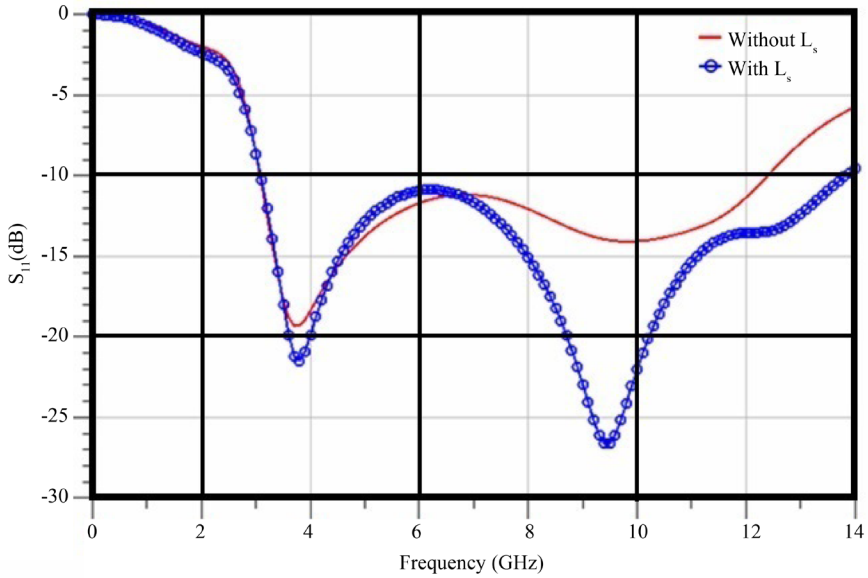



**Figure 4.** The simulation of $S_{11}$ with/without $L_s$.

we must check the effects of gain and the noise figures.

From **Figure 5(a)**, the noise figure with source inductor is 3 - 4.7 dB and without source inductor it is 3 - 4.1 dB, respectively. From **Figure 5(b)**, the forward gain with source inductor is 11.3 - 12.1 dB and without source inductor it is 11.7 - 12.9 dB, respectively. For the proposed circuit, first, the number of inductors must be decreased to decrease chip size. Second, input matching for the whole band must be done. Third, it is necessary to avoid the generation of thermal noise sources with a parasitic resistor.

Finally, whether the source inductor is adopted or not in the circuit for wideband application, there is a little difference of performance from the effect of gain or noise figure. So the source inductor is omitted to save the chip size in our proposed circuit. The detail usage of source inductor is more described in the references [34].

## 2.3. Analysis of Current Reused Stage and Output Buffer

Cascode topology is commonly used to save power and for high gains with a fixed supply voltage application. Recently, the current reused structure has been popularly adopted [27] [32] [35]. The first stage ($C_1$, $C_2$, $L_1$, $L_2$, $M_1$) is designed to resonate at the lower band, and the second stage ($R_1$, $L_4$, $L_5$, $M_2$) is designed to resonate at the higher band.

For RF signal analysis, the forward gain $A_v$ from signal source $V_{sig}$ to output voltage $V_{out}$ can be expressed as the following Equation (9):

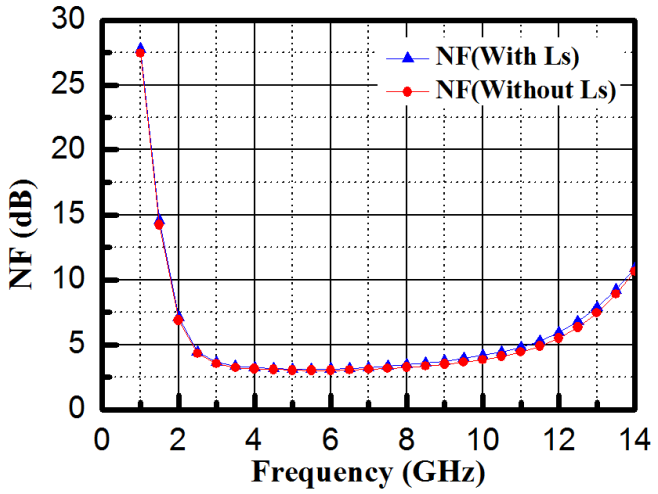
$$A_V = \left|\frac{V_{out}}{V_{sig}}\right| = \left|A_{V1}\right| \cdot \left|A_{V2}\right| \cdot \left|A_{V3}\right| \tag{9}$$

where $A_{V1}$ is the gain of transistor $M_1$, $A_{V2}$ is the gain of transistor $M_2$ and $A_{V3}$ is the gain of transistor $M_3$, respectively. The detailed derivation can be seen in the appendix.

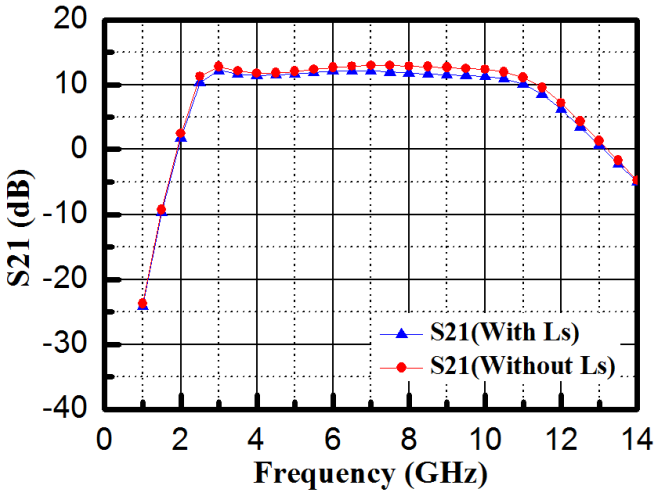
The output resistance $R_{out}$ is approximated with a low frequency model as in Equation (10):

$$R_{out} \approx \frac{1}{g_{m3}} // r_{o3} // r_{o4} \tag{10}$$

When $g_{m3}$ is the transconductance of transistor $M_3$, $r_{o3}$ and $r_{o4}$ are the output resistance of transistors $M_3$ and $M_4$, respectively. For UWB application, the inter stage inductor $L_6$ can resonate with the parasitic capacitor ($C_{gs3}$) of transistor $M_3$ which creates gain peaking at the high frequency band at about 11 GHz. Of course, it also provides the best gain flatness of the proposed circuit. For achieving good gain flatness, the optimization value of $L_6$ and $L_4$ are 2.93 nH and 0.48 nH, respectively.




(a)




(b)

**Figure 5.** (a) NF with/without source inductor (b) $S_{11}$ with/without source inductor.

## 2.4. Analysis of Body Biased Technique

The body biased technique is not used for designing in traditional electronic circuitry with respect to body effect. Recently, self forward body bias and adaptive body bias have been adopted to design circuits that use less power in narrow band considerations [29] [36]-[38]. The wideband and UWB LNA are even reported in the following references [28] [39] [40].

Since the standard CMOS process is without a multiple gate oxide option, the threshold voltage $V_T$ can be calculated by adjusting with $V_{SB}$ as shown in Equation (11):

$$V_T = V_{T0} + \gamma\sqrt{2\varphi_F}\left[\sqrt{\left(1-\frac{V_{BS}}{2\varphi_F}\right)}-1\right] \tag{11}$$

where $V_{SB}$ is the source to body voltage, $V_{T0}$ is the threshold voltage for $V_{SB} = 0$, $\gamma$ is a process dependent parameter, and $\phi_F$ is a semiconductor parameter with a typical value in the range of 0.3 to 0.4 V.

There are two models to understand the body bias technique with analytical expression of the circuit.

1) Body effect analog modeling

First, assuming $V_{BS} \ll \phi_F$ which is the "small signal" approach, and by applying the Taylor series to expression (11), we obtain Equation (12).

$$V_T = V_{T0} + \alpha V_{BS} \Rightarrow \alpha = -\frac{1}{2\sqrt{2\varphi_F}} \tag{12}$$

This Equation (12) highlights a linear relationship between the threshold voltage of the MOS transistor and the potential applied to its bulk.

2) DC mode

The MOS drain current is given by:

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left\{V_{GS} - \left[V_{T0} + \gamma\sqrt{2\varphi_F} \times \left[\sqrt{\left(1 - \frac{V_{BS}}{2\varphi_F}\right) - 1}\right]\right]\right\}^2 \tag{13}$$

For a given $V_{GS}$, $I_D$ current flowing through the MOS transistor depends on bulk-to-source voltage. Hence, transistor biasing can be controlled thanks to the body effect in a DC approach. However, one has to pay attention to the fact that the $V_{SB}$ range is limited. Indeed, if the $V_T$ enhancement induces no significant parasitic constraint on DC characteristics despite the current decrease, the reduction of the threshold voltage can disturb the transistor effect.

Assuming that $V_{SB}$ is lower than roughly speaking 0.7 V, the bulk-to-source PN junction of the NMOS transistor is thus forward biased, producing a leakage current and aborting the transistor functionality. It sets up the limit whose body effect is useful to implement a function thanks to the DC approach. To use body bias NMOSFET, a deep Nwell process is needed. In addition, a deep Nwell process can reduce noise cross-talk through the substrate [39].

This circuit design with body bias technique allows for a reduction in power consumption. A 0.45 V body bias is used to make the transistors in the strong inversion region. It can be seen from **Figure 6(a)** that the transistor with 0.45 V body bias enters the strong inversion region, while the one with 0 V body bias is still in the weak inversion region.

The gain and NF of the LNA are drawn versus $V_{BS}$ as shown in **Figure 6(b)**. The reduction of body bias implies a current decrease thus lessening both gains and noise figures. Therefore, we set $V_{BB}$ = 0.45 V. Practically, the forward body voltage is limited to 0.4 - 0.7 V.

To further investigate the influence of the bias conditions on the noise figure (NF), the simulated values versus gate to source voltage ($V_{GS}$) for the different body bias voltages are demonstrated in **Figure 6(c)**, which provides the design guidelines of the LNA. The cross section region with optimum values are preferred, the voltages of $V_{GS}$ and $V_{BS}$ are as low as good for low power design. Therefore, the voltage $V_G$ is chosen as 0.55 V.

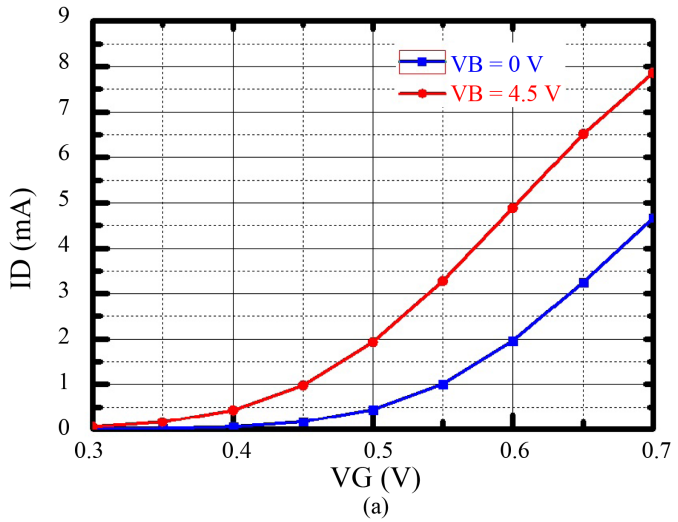
However, how much power can be reduced by the body biased technique is still uncertain. In the circuit, if the parameter gain and $S_{11}$ are in the same condition, then without body bias, the simulation of power consumption in the core circuit is 4.44 mW for 1.2-V supply voltage and 7.23 mW including the output buffer. With body bias, the simulation of power consumption in the core circuit is 3.24 mW and 4.1 mW including the output buffer. The measurement of the power consumption is 3.32 mW and 4.6 mW including the output buffer.

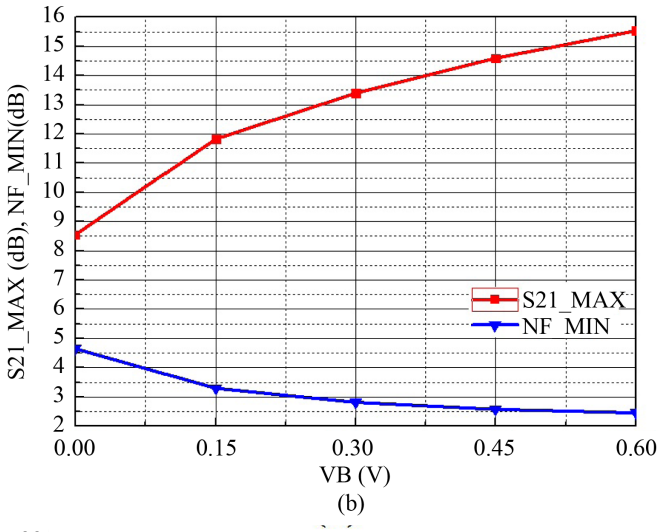
## 3. Measurement

**Figure 7** shows the die photo of the UWB LNA with the body bias technique, which has a chip size of 0.928 $mm^2$. In **Figure 8** it can be seen that the input return loss ($S_{11}$) is lower than −12 dB, but in **Figure 9**, it can be seen that the output return loss ($S_{22}$) is lower than −14 dB from 3.1 GHz to 10.6 GHz, respectively. The power gain, whose peak value is 13 dB, is shown in **Figure 10**. In **Figure 11**, it can be seen that the noise figure is 4 dB - 5.7 dB from 3.1 GHz to 10.6 GHz with a 1 V supply voltage. In **Figure 12**, the third-order input intercept point ($IIP_3$) is −14 dBm. The total power consumption is 4.6 mW at 1 V supply voltage.

To compare the overall performance of our LNAS with previously published ones, a figure of merit (FOM) that takes into account the gain, NF, BW, $IIP_3$, and the DC power consumption of the LNA is defined as [41] [42]

$$\text{FOM} = \frac{\text{Gain}_{\text{MAX(dB)}} \times \text{BW}_{\text{GHz}}}{(F-1) \times P_{D(\text{mW})}} \tag{14}$$



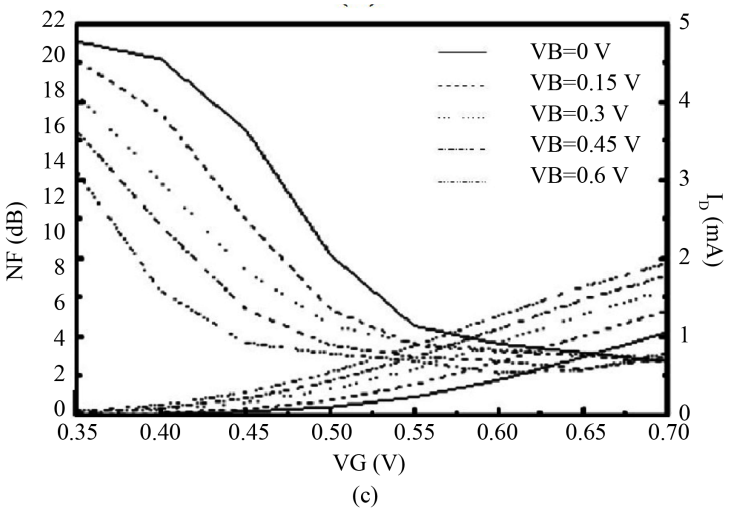




**Figure 6.** (a) Simulation $I_D$ and $V_G$ characteristics of a NMOS transistor with forward body bias; (b) Characteristics of the power gain and noise verse $V_{BS}$; (c) Simulation NF and $I_D$ of the MOSFET with a fixed $V_{DS}$ of 1 V for the different body bias.

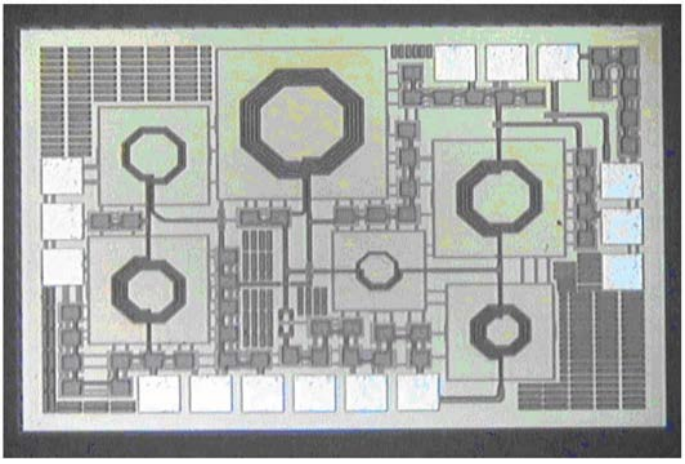


**Figure 7.** Layout of the proposed UWB LNA with body bias technique.

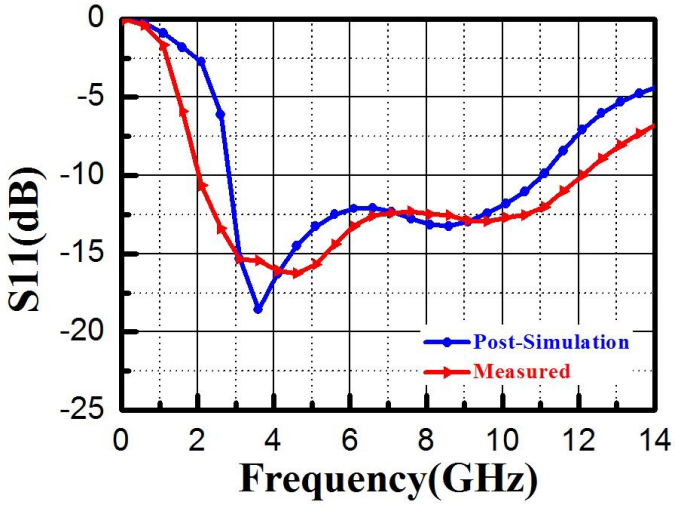



**Figure 8.** Measured and simulated $S_{11}$ of the fabricated LNA.

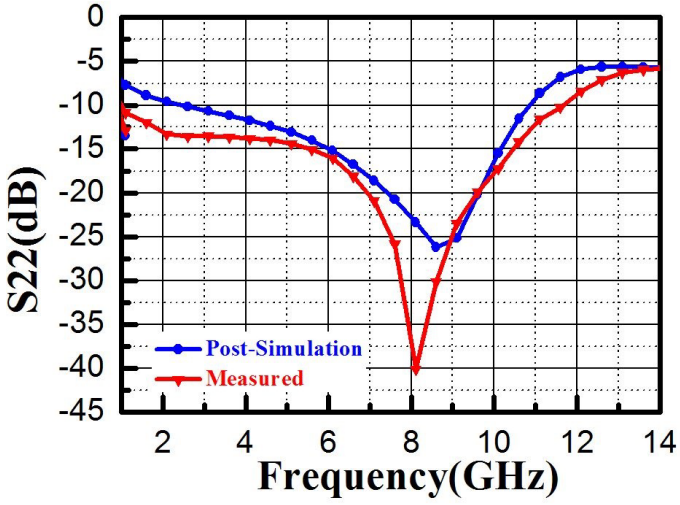



**Figure 9.** Measured and simulated $S_{22}$ of the fabricated LNA.

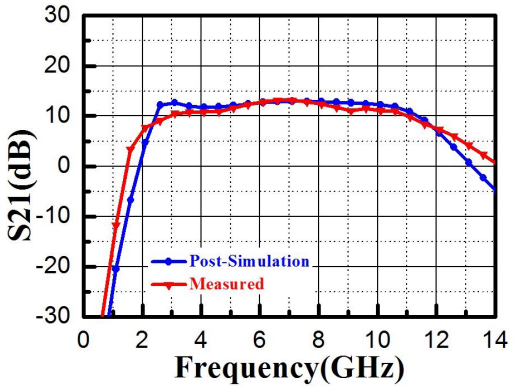



**Figure 10.** Measured and simulated $S_{21}$ of the fabricated LNA.

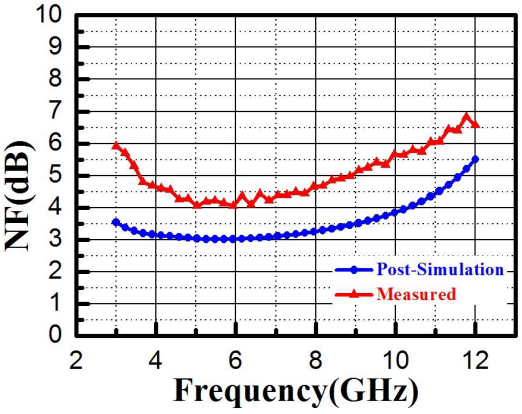



**Figure 11.** Measured and simulated NF of the fabricated LNA.

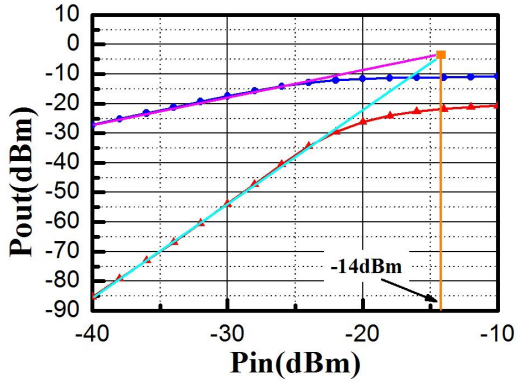



**Figure 12.** Measured $IIP_3$ of the fabricated LNA.

$$\mathrm{FOM}_{\_\mathrm{IIP}_3} = \frac{\mathrm{Gain}_{\mathrm{MAX(dB)}} \times \mathrm{BW}_{\mathrm{GHz}} \times \mathrm{IIP}_{3(\mathrm{mW})}}{(F-1) \times P_{D(\mathrm{mW})}} \tag{15}$$

Where BW is the bandwidth, $P_D$ is the power consumption in milliwatts, the values of gain and noise factor $F$ are their absolute values, $IIP_3$ is indicated as linearity of the amplifier or circuit, and also called the input third-order intercept point.

The comparison of the proposed work with other reported papers are shown in **Table 1**. Our work shows high

**Table 1.** Measured comparison of the proposed 3.1 - 10.6 GHz.

| Reference | [10] '09 | [14] '10 | [19] '07 | [22] '10 | [27] '10 | This work |
|---|---|---|---|---|---|---|
| Technology (CMOS) | 0.18-μm | 0.18-μm | 0.18-μm | 0.18-μm | 0.18-μm (LNA2) | 0.18-μm |
| Frequency (GHz) | 1 - 10 | 3.1 - 10.6 | 1.2 - 11.9 | 3.1 - 10.6 | 3.1 - 10.6 | 3.1 - 10.6 |
| $S_{11}$ (dB) | <−8 | <−11 | N/A | <−13.5 | <−8.6 | <−12 |
| $S_{22}$ (dB) | <−10.8 | N/A | N/A | <−10.1 | <−10 | <−14 |
| $S_{21MAX}$ (dB) | 10.5 | 11/14 | 10.6 | 12 | 12.26 | 13 |
| $NF_{min}$ (dB) | 4.2 | 5.1/4.5 | 3.4 | 5.27 | 3.84 | 4 |
| $IIP_3$ (dBm) | 1 | −12 | −6.2 | −2.23 | −11 | −14 |
| $P_{DC\_CORE}$ (mW) | 12.65 | 9/21 | 20 | 4.5 | 10.34 | 3.32 |
| Area ($mm^2$) | 0.69 | 0.46 | 0.59 | 1.03 | 0.536 | 0.928 |
| FOM (only core LNA) | 4.58 | 4.09/6.41 | 4.77 | 8.44 | 6.26 | 12.01 |
| $FOM_{\_IIP3}$ (only core LNA) | 5.77 | 0.258/0.403 | 1.14 | 5.05 | 0.495 | 0.773 |

performance of gain and low power dissipation.

In general case of low noise amplifier, most of the circuit design did not consider the linearity characterization. The linearity has a serious effect on the power amplifier. Therefore, we can show that our performance of FOM is better than others, and $FOM_{\_IIP3}$ is fairly good but still not the optimal choice.

## 4. Conclusion

In this paper, a UWB low noise amplifier with body bias technique has been presented. The proposed body bias technique is employed to achieve low power consumption. The T-type matching network used for input matching to achieve gain flatness and frequency bandwidth. The power consumption is as low as 4.6 mW with a 1 V supply voltage. From 3.1 to 10.6 GHz, the maximum power gain is 13 dB and the minimum noise figure is 4 dB.

## Acknowledgements

This project was supported by the National Science Council, (NSC100-221-E-224-072), Taiwan, ROC. The authors wish to thank the Chip Implementation Center (CIC) and TSMC for supporting the CMOS process and further fabrication.

## References

[1] Siwiak, K. and McKeown, D. (2004) Ultra-Wideband Radio Technology. Wiley, Hoboken.

[2] Aiello, G.R. and Rogerson, G.D. (2003) Ultra-Wideband Wireless Systems. *IEEE Microwave Magazine*, **4**, 36-47. http://dx.doi.org/10.1109/MMW.2003.1201597

[3] Lu, Y., Yeo, K.S., Cabuk, A., Ado, M. and Lu, Z. (2006) A Novel CMOS Low-Noise Amplifier Design for 3.1 to 10.6-GHz Ultra-Wide-Band Wireless Receivers. *IEEE Transactions on Circuits and Systems I*: *Regular Papers*, **53**, 1683-1692.

[4] Liu, R.-C., Lin, C.-S., Deng, K.-L. and Wang, H. (2005) A 0.5-14 GHz 10.6 dB CMOS Cascade Distributed Amplifier. 2003 *Symposium on VLSI Circuits*, *Digest of Technical Papers*, Kyoto, 12-14 June 2003, 78-81.

[5] Zhang, F. and Kinget, P.R. (2006) Low-Power Programmable Gain CMOS Distributed LNA. *IEEE Journal of Solid-State Circuits*, **41**, 1333-1343. http://dx.doi.org/10.1109/JSSC.2006.874283

[6] Yu, Y.H., Chen, Y.-J.E. and Heo, D. (2007) A 0.6-V Low Power UWB CMOS LNA. *IEEE Microwave and Wireless Components Letters*, **17**, 229-231. http://dx.doi.org/10.1109/LMWC.2006.890502

[7] Heydari, P. (2007) Design and Analysis of a Performance-Optimized CMOS UWB Distributed LNA. *IEEE Journal of Solid-State Circuits*, **42**, 1892-1905. http://dx.doi.org/10.1109/JSSC.2007.903046

[8] Kim, C.-W., Kaang, M.S., Anh, P.T., Kim, H.-T. and Lee, S.-G. (2005) An Ultra-Wideband CMOS Low Noise Amplifier for 3-5-GHz UWB System. *IEEE Journal of Solid-State Circuits*, **40**, 554-547.

[9] Chen, H.K., Chiang, D.C., Juang, Y.Z. and Lu, S.S. (2007) A Compact Wideband CMOS Low-Noise Amplifier Using

Shunt Resistive-Feedback and Series Inductive-Peaking Techniques. *IEEE Microwave and Wireless Components Letters*, **17**, 616-618. http://dx.doi.org/10.1109/LMWC.2007.901797

[10] Hsu, M.-T. and Hsu, S.-Y. (2009) A Low Power CMOS LNA for 1 - 10 GHz Application. *IEEE Asia-Pacific Microwave Conference*, 2009. *APMC* 2009, 1132-1135.

[11] Hsu, M.-T. and Liu, T.-S. (2010) Using Inverter Structure for 2-6GHz Low Power High Gain Low Noise Amplifier. *Proceedings of the IEEE Asia-Pacific Microwave Conference*, Yokohama, 7-10 December 2010, 346-349.

[12] Hsu, M.-T. and Lin, Y.-H. (2011) A Low Power High Gain CMOS LNA for UWB Receivers. *Proceedings of the IEEE Asia-Pacific Microwave Conference*, Melbourne, 5-8 December, 259-262.

[13] Reiha, M.T. and Long, J.R. (2007) A 1.2 V Reactive-Feedback 3.1-10.6 GHz Low-Noise Amplifier in 0.13 µm CMOS. *IEEE Journal of Solid-State Circuits*, **42**, 1023-1033. http://dx.doi.org/10.1109/JSSC.2007.894329

[14] Fu, C.T., Kuo, C.N. and Taylor, S.S. (2010) Low-Noise Amplifier Design with Dual Reactive Feedback for Broadband Simultaneous Noise and Impedance Matching. *IEEE Transactions on Microwave Theory and Techniques*, **58**, 795-806. http://dx.doi.org/10.1109/TMTT.2010.2041570

[15] Yeh, H.C., Liao, Z.Y. and Wang, H. (2011) Analysis and Design of Millimeter-Wave Low-Power CMOS LNA with Transformer-Multicascode Topology. *IEEE Transactions on Microwave Theory and Techniques*, **59**, 3441-3454.

[16] Pepe, D. and Zito, D. (2009) 22.7-dB Gain-19.7-dB ICP1dB UWB CMOS LNA. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, **56**, 689-693.

[17] Park, B., Choi, S. and Hong, S. (2010) A Low-Noise Amplifier with Tunable Interference Rejection for 3.1 to 10.6-GHz UWB Systems. *IEEE Microwave and Wireless Components Letters*, **20**, 40-42. http://dx.doi.org/10.1109/LMWC.2009.2035963

[18] Razavi, B. (2005) A UWB CMOS Transceiver. *IEEE Journal of Solid-State Circuits*, **40**, 2555-2562. http://dx.doi.org/10.1109/JSSC.2005.857430

[19] Liao, C.F. and Liu, S.I. (2007) A Broadband Noise-Canceling CMOS LNA for 3.1-10.6-GHz UWB Receivers. *IEEE Journal of Solid-State Circuits*, **42**, 329-339. http://dx.doi.org/10.1109/JSSC.2006.889356

[20] Wu, C.Y., Lo, Y.K. and Chen, M.C. (2009) A 3-10 GHz CMOS UWB Low-Noise Amplifier with ESD Protection Circuits. *IEEE Microwave and Wireless Components Letters*, **19**, 737-739. http://dx.doi.org/10.1109/LMWC.2009.2032022

[21] Chen, K.H., Lu, J.H., Chen, B.J. and Liu, S.I. (2007) An Ultra-Wide-Band 0.4-10-GHz LNA in 0.18-$\mu$m CMOS. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, **54**, 217-221.

[22] Weng, R.M., Liu, C.Y. and Lin, P.C. (2010) A Low-Power Full-Band Low-Noise Amplifier for Ultra-Wideband Receivers. *IEEE Transactions on Microwave Theory and Techniques*, **58**, 2077-2083.

[23] Hasan, S.M.R. (2010) Analysis and Design of a Multistage CMOS Bandpass Low-Noise Preamplifier for Ultrawideband RF Receiver. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **18**, 638-651.

[24] Shaeffer, D.K. and Lee, T.H. (1997) A 1.5-V 1.5-GHz CMOS Low Noise Amplifier. *IEEE Journal of Solid-State Circuits*, **32**, 745-759. http://dx.doi.org/10.1109/4.568846

[25] Bevilacqus, A. and Niknejad, A.M. (2004) An Ultrawideband CMOS Low-Noise Amplifier for 3.1-10.6-GHz Wireless Receivers. *IEEE Journal of Solid-State Circuits*, **39**, 2259-2268. http://dx.doi.org/10.1109/JSSC.2004.836338

[26] Hsu, M.-T. and Li, K.-J. (2007) An Ultrawideband CMOS Low Noise Amplifier for 3.1-10.6GHz Wireless Communication. *Proceedings of the* 2007 *IEEE International Conference on Ultra-Wideband*, Singapore, 24-26 September 2007, 457-460.

[27] Lin, Y.S., Chen, C.Z., Tang, H.Y., Chen, C.C., Lee, J.H., Huang, G.W. and Lu, S.S. (2010) Analysis and Design of a CMOS UWB LNA with Dual-RLC-Branch Wideband Input Matching Network. *IEEE Transactions on Microwave Theory and Techniques*, **58**, 287-296.

[28] Hsu, M.T. and Wu, K.L. (2011) Design of UWB Low Power Low Noise Amplifier with Body Bias Technique. *Proceedings of the* 2011 *Asia-Pacific Microwave Conference*, Melbourne, 5-8 December 2011, 227-230.

[29] Chien, J. and Lu, L. (2001) 40-Gb/s High-Gain Distributed Amplifiers with Casecaded Gain Stages in 0.18-µm CMOS. *IEEE Journal of Solid-State Circuits*, **42**, 2715-2725.

[30] Shaeffer, D. and Lee, T. (1997) A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier. *IEEE Journal of Solid-State Circuits*, **32**, 745-759. http://dx.doi.org/10.1109/4.568846

[31] Lee, T.H. (2003) The Design of CMOS Radio-Frequency Integrated Circuits. Second Edition, Cambridge University Press, Cambridge.

[32] Lin, Y.J., Hsu, S.S.H., Jin, J.D. and Chan, C.Y. (2007) A 3.1 - 10.6 GHz Ultra-Wideband CMOS Low Noise Amplifier with Current-Reuse Technique. *IEEE Microwave and Wireless Components Letters*, **17**, 232-234.

http://dx.doi.org/10.1109/LMWC.2006.890503

[33] Sapone, G. and Palmisano, G. (2011) A 3-10-GHz Low-Power CMOS Low-Noise Amplifier for Ultra-Wideband Communication. *IEEE Transactions on Microwave Theory and Techniques*, **59**, 678-686.

[34] Mou, S.X., Ma, J.-G., Seng, Y.K. and Anh, D.M. (2005) A Modified Architecture Used Input Matching in CMOS Low Noise Amplifier. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, **52**, 784-788.

[35] Huang, Z.Y., Huang, C.C., Hung, Y.T. and Chen, M.P. (2008) A CMOS Current Reused Low-Noise Amplifier for Ultra-Wideband Wireless Receiver. *Proceedings of the International Conference on Microwave and Millmeter Wave Technology*, Nanjing, 21-24 April 2008, 1499-1502.

[36] Jean-Baptiste, B., Thierry, T. and Herve, L. (2004) Body Effect Principle Applied to RF CMOS Circuits. *Proceedings of the* 16*th International Conference on Microelectronics*, Tunis, 6-8 December 2004, 114-117.

[37] Wu, D., Huang, R., Wong, W. and Wang, Y. (2007) A 0.4V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application. *IEEE Microwave and Wireless Components Letters*, **17**, 543-545. http://dx.doi.org/10.1109/LMWC.2007.899323

[38] Liu, Y. and Yuan, J.S. (2011) CMOS RF Low-Noise Amplifier Design for Variability and Reliability. *IEEE Transactions on Device and Materials Reliability*, **11**, 450-457.

[39] Li, C.M., Li, M.T., He, K.C. and Tarng, J.H. (2010) A Low-Power Self-Forward-Body-Bias CMOS LNA for 3-6.5 GHz UWB Receivers. *IEEE Microwave and Wireless Components Letters*, **20**, 100-102. http://dx.doi.org/10.1109/LMWC.2009.2038526

[40] Chang, J.-F. and Lin, Y.-S. (2011) 0.99 mW 3-10 GHz Common-Gate CMOS UWB LNA Using T-Match Input Network and Self-Body-Bias Technique. *Electronics Letters*, **47**, 658-659.

[41] Gramegna, G. and Erratico, G. (2001) A Sub-1-dB NF ± 2.3-kV ESD-Protected 900-MHz COS LNA. *IEEE Journal of Solid-State Circuit*, **36**, 1010-1017.

[42] Chen, M.Q. and Lin, J.S. (2009) A 0.1-20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm Digital CMOS. *IEEE Microwave and Wireless Components Letters*, **19**, 323-352.

## Appendix

This section is the calculation of gain. **Figure APP1** shows the small signal high frequency model of the complete circuit. The overall gain of the small signal analysis can be expressed by Equation (1):

$$|A_v| = \left|\frac{V_{out}}{V_{sig}}\right| = A_{v1} \cdot A_{v2} \cdot A_{v3} \tag{1}$$

where $V_{out}$ is the output voltage, $V_{Sig}$ is the signal source voltage, $A_{v1}$ is the gain of transistor $M_1$, $A_{v2}$ is the gain of transistor $M_2$ and $A_{v3}$ is the gain of transistor $M_3$.

The gain of the transistor can be expressed by Equations (2)-(4):

$$A_{v1} = \frac{V_{d1}}{V_{gs1}} \cdot \frac{V_{gs1}}{V_{g1}} \cdot \frac{V_{g1}}{V_{sig}} \tag{2}$$

where $V_{d1}$ is the voltage of transistor $M_1$ drain terminal, $V_{gs1}$ is the voltage on $C_{gs1}$, $V_{g1}$ is the voltage of transistor $M_1$ gate terminal.

$$A_{v2} = \frac{V_L}{V_{d2}} \cdot \frac{V_{d2}}{V_{gd2}} \cdot \frac{V_{gs2}}{V_{d1}} \tag{3}$$

where $V_L$ is the output voltage of transistor $M_2$, $V_{d2}$ is the voltage of $M_2$ drain terminal, $V_{gs2}$ is the voltage on $C_{gs2}$.

$$A_{v3} = \frac{V_{out}}{V_{s3}} \cdot \frac{V_{s3}}{V_{g3}} \cdot \frac{V_{g3}}{V_L} \tag{4}$$

where $V_{s3}$ is the voltage of transistor $M_3$ source terminal, $V_{g3}$ is the voltage of $M_3$ gate terminal.

We can calculate each ratio of the previous description from Equations (2) to (4) by the backward direction. Therefore, we can obtain the following equation from (5) to (12).

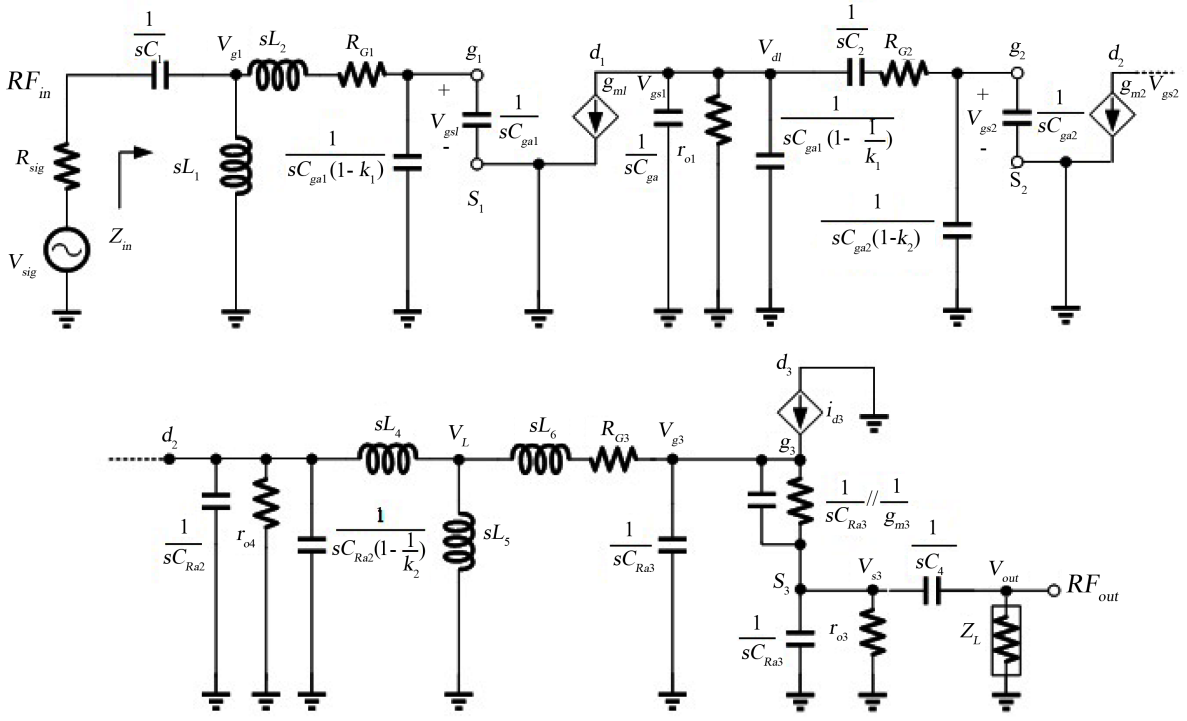



**Figure APP1.** Small signal model.

$$\left|\frac{v_{out}}{v_{s3}}\right| = \left|\frac{Z_L}{\frac{1}{sC_4} + Z_L}\right| \tag{5}$$

$$\left|\frac{v_{s3}}{v_{g3}}\right| = \left|\frac{\frac{1}{sC_{ds3}} // r_{o3} // \left(\frac{1}{sC_4} + Z_L\right)}{\left(\frac{1}{sC_{gs3}} // \frac{1}{g_{m3}}\right) + \left(\frac{1}{sC_{ds3}} // r_{o3} // \left(\frac{1}{sC_4} + Z_L\right)\right)}\right| \tag{6}$$

$$\left|\frac{v_{g3}}{v_L}\right| = \left|\frac{\left\{\frac{1}{sC_{gd3}} // \left[\left(\frac{1}{sC_{gs3}} // \frac{1}{g_{m3}}\right) + \left(\frac{1}{sC_{ds3}} // r_{o3} // \left(\frac{1}{sC_4} + Z_L\right)\right)\right]\right\}}{\left(sL_6 + R_{G3}\right) + \left\{\frac{1}{sC_{gd3}} // \left[\left(\frac{1}{sC_{gs3}} // \frac{1}{g_{m3}}\right) + \left(\frac{1}{sC_{ds3}} // r_{o3} // \left(\frac{1}{sC_4} + Z_L\right)\right)\right]\right\}}\right| \tag{7}$$

$$\left|\frac{v_L}{v_{d2}}\right| = \frac{sL_5 // \left\{\frac{1}{sC_{gd3}} // \left[\left(\frac{1}{sC_{gs3}} // \frac{1}{g_{m3}}\right) + \left(\frac{1}{sC_{ds3}} // r_{o3} // \left(\frac{1}{sC_4} + Z_L\right)\right)\right]\right\}}{sL_4 + \left\{sL_5 // \left\{\frac{1}{sC_{gd3}} // \left[\left(\frac{1}{sC_{gs3}} // \frac{1}{g_{m3}}\right) + \left(\frac{1}{sC_{ds3}} // r_{o3} // \left(\frac{1}{sC_4} + Z_L\right)\right)\right]\right\}\right\}} \tag{8}$$

$$\left|\frac{v_{d2}}{v_{gs2}}\right| = \left|-g_{m2} \cdot \left[\frac{1}{sC_{ds2}} // r_{o2} // \frac{1}{sC_{gd2}\left(1 - \frac{1}{k_2}\right)}\right]\right| \tag{9}$$

$$\left|\frac{v_{gs2}}{v_{d1}}\right| = \left|\frac{\frac{1}{sC_{gd2}\left(1-k_2\right)} // \frac{1}{sC_{gs2}}}{\left(\frac{1}{sC_2} + R_{G2}\right) + \left(\frac{1}{sC_{gd2}\left(1-k_2\right)} // \frac{1}{sC_{gs2}}\right)}\right| \tag{10}$$

$$\left|\frac{v_{d1}}{v_{gs1}}\right| = \left|-g_{m1} \cdot \left[\frac{1}{sC_{ds1}} // r_{o1} // \frac{1}{sC_{gd1}\left(1 - \frac{1}{k_1}\right)}\right]\right| \tag{11}$$

$$\left|\frac{v_{gs1}}{v_{g1}}\right| = \left|\frac{\frac{1}{sC_{gd1}\left(1-k_1\right)} // \frac{1}{sC_{gs1}}}{\left(sL_2 + R_{G1}\right) + \left(\frac{1}{sC_{gd1}\left(1-k_1\right)} // \frac{1}{sC_{gs1}}\right)}\right| \tag{12}$$

In the circuit, analysis of the high frequency models always meets the Miller's theorem. The ratio of drain to gate node with transistor $M_1$ is by $K_1 = \frac{V_{d1}}{V_{gs2}}$. Transistor $M_2$ is also simply expressed as $K_2 = \frac{V_{d2}}{V_{gs2}}$. Therefore, $K_1$ and $K_2$ can be obtained in equations (13) and (14), respectively. Finally, we can get the total overall gain of the complete circuit in Equation (1).

$$k_1 = -g_{m1} \cdot \left[ \frac{1}{sC_{ds1}} // r_{o1} // \frac{1}{sC_{gd1}\left(1 - \frac{1}{k_1}\right)} \right] \tag{13}$$

$$k_2 = -g_{m2} \cdot \left[ \frac{1}{sC_{ds2}} // r_{o2} // \frac{1}{sC_{gd2}\left(1 - \frac{1}{k_2}\right)} \right] \tag{14}$$