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A Novel Device for Real-Time Monitoring of High Frequency Phenomena in CENELEC PLC Band

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ABSTRACT

This paper proposes the design and development of a novel, portable and low-cost intelligent electronic device (IED) for real-time monitoring of high frequency phenomena in CENELEC PLC band. A high speed floating-point digital signal processor (DSP) along with 4 MSPS analog-to-digital converter (ADC) is used to develop the intelligent electronic device. An optimized algorithm to process the analog signal in real-time and to extract the meaningful result using signal processing techniques has been implemented on the device. A laboratory environment has setup with all the necessary equipment including the development of the load model to evaluate the performance of the IED. Smart meter and concentrator is also connected to the low voltage (LV) network to monitor the PLC communication using the IED. The device has been tested in the laboratory and it has produced very promising results for time domain as well as frequency domain analysis. Those results imply that the IED is fully capable of monitoring high frequency disturbances in CENELEC PLC band.

Keywords: Power Line Communication (PLC); Digital Signal Processor (DSP); Analog-to-Digital Converter (ADC); Fast Fourier Transform (FFT); High Frequency (HF) Interference

1. Introduction

Recent technological developments have enabled the evolution of devices that uses power line communication (PLC) to send and receive control signals with some degree of reliability. The primary purpose of power line is to carry power not data which means reliable communication over power lines are difficult due to noise created by loads and devices connected to the PLC network. All power electronic devices generate and emit unwanted electrical signals (EMI noise) that can lead to a performance degradation of PLC network. They generate high frequency conducted and radiated EMI noise and draw distorted line currents due to the sharp edges of the switching waveform with high du/dt. The most common high frequency noise sources are compact fluorescent lamps (CFL), switched power supplies, frequency converters and AC motors that can cause significant amount of reduction in signal-to-noise ratio (SNR) in PLC network [1]. For Western Europe, the regulation concerning communications over low voltage network are described in CENELEC standard EN 50065-1 entitled "Signalling on low-voltage electrical installation in the frequency range 3 kHz to 148.5 kHz". The allowed frequency range *i.e.* 3 to 148.5 kHz is further divided into five sub-bands. The use of frequency band 3 kHz up to 95 kHz is restricted to electricity suppliers and their licensees [2]. The object of the standard is to limit interference caused by signal transmission equipment to sensitive electronic equipment.

The frequency range in the "traditional" harmonic range up to 2 to 3 kHz has been under investigation for several years and large amount of knowledge has been gathered through the years on this issue. However, little or no attention has been paid to the frequency range above the low-frequency harmonic range, or at least between 2 to 150 kHz. This is probably due to the apparent absence of well documented cases of interference found within this frequency range [3]. Another more fundamental reason is the lack of appropriate measuring equipment to record and analyze high frequency phenomenon in PLC network. Conventional monitoring equipment such as, oscilloscope, network analyzer and spectrum analyzer are not optimized for PLC application because they cannot do any post-processing on the measured data which is necessary to monitor the behavior of PLC network. Some previous work carried out on this topic have been presented in [4,5] but they are currently unavailable and work presented in [6] has a limited functionality for a specific platform. One main reason for concern is the possible interference of high frequency distortion with power line communication

e.g., automatic meter reading (AMR). The frequency range used for PLC *i.e.* 3 to 95 kHz is the same range that is often used for switching in switched mode power supplies, high frequency (HF) ballasts, etc. It is a considerable issue for the successful and efficient operation of an AMR. Therefore, long term measurements and real-time analysis of high frequency interference to monitor the power quality of the PLC network has become more essential than ever before. This paper discusses the development of a novel and low-cost intelligent electronic device (IED) for continuous monitoring of power quality and high frequency phenomena in PLC network.

The rest of the paper is organized as follows. Section 2 briefly explains the hardware architecture of the IED. Section 3 discusses about the prototype development of the IED. Section 4 describes the design flow and efficient signal processing algorithm implementation on a low-cost digital signal processor (DSP) to meet the real-time challenges. Section 5 talks about the detailed laboratory setup to test the PLC and other high frequency signals with the IED. The experimental results obtained by IED are discussed in Section 6. Finally, the paper is summarized in Section 7.

2. Hardware Architecture

The hardware architecture of this novel and low-cost IED is based on the development idea proposed in [7]. **Figure 1** shows the modified block diagram of the architecture. The hardware architecture includes signal conditioning, data acquisition and DSP block. Analog signal coming from the LV network needs signal conditioning before an acquisition unit can reliably and accurately acquire the signal. The signal conditioning block includes steps like signal decoupling from the LV network, attenuation, filtering and amplification. Data acquisition block is equipped with ADS7881, a 12-bit analog-to-digital converter to sample the analog signal. Afterwards, a high speed floating-point DSP C6713 with an operating frequency of 225 MHz is used to apply signal processing algorithms to mathematically manipulate the digital data.

A high pass filter and voltage divider circuit as shown in **Figure 2** has been developed as a front-end module to couple with LV network to attenuate the voltage signal to ±2.5 volt. It is the common input voltage range for data acquisition unit.

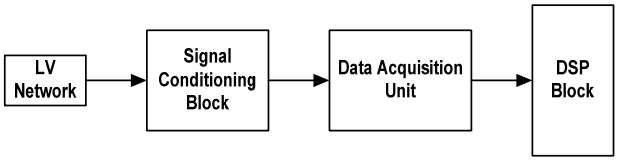

Figure 1. Development approach of the IED.

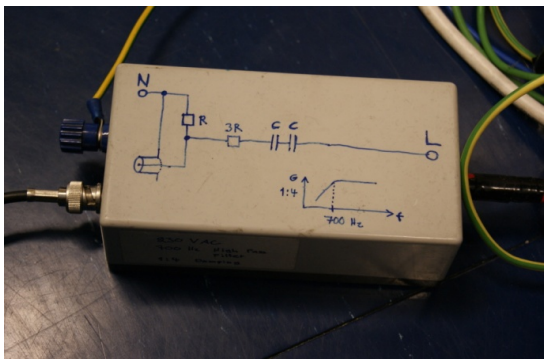

Figure 2. Front-end module for LV network.

3. Prototype of Intelligent Electronic Device

The prototype of intelligent electronic device following the hardware architecture discussed in Section 2 has been developed which is shown in **Figure 3**. The data acquisition block has been interfaced with DSP using 5 - 6K Interface board developed by Texas Instrument. The 5 - 6K board is intended to maintain a compatible interface with the TMS320 series of DSP according to the guidelines set forth in the TMS320 Cross-Platform Daughter Card Specification (SPRA711) [8]. Additional power of ±12 V and +5 V are required to power up the interface board which is necessary for the analog front end and analog power rail of the ADS7881, respectively.

4. Software Interface

Main novelty of the device comes in the software part where the objective is to capture and process the signal in real-time continuously for a longer period of time (days or weeks). The software interface has been developed to collect and process the samples as quickly as possible. **Figure 4** depicts the DSP design implementation flow diagram of the IED. It starts with initializing the necessary functions for board support libraries, DSP and ADC interfaces, resetting interrupt and timer. The most efficient way of accomplishing real-time processing is by using a timer, hardware interrupt and a software interrupt.

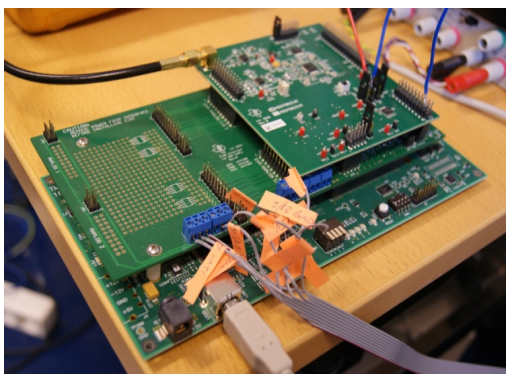

Figure 3. Prototype of the intelligent electronic device.

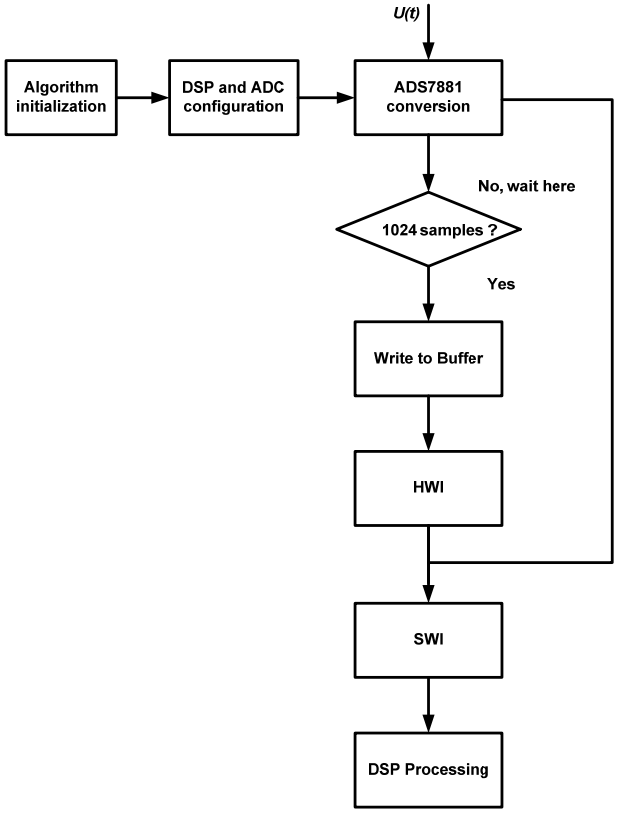

Figure 4. DSP design implementation flow of the IED.

The algorithm is written to collect 1024 continuous samples of analog signal then computing FFT then performing additional post-processing on the FFT data. As soon as 1024 samples are stored into the Buffer, ADC interrupts the DSP which trigger software interrupt (SWI) and go back to fill another set of data to the Buffer. During the time another set of 1024 samples are stored into the Buffer, the SWI executes the inter service routine (ISR) which includes the scaling and computation of signal processing algorithm of the sampled data. The only time constraint is that all the data inside software interrupt service routine must be processed before the active Buffer fills up. It is much easier to meet the real-time constraints with this implementation.

Continuous monitoring of the PLC network is another major aspect of this novel device. It is not possible to meet such goal due to the limited amount of memory available on the DSP. To overcome this issue, a laptop has been attached to the IED which works as a data storage unit. A C code is written to transfer the processed data to the laptop through JTAG emulation.

Frequency Domain Analysis

Time domain waveform does not provide sufficient information about the signals. Therefore, frequency domain analysis is necessary to draw the meaningful result. The waveform assessment is indeed a challenging and time consuming task. It requires an appropriate method and tool especially if real-time processing is a big concern. There are quite a few methods of waveform parameters estimation but, arguably, one of the most popular tools is discrete Fourier transform (DFT), especially its fast algorithm version called fast Fourier transform (FFT). An efficient FFT algorithm is implemented on the IED to meet the real-time challenges. Typical FFT algorithms assume complex input and output data. Most of the time domain data are real valued. A simple solution to this problem is to pad N-length zero-valued sequence as imaginary component with real-valued signal to make it a complex input to compute the FFT. However, this method is obviously inefficient. The algorithm used in this application assumes N-point real sequence as N/2-point complex valued sequence then it computes N/2-point complex FFT on the complex valued sequence. In the first step, only N/2 points of the N-point sequence are computed. Since the FFT of a real-sequence has symmetric properties, the remaining N/2 points FFT are easy to compute with equations. Complete description of the algorithm along with equations can be found in [9].

5. Experimental Setup

The prototype IED has been tested in the laboratory. A setup using smart energy meter and data concentrator which acts as a central unit has been used. These meters are fully electronic and smart which record the consumption of electric energy and send that information to the utility for billing purposes. They communicate over low voltage network using power line communication. **Figure 5** shows the necessary connection setup to power the signal conditioning, data acquisition and DSP block of the IED. **Figure 6** shows the smart meter and concentrator setup used to test the PLC communication using the prototype IED. Modern energy saving lighting can emit high frequency interference in the frequency range chosen for PLC communication. A low-power load model based on CFL and LED lamps as shown in **Figure 7** is developed to test the capability of IED to detect the high frequency phenomena in PLC network. A block diagram showing the experimental setup among LV network, smart meter, concentrator and load model is shown in **Figure 8**. Prototype IED is used to monitor the adverse interaction between PLC communication signals and noise generated by the load.

6. Results

This section explains about the results computed by the prototype IED. Matlab has been used to plot all the figures for better presentation. Before making any measurements with the load setup, a reliability test of the IED

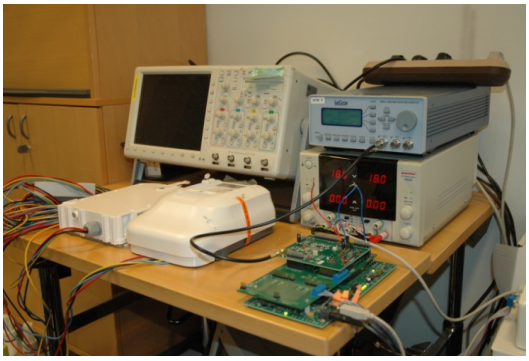

Figure 5. Connection setup in the laboratory.

Figure 6. Smart meter and concentrator setup.

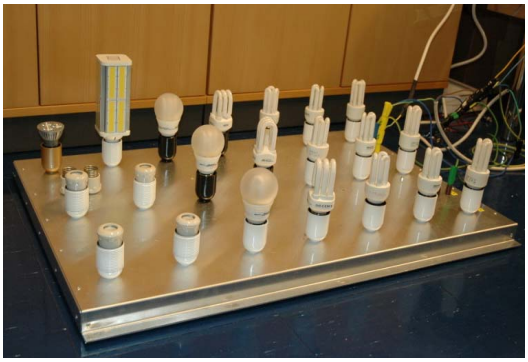

Figure 7. Load model based on CFL and LED lamps.

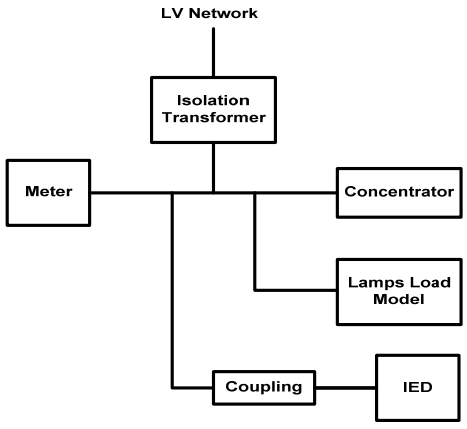

Figure 8. Block diagram showing the experimental setup.

along with the software algorithm implemented on the IED has been made by comparing the FFT spectrum of the known signal computed by the IED and measured by Rhode & Schwarz spectrum analyzer ESPI-3. **Figure 9** shows the spectrum of 80 kHz signal captured by IED and spectrum analyzer. The spectrum analyzer is typically a more expensive piece of test equipment when compared with this low-cost IED. Despite the low sampling frequency and dynamic range, IED has detected the 80 kHz signal quite accurately comparing to the spectrum analyzer which is evident from the graph.

After successful reliability test, IED was connected with the load setup to monitor the behaviour of the PLC network. **Figure 10** depicts the time-domain waveform (without scaling) of 50 Hz signal captured by the IED. It is clearly visible that PLC signals are modulated over 50 Hz cycle and communication between meter and concentrator is going on in most of the cycle. No communication is going on between meter and concentrator for a short duration of time which is also indicated in the waveform.

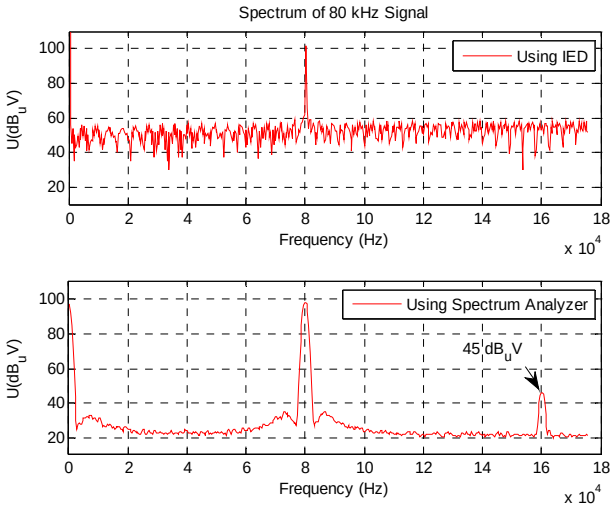

Figure 9. Spectrum analysis using IED and spectrum analyzer.

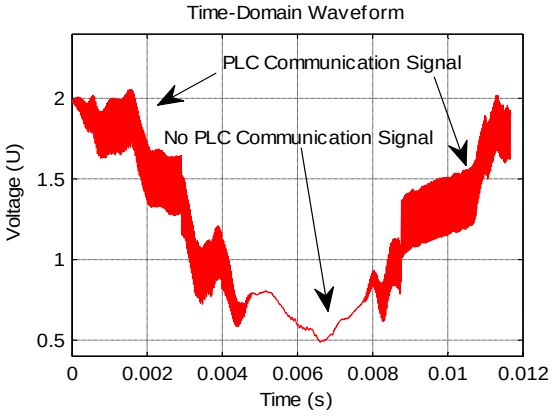

Figure 10. Time-domain waveform captured by the IED.

Frequency-domain analysis gives description about the distribution of energy in the signal as a function of frequency. It is necessary to determine other high frequency components present in the signal which act as a noise. **Figures 11** and **12** shows the frequency domain analysis of the load network computed by the IED. It can be observed from the graphs that the IED is capable of monitoring frequencies up to 175.78 kHz with the current system implementation. High frequency phenomena can be observed in both the spectrum through the whole PLC band. The primary source of the noise is the load model which has CFL and LED lamps connected with it. The operating frequency of a CFL is often just above 40 kHz. The high frequency components above 40 kHz in both the spectrum are the emission caused by the switching element in the CFL. In **Figure 11**, the fundamental harmonics can be seen clearly at 43 kHz, followed by a second harmonic at 86 kHz and a third harmonic at 129 kHz. Harmonics can easily pollute the network which is a big concern for successful PLC communication. Other high frequencies present at 12 kHz and 115 kHz as shown in **Figure 12** are probably due to other power electronic devices connected to the distribution network.

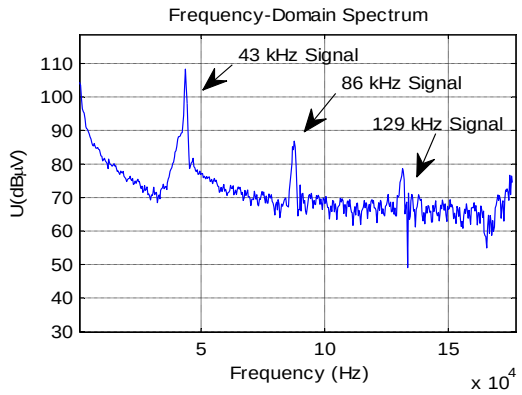

Figure 11. Frequency-domain spectrum computed by the IED.

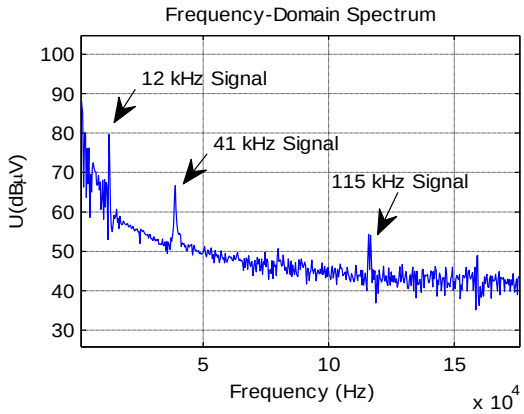

Figure 12. Frequency-domain spectrum computed by the IED.

As is known, the noise floor limits the smallest measurement that can be taken with certainty since no measured amplitude can, on average, be less than the noise floor. According to the EMC standard EN 55011, conducted emissions from RF equipments should be below 56 $dB_{\mu}V$ at 150 kHz and decrease to 46 $dB_{\mu}V$ at 500 kHz. The IED has been designed to meet the following measurement limits. Noise floor of the IED is around 45 $dB_{\mu}V$ which can be observed from **Figure 12**.

It can be further analyzed from **Figure 9** that spectrum measured by spectrum analyzer has second harmonic at 160 kHz which is not found in the spectrum computed by IED because its amplitude is just below the noise floor of the IED. The result proves that IED is capable of monitoring the lowest possible interference set forth by the EMC standard.

7. Conclusion

The design and development of a novel intelligent electronic device for real-time monitoring of high frequency disturbances in PLC network is presented in this paper. The prototype IED has been tested in the laboratory with adequate equipments. The test results have shown very efficient performance in the robust distribution network and computed very accurate results. The IED provides a versatile environment to study and analyze the behavior of LV network in general and PLC network in particular. Moreover, it can be used as a cost-effective platform to develop tools for electrical utilities to monitor the PLC network to solve the practical issues related to disturbances and PLC communication problems. The future prospect of the IED is to make index calculation from the FFT data to extract the valuable information to classify the quality of the signal. The IED will be installed in real field for longer durations of time to monitor the time-variant behavior of the PLC network.

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