Deep Traps and Parasitic Effects in $Al_{0.25}Ga_{0.75}N$/GaN/SiC Heterostructures with Different Schottky Contact Surfaces

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Abstract

Hysteresis phenomenon in the capacitance-voltage characteristics under reverse-biased Schottky gate has been investigated for $Al_{0.25}Ga_{0.75}N$/GaN/SiC structures having three different gate surfaces. This parasitic effect was correlated with the presence of deep levels in our samples. Indeed, we have noticed the presence of two traps named H1 and A1; their respective activation energies, which are determined using capacitance deep level transient spectroscopy (DLTS) are respectively 0.74 and 0.16 eV. The H1 hole trap was associated to extended defect in the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure such as threading dislocations and was responsible of capacitance hysteresis phenomenon. The A1 electron trap appears only in the HEMT (1), which has the smaller Schottky contact area. This trap was related to a punctual defect and attributed to free surface states in the access region between the gate and the source.

Keywords

AlGaN/GaN HEMT, Capacitance Hysteresis, Deep Traps, Gate Surface Effect

Subject Areas: **Applied Physics**

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1. Introduction

GaN high electron mobility transistors (HEMT's) have revolutionized power amplification from RF to millimeter-wave regime. At 4 GHz, a power density in excess of 40 W/mm has been demonstrated [1] [2]. However, the degradation and the reliability problem of GaN-based HEMT's, caused by the trap-related effects, has been a critical problem that was widely discussed in recent years [3]-[12]. These defects may result from surface states and threading dislocations in the AlGaN/GaN herostructures [6]-[12]. The well-known phenomena are capacitance hysteresis [7] [10] [11], high leakage current [10]-[13], Kink effect [3]-[6] and drain current collapse [3] [5] [6] [9]. In this context, as a preliminary study of parasitic effects, we had started by examining the electrical behavior on the AlGaN/GaN heterostructures by the use of a variety of electrical techniques C (V), Ig (Vg), Ids (Vds), capacitance DLTS and drain-current DLTS [6] [10] [11]. This study enabled us to locate certain anomalies in the electrical characteristics of these components which seem to be caused by trapping mechanisms of the carriers by defects. In particular, capacitance DLTS measurements carried out for three samples with different Schottky contact surfaces [(200 µm × 200 µm), (2 µm × 100 µm) and (1 µm × 100 µm)] revealed the presence of two defects; one negative peak corresponding to a hole trap labeled H1 having an activation energy of 0.74 eV, associated to an extended defect in the AlGaN/GaN heterostructures, and one positive peak corresponding to an electron trap labeled A_1 observed only in the transistor having the smaller Schottky contact surface. The possible explanations of its origin will be established in this work.

2. Experimental

The components under test have been grown by metal organic chemical vapor deposition (MOCVD) on SiC substrate. The device structure growth and its fabrication details were reported elsewhere [6] [10], see **Figure 1**. For this study, the devices have different Schottky contact surfaces of 200 µm × 200 µm, 2 µm × 100 µm and 1 µm × 100 µm for diode, HEMT (2) and HEMT (1) respectively. The C (V) and Capacitance DLTS measurements were done using experimental setups described in detail elsewhere [10].

3. Results and Discussions

3.1. Capacitance-Voltage Measurements

Capacitance-voltage (C-V) measurements of the three (Ni/Au)/$Al_{0.25}Ga_{0.75}N$/GaN/SiC structures were performed at a frequency of 1 MHz and a temperature between 50 and 320 K (an example is given in **Figure 2**) by sweeping voltage successively down (Vg from 1 to −10 V) and up (Vg from −10 to 1 V); the voltage sweep directions are shown in **Figure 2**.

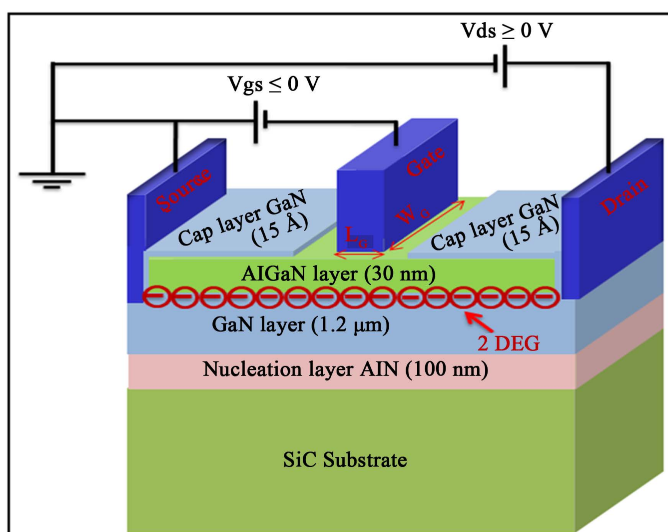


Figure 1. Cross-sectional schematic of an (Ni/Au)/AlGaN/GaN/SiC structure adopted for this work (not to scale).

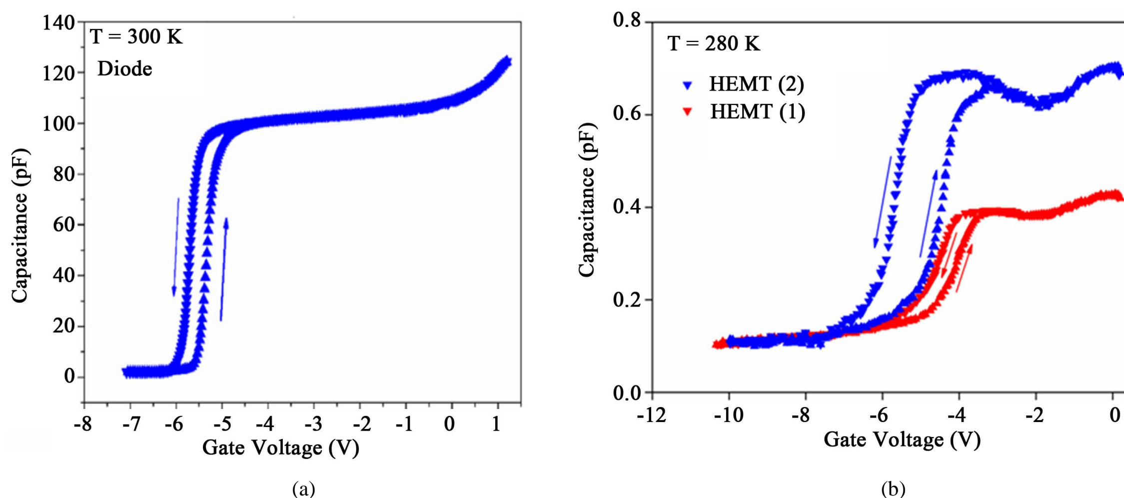


Figure 2. C (V) characteristics, for (a) diode and (b) HEMT (1) and HEMT (2).

A hysteresis phenomenon, expressed by a shift towards lower reverse bias during the return sweep, has been observed. Saadaoui *et al*. [10] [11] have claimed that the hysteresis curve can be explained as follow: A) emission of electrons, B) total depletion of electrons, C) injection and trapping of electrons and D) accumulation of electrons.

This phenomenon indicates a built-in negative charge increase either in the AlGaN barrier or in the GaN buffer layer. This accumulated negative charge is very possibly due to the electron injection from the gate into the AlGaN barrier layer through a trap-assisted tunneling mechanism at high reverse bias [10].

To better understand the hysteresis phenomenon dependence with the temperature, we have determined the hysteresis area at each temperature for the three samples (see the **Figure 3**). We note that the evolution of this phenomenon presents a maximum at ~290 K, for the three samples, whereas it is absent at low temperatures (T ≤ 200 K). This behavior is practically identical to that observed in the (Ni/Au)/$Al_{0.25}Ga_{0.75}N$/GaN/SiC Schottky barrier diode [10], which reflects the thermal activation of deep traps. In **Figure 3**, We remarked that, the hysteresis area at ~290 K in C (V) characteristics is twice higher in the case of HEMT (2), which is in good agreement with the amplitude of the H1 peak observed by DLTS measurements. So, it is reasonable to suggest that H1 trap is responsible of hysteresis phenomenon [10].

3.2. Capacitance DLTS Measurements

In order to clarify the origin of this anomaly, DLTS measurements have been carried out in the temperature range from 50 to 320 K for different rate windows (e_n) and a filling pulse time of 0.5 ms. The DLTS spectra for diode, HEMT (1) and HEMT (2) at $e_n = 213\ s^{-1}$, presented in the **Figure 4**, reveal the presence of one negative peak corresponding to a hole trap labeled H_1 and one positive peak corresponding to an electron trap labeled A_1.

The activation energies were deduced from the Arrhenius diagram of Ln (T^2/e_n) versus 1000/T, as shown in **Figure 5**. The Capture cross section (σ_n) and trap density (N_t) of each observed levels on the DLTS spectrum are summarized in **Figure 5**.

The H_1 trap, observed in the three samples, and the A_1 trap observed only in the HEMT (1), have an activation energy of 0.73 - 0.75 eV and 0.16 eV, respectively. We remarked that, the DLTS spectra of these samples show that the H_1 peak amplitude is higher in the case of diode, which is in good agreement with the hysteresis area in C (V) characteristics. So, it's reasonable to suggest that H_1 trap is responsible of hysteresis phenomenon appearance and leakage current, as demonstrated in our previously work [10] [11]. The H_1 is probably a threading dislocation in the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure [11].

The A_1 trap is related to a punctual defect [11] which appears in the HEMT (1) and is completely disappeared when the gate area becomes important; thus, it seems to be reasonable that this trap ought to be attributed to free surface states in the access region between the gate and the source. Indeed, the gate area increase results a decrease in the free surface between gate and source, which minimize the surface defects [11].

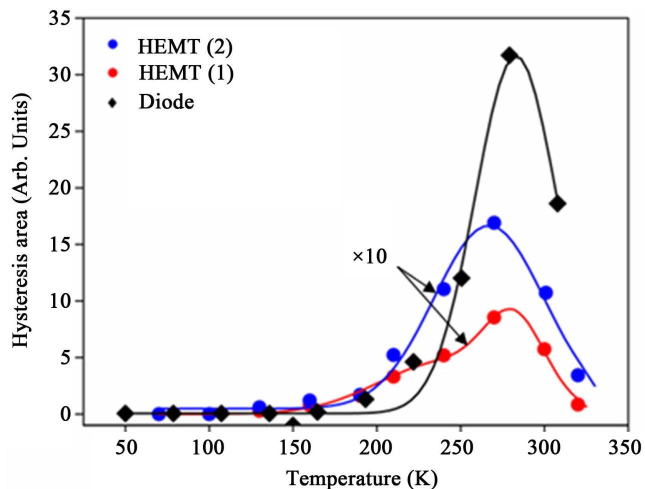


Figure 3. The temperature dependence of the Hysteresis area, for the three samples.

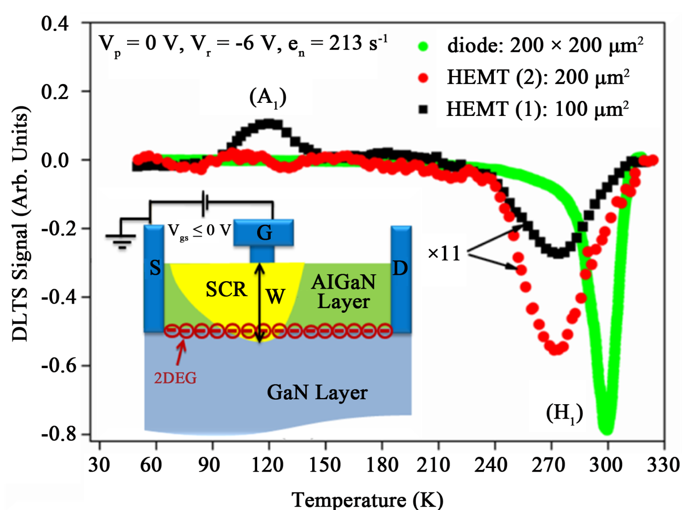
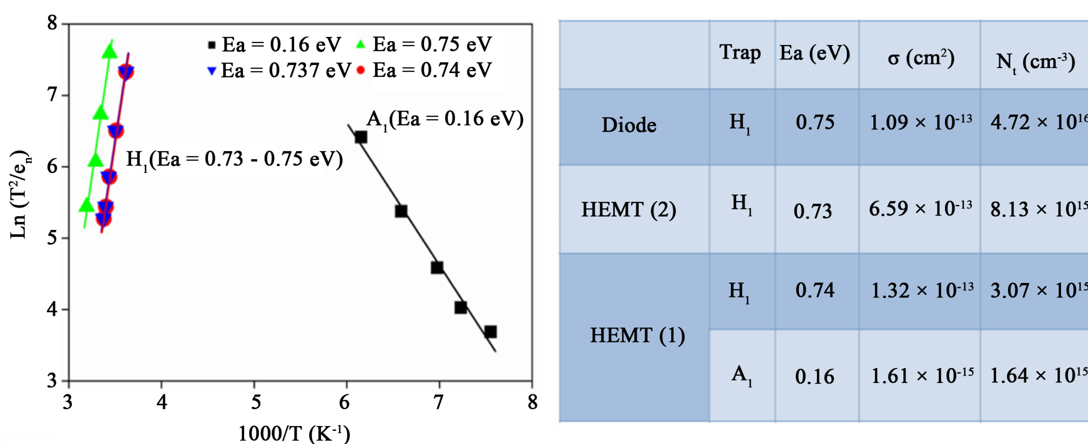


Figure 4. DLTS spectra at reverse voltage $V_r = -6$ V for the three samples. In the inset, a schematic section of the HEMT structure showing the analysis region (not to scale).



	Trap	Ea (eV)	σ (cm²)	N_t (cm^{-3})
Diode	H_1	0.75	1.09×10^{-13}	4.72×10^{16}
HEMT (2)	H_1	0.73	6.59×10^{-13}	8.13×10^{15}
HEMT (1)	H_1	0.74	1.32×10^{-13}	3.07×10^{15}
	A_1	0.16	1.61×10^{-15}	1.64×10^{15}

Figure 5. Arrhenius diagrams plotted for each observed level. The extracted activation energy (Ea), Capture cross section (σ_n) and trap density (N_t) values are summed up in the table.

4. Conclusion

In conclusion, $Al_{0.25}Ga_{0.75}N$/GaN/SiC structures with three different gate areas have been characterized by temperature-dependent C (V). We have marked a capacitance hysteresis phenomenon more significant around the room temperature. This effect is explained by defect-assisted tunneling. This mechanism was assisted by some extended defects as threading dislocations. Using Capacitance DLTS measurements, we have identified two trap levels H_1 and A_1. The H_1 hole trap was associated to extended defect in the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure such as threading dislocations and was responsible of capacitance hysteresis phenomenon. The A_1 electron trap appears only in the HEMT (1), which has the smaller Schottky contact area. This trap was related to a punctual defect and attributed to free surface states in the access region between the gate and the source. These defects were already found in our previous works should have an impact on the transport mechanisms though the Schottky contacts which is the aim of future works.

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