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The Modelization of the Wet Etching Rate by the Segregation Boron and Phosphorus Distributions in Si/SiO$_2$

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Abstract

This study investigated the effects of doping on the etching of SiO$_2$ and in particular on the etched edge (parts). We have modelized and optimized using experimental data the etching rate of SiO$_2$. The effects of temperature and oxide nature are factors taken into account in the modelization. The optimization of temperature permits to define the ideal temperature to be used in order to approach anisotropy and to permit repeatability to the etching process in industry. The modelization is applied on three types of silicon dioxide. It is applied on nondoped, n-doped and p-doped SiO$_2$. The role of the work is to find a model using empirical relationships based on experimental results, to calculate the SiO$_2$ etch rate depending on the type of doping, and temperature. The commented results are based on the segregation at Si/SiO$_2$. We have developed a "theory" based on an empirical equation which modelizes the etch rate in non doped SiO$_2$, to modelize it for those n-doped and p-doped. This "theory" stipulates that the etch rate in doped SiO$_2$ can be predicted by knowing the etch rate in nondoped one. Thus, we have extracted an entity what we called "segregation proportionality", proportional to the diffusion-segregation boron and phosphorus distributions in the silicon dioxide-silicon, and which can be physically and chemically explained.

Keywords

Segregation Coefficient, Doping, Temperature, Modelization, Optimization

Subject Areas: Chemical Engineering & Technology, Electric Engineering

1. Introduction

One of the most basic steps in Integrated Circuit (IC) manufacturing is masking a wafer with silicon dioxide. Subsequent removal of all or part of this oxide layer is critical to device fabrication. "Windows" are formed by chemically etching away the SiO_2 layer at locations defined by lithography methods. This allows chemical action with silicon to take place within those openings, *i.e.* doping, or metal contacts. Thus, the quality of these etched openings is the key to control the electrical properties of the device.

Every step in the conception of semiconductor Circuits must go through several technological processes including: the diffusion, oxidation, photolithography and etching. The chemical etching is the core technology for the elaboration of Microsystems because it allows the realization of various geometric shapes. The shape of the cavity depends not only on the nature and concentration of etching solutions [1]-[3], and the shape of the mask used and the orientation [4], but also on the type of doping of the face exposed, which is focused on in this study. In general, the wet etching is controllable by time, temperature, solution concentration, and solution recirculation or wafer agitation. The etching mechanism of SiO_2 has been described chemically by several researchers [5] [6]. It has been well documented that the etching rates of chemically vapor deposited (CVD) SiO_2 films doped with boron, phosphorous, or arsenic depend on the glass composition and doping concentration as well as the concentration of NH_4F in the buffered solution of HF (BOE) [7] [8]. Many studies have focused on predictive simulation of anisotropic etching. However, the simulated shapes are often in disagreement with experiment near the corners. Concerning the etching chemistry, the operation process involves the transport of reactants to the surface, the surface reaction and the transport of products from the surface. Physically, the silicon dioxide etching is accompanied by rise of pits, the holes begin to grow and their number decreases. This process is repeated several times until the surface becomes completely etched but before the end of etching, and other pits are formed inside the SiO_2 (in the interne layers), so with the use of different methods [9] [10] to simulate this phenomenon, the simulation is still difficult. The recourse to the modelization is preferable.

We modelize the SiO_2 etch rate using empirical relationship issued from experimental results, which coincide with the experience in certain parts of the oxide. The modelization consists to use a common expression for the three studied cases that characterize the difference in the existence of a factor depending on the dopants's segregation coefficient. It is found that it is sufficient to do a modelization of the etch rate in non doped silicon dioxide, and to deduce it for an n-doped and p-doped one through the parameter called "segregation proportionality". This article is organized as follows: in Section 2, we describe the experimental detail used in this work. Results and discussions of our study will be presented in Section 3. Finally, a summary of the work is given in Section 4.

2. Experimental Detail

2.1. Samples Preparation

The experiment was realized in the manufacture of IC devices (Entreprise Nationale des Industries Electroniques (ENIE) Sidi Bel Abbes). At the beginning the four point probe technique is used to determine the silicon resistivity.

The work is done on:
- Silicon wafers slightly doped of a resistivity of 4.13 Ωcm.
- P type silicon wafers doped with Boron of a resistivity of 0.75 Ωcm.
- N type silicon wafers doped with phosphorus with a resistivity of 0.75 Ωcm.

Silicon dioxide (SiO_2) is then grown on silicon wafers slightly doped, on P type silicon wafers and N type silicon wafers in a diffusion furnace using high temperatures (~11,000 to 1200˚C). The wafers are placed in quartz boats. The boats are then placed on a platen which transports them into the furnace's quartz tube. The loading and the unloading of 10,000 A oxidized wafers is manual. When exposed to H_2O vapor, the wafers in the oven oxidize forming silicon dioxide (SiO_2) layers between 8000 to 10,000 Å.

N doped and P doped oxides are formed by first depositing the impurity on the silicon wafers, followed by a simultaneous diffusion and oxidation in the furnace.

2.2. Etching Process

Hydrofluoric acid (HF) is universally used as a "buffered" solution, which can keep the etch rate low and constant,

by moderating the PH level of the bath. This allows the etching time to be reliably correlated to the etching depth.

The wet etching is prepared in BOE; (with 6 volumes of 40% NH$_4$F: 1).

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{1}$$

The samples are then immersed in a temperature-controlled etchant bath for the length of time necessary to completely remove the silicon dioxide layer. The etch rate depends on the density, type of silicon dioxide film and temperature. Before beginning etching, the time needed to etch through the oxide of known thickness is calculated using the known etch rate of the BOE solution. The etch rate at room temperature ranges between 700 to 1000 Å/min.

A stop watch is used to time the etching process. The wafer is immersed for about half of the estimated time, removed and rinsed with D.I water.

If the silicon dioxide has not been completely etched away, by observing the backside of the wafer for a few seconds, it is immersed again in the BOE solution for an additional 30 seconds. After each etching process, rinsing with D.I water is carried followed by a drying with N$_2$ gun. The color of the remained oxide under a light microscope using incident white light is viewed to estimate its thickness using an oxide color chart.

Alternating between the acid immersion with intervals of 20 seconds, wafers are then rinsed and dried until completion of the operation.

The color is checked again. If White color, the silicon has shown up. Etching the oxide between 10 to 20 seconds longer than necessary, because a very thin oxide layer is invisible since the last few hundred Angstroms of oxide which do not show any color. The etched surface is cleaned for 5 minutes by D.I water and dried with Nitrogen gun. As a final check, the wafer is placed under the microscope, where no oxide should be seen (which has colors), but instead silicon will appear.

3. Results and Discussion

The etching process involves chemical reactions at the surface exposed to the acid. The temperature and doping exercise an effect on the etching rate of SiO$_2$. It is well known that the temperature increases the etch rate as it can be seen either from the graphics in all figures exposed in the paper. An interpolation of experimental data is given. From the reading of the curves an important parameter explaining the phenomenon occurring during etching is extracted.

The nondoped silicon dioxide etching is almost uniformly, it presents a linear or slightly concave profile as illustrated on **Figure 1** which show a constant rate between two points (slope).

For algebraic change in temperature values corresponds a geometrical change in the etch rate. An augmentation in temperature by 10°C lead to an augmentation in the etch rate with a factor of 1.78.

The analytical curve approaches the experimental one.
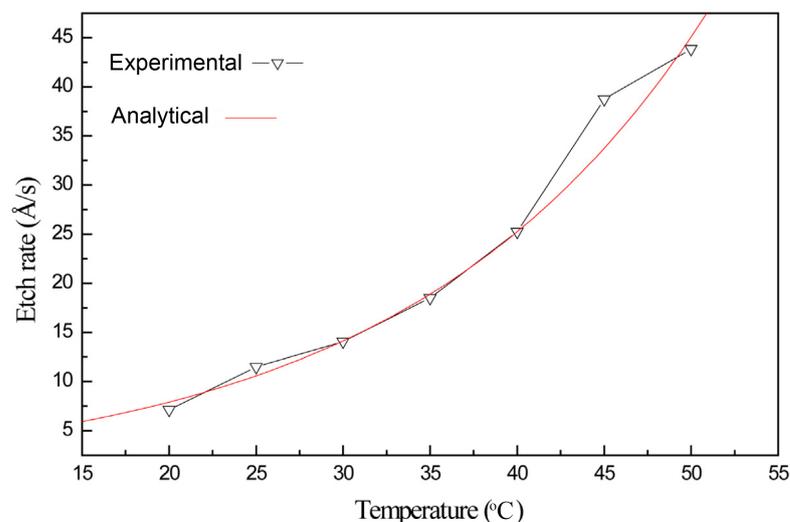
Figure 1. Modelization of nondoped SiO$_2$ etch rate versus temperature.

The etch rate is modelized by the following equation:

$$R(T) = 2.481 \cdot \exp(0.058T) \tag{2}$$

The modelization of the p-doped and n-doped SiO$_2$ etch rate is given by a multiplication of the etch rate in non doped SiO$_2$ by respectively a factor n$_B$ and n$_P$ proportional to the segregation coefficient as given in Equation (3) and Equation (4).

$$R_p(T) = np \cdot R(T)$$
$$np \propto m \text{ Phosphorus case} \tag{3}$$
$$np = 1.08$$

and

$$R_B(T) = nB \cdot R(T)$$
$$nB \propto m \text{ Boron case} \tag{4}$$
$$nB = 0.8$$

with m is the segregation coefficient measured and simulated in many studies [11]-[13].

The etching of SiO$_2$ doped with boron is almost uniform as in the previous case, but is growing and accentuated in the free zones from Boron or which presents few impurities. The top layer of oxide doped with boron (**Figure 2**) behaves as non doped oxide.

The etching of SiO$_2$ doped with phosphorus is fast as compared to the case of non doped Silicon dioxide.

The etching of SiO$_2$ doped with phosphorus is fast as compared to the case of non doped Silicon dioxide (**Figure 3**).

We knew that during the development of structures of an integrated circuit (I.C), each phase of diffusion is followed or accompanied by the growth of a new silicon dioxide film. The oxide growth can have a significant influence on the impurities distribution of the layers under unclaimed in particular close to the interface oxide-silicon. On this point we will emit comments and explanations on the observed phenomena. It is necessary to indicate the effect of the oxide fixed charges on the etching rate. The reduction or the increase in the carriers' concentrations close to the surface can be due to the presence of fixed charges in the oxide. Obviously, the concentration in impurities remains unchanged. The perturbations brought to the surface concentrations by the accumulation phenomenon are not modified by the oxide etching. In the case of induced charges close to the surface, this one tends to reach a normal equilibrium after disappearance of the oxide. So, during the oxide growth on silicon doped with boron, a weak variation of the surface concentration is noticed. Boron tends to preserve an equal affinity for the two solid phases [12]. In addition, phosphorus has a weak affinity for the oxide, but accumulates in the vicinity of the Si/SiO$_2$ interface [12].
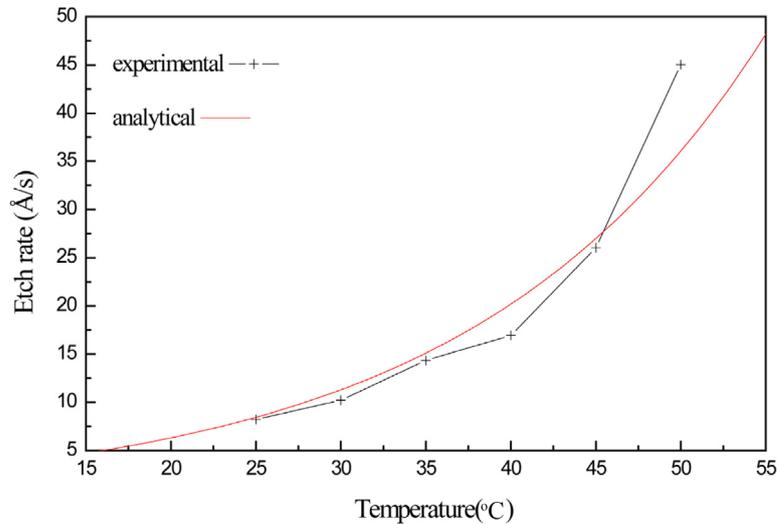
Figure 2. Modelization of p-doped SiO$_2$ etch rate versus temperature.

It is exposed in **Figure 4** the "segregation proportionality" factor to see the difference that exists between etch rate in non doped, n-doped and p-doped SiO_2. We found that the etching rate of SiO_2 doped with phosphorus is fast as compared to the case of non doped silicon dioxide, and it is slower in p-doped SiO_2 as compared to the two other studied cases as shown also on **Figure 4**. This is suggested by the "segregation proportionality" and is in concordance and confirmed by what it is occurring during etching.

In part, it is believed physically that since phosphorous has five valence electrons, the bonded oxygen atom has a larger number of valence electrons from which to choose. Thus, the silicon-oxygen bond is broken more easily in the n-doped silicon dioxide than in the non doped film. Conversely, a boron doped film has fewer valence electrons available and consequently, the silicon-oxygen bond is more difficult to break resulting in an etch rate that is lower than that for non doped silicon glass.

In another part, for doped oxide by boron or phosphorus, the etching rate is either uncontrollable respectively at the beginning of the attack (at surface) or at the end of the attack (the interface). This suggests qualitatively a segregation factor in the two cases. Boron which agglomerates at surface facilitates the etching of deeper layers, especially at the Si/SiO_2 interface. While phosphorus which agglomerates at the interface suggests an early
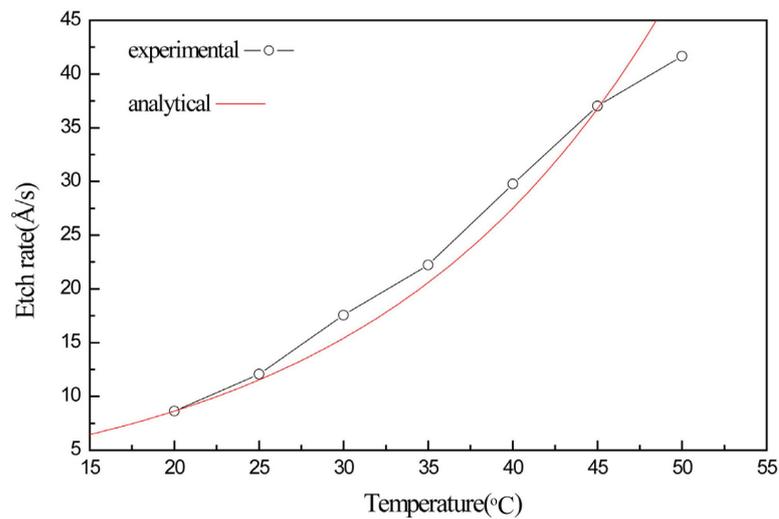
Figure 3. Modelization of n-doped SiO_2 etch rate versus temperature.
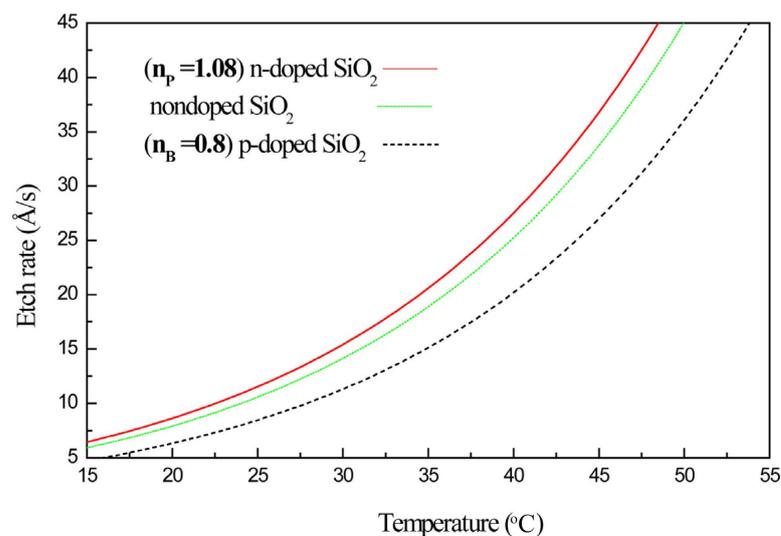
Figure 4. Comparison by the "segregation proportionality" of the etch rate between a non doped, n-doped and p-doped SiO_2.
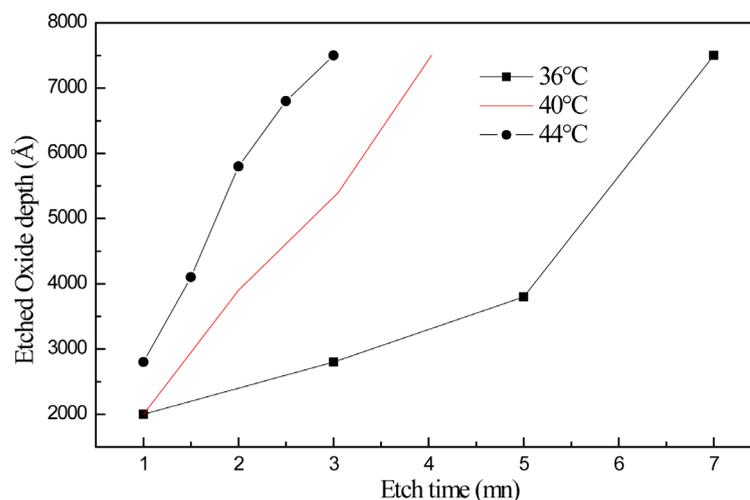
Figure 5. The removed oxide thickness versus etch time at different temperatures.

etching rate relatively large and diminishes close to the interface. The "segregation proportionality" factor used in the etch rate calculation in the n-doped and the p-doped SiO_2 summarizes and traduces these phenomena.

Normalization of Temperature

What we have seen in this study is the qualitative and the quantitative aspect of chemical etching rate of SiO_2 as function of temperature and the type of doping, but the industry is looking for more fixed laws for etching in order to repeat it under the same conditions for any thickness oxide. Using empirical equations we have leads to a prediction of SiO_2 rate etching by extracting a fixed entity depending on segregation coefficient for each case. Another purpose for the industry is to reach an operating point for which the etch rate is linear. The following results elucidate it.

We concluded as it is shown on **Figure 5**, a constant attack around $40°C \pm 1°C$ which is selected as an operating point of the oxide etching.

4. Conclusion

The analytical expressions used to model the etch rate match very well with experimental results. We have indirectly shown in this study, a qualitative and/or a quantitative way, to calculate the degree of segregation of an impurity from another by using the wet etching technique. This is allowed by the factor we have extract from analytical calculation and which is linearly related to the segregation coefficient. A good linearity is reached under $40°C \pm 1°C$ permitting a control of the SiO_2 etching, which prevents undercutting and over etching.

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