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Reduction of Dislocation Densities of Ge Layers Grown on Si Substrates by Using Microwave Plasma Heating and Fabrication of High Hole Mobility MOSFETs on Ge Layers

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Abstract

We have developed a microwave plasma heating technique to rapidly heat the transition metal. W/SiO_2 layers were deposited on Ge/Si heterostructures. By heating the W, dislocations in Ge layers originated from lattice mismatch between Ge and Si crystals were reduced drastically. We have fabricated p-MOSFETs on Ge/Si substrates and realized higher mobility of about 380 cm^2/Vs than that of Si p-MOSFET.

Keywords

Microwave Plasma Heating, High Hole Mobility, Ge on Si

1. Introduction

Since Ge is a high-mobility material compared to Si, has been attracting attention as the next generation of devices [1] [2] [3] [4]. However, since the Ge material has low thermal conductivity, devices fabricated on bulk Ge substrates have low performance due to heat during device operation. And they are not suitable to high-speed operation because Ge material has 1000 times higher intrinsic carrier concentration than that of Si material and parasitic capacitance is also high. To overcome these problems, we grow epitaxially very thin Ge layers on Si substrates. Since Si and Ge crystal have about 4% of lattice mismatch, dislocations are in Ge layers [5] [6].

In this paper, we report that dislocations in Ge layers of Ge/Si heterostructures can bedrastically reduced using new heating method, which can enable us

to heat transition metals selectively and rapidly. We also fabricated p-MOSFET on Ge layer which was heated by our developed method and demonstrated about 2 times higher carrier mobility than that of Si p-MOSFET.

2. Experimental Methods

2.1. Sample Preparation

We grew epitaxially 10 nm Si buffer layers on n-Si(100) substrates at 600˚C. Then, 300 nm-Ge layers were grown on Si layers at the low temperature of 300˚C to avoid island growth. Then, 150 nm-SiO_2 films were deposited at 300˚C by plasma CVD and successively 100 nm-W films were deposited at room temperature by RF sputtering.

2.2. Microwave Plasma Heating

We have developed microwave plasma heating method. This method enables us to heat transition metals selectively by exposing them to hydrogen plasma. Apparatus has four components: a reaction chamber, a 2.45 GHz microwave generator, a gas flow control unit, and a rotary pump evacuation system [7].

In all the experiments, input microwave power is 1000 W, hydrogen gas flow rate is 5 sccm, and pressure is 30 Pa. **Figure 1** shows a typical temperature profile when W film deposited on Ge layer was exposed to hydrogen microwave plasma and the peek temperature was 800˚C. We prepared the samples by changing the plasma exposure time, and the peek values of temperature profiles were from 700˚C to 900˚C.

2.3. MOSFET Fabrication

For MOSFET fabrication, 10 nm-Si buffer layers were grown on n-Si substrate using MBE apparatus at 600˚C. Next, 40 nm-Ge layers were grown at 300˚C. 5 nm-Si cap films were grown at 300˚C. Then, 150 nm-SiO_2 films were deposited at 300˚C by plasma CVD and successively 100 nm-W films were deposited at room temperature by RF sputtering. We heated these samples by the method.

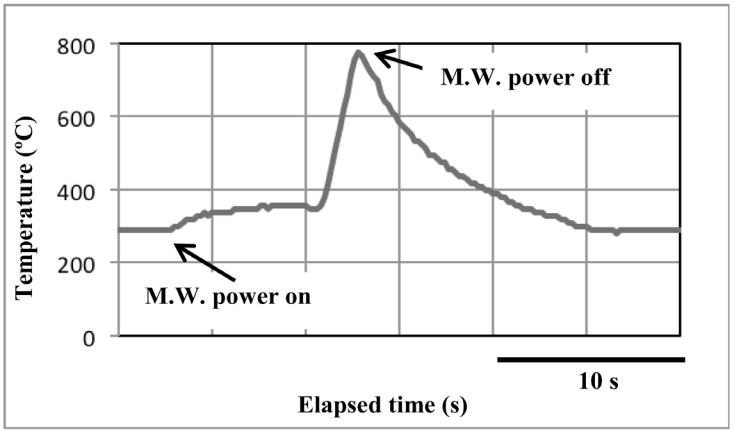

Figure 1. Temperature profile of sample exposed to hydrogen microwave plasma.

The peek values of temperature profiles were around 800˚C. After removing W/SiO_2 layers, we fabricate MOSFETs using conventional device fabrication processes on 5 nm-Si/40 nm-Ge/n-Si substrates. BF2 ions were implanted in source and drain regions at the accelerating voltage of 40 kV with the dose of $1.0 \times 10^{15}/cm^2$. The gate insulator was plasma CVD SiO_2.

3. Results and Discussion

3.1. Optimization of Heating Conditions

We observed microstructures of Ge layers by TEM and STEM. **Figure 2** shows a TEM image of before the heat treatment. The Ge layer has many dislocations. **Figure 3** shows the results of STEM-EDX. Ge layers were grown on Si substrate without mixing between Ge and Si atoms. **Figure 4** shows a STEM image of the sample heated up to 900˚C. It can be seen that Si and Ge atoms are mixed. **Figure 5** and **Figure 6** are STEM images of the sample sheated up to 800˚C and 700˚C, respectively. Mixing between Si and Ge layers are not observed. In addition, we confirmed using STEM-EDX that no mixing occurred. **Figure 7** is a TEM image of the sample heated up to 700˚C. It is seen that dislocations in the Ge layer is drastically decreased.

The heat treatment can reduce dislocations when the peek temperature is from 700˚C to 800˚C, and the mixing between Si and Ge layers do not occur.

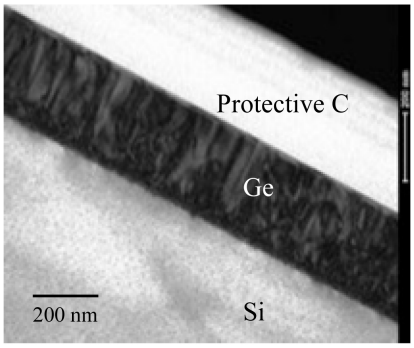

Figure 2. Cross sectional TEM image of as grown sample.

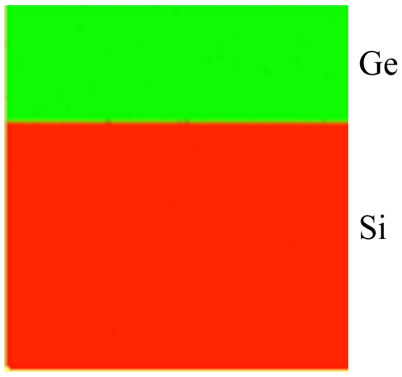

Figure 3. EDX mapping images of Si and Ge elements of as grown sample.

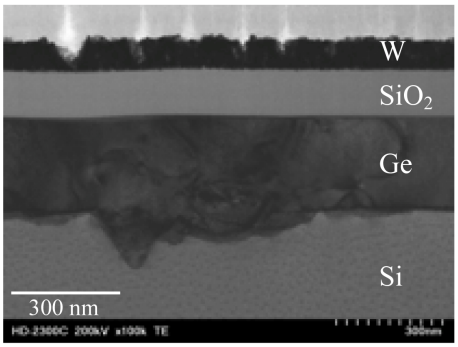

Figure 4. Cross sectional STEM image of sample heated up to 900˚C.

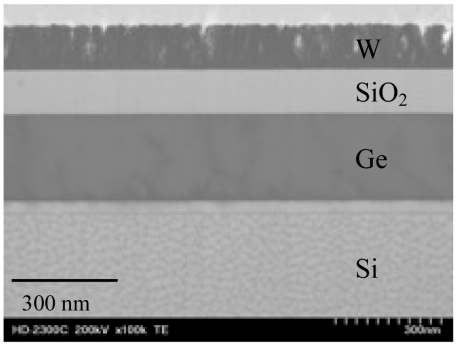

Figure 5. Cross sectional STEM image of sample heated up to 800˚C.

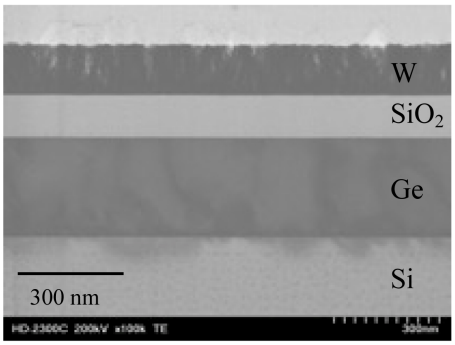

Figure 6. Cross sectional STEM image of sample heated up to 700˚C.

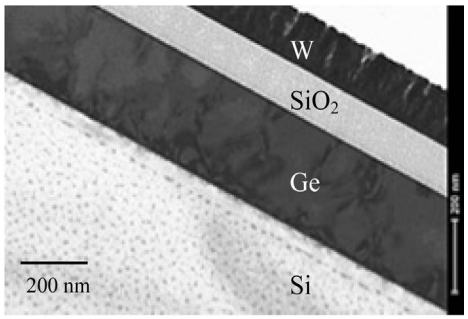

Figure 7. Cross sectional TEM image of sample heated up to 700˚C.

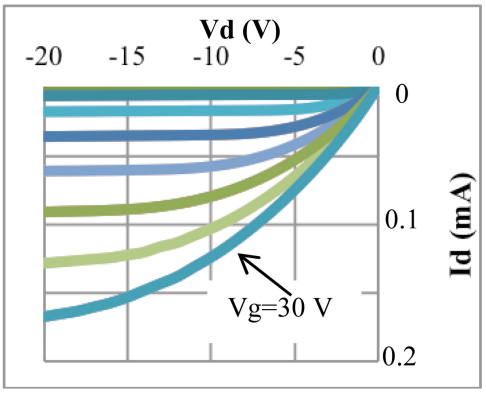

Figure 8. Id-Vd curves of sample which was not heated.

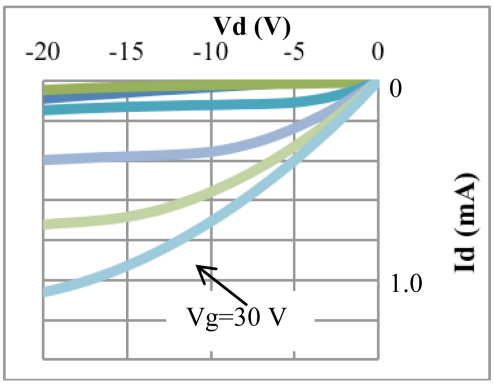

Figure 9. Id-Vd curves of sample heated up to 750˚C.

3.2. MOS FET Fabrication

Figure 8 and **Figure 9** show Id-Vg characteristic of the samples which was not heated and was heated up to 750˚C, respectively. Device dimensions are 100 μm of a channel length and 150 μm of a channel width. The gate voltage was changed from 10 V to −30 V with 4 V increment. The heated sample has one order higher current at the same gate voltage. Effective hole mobility was derived using the split C-V method. We obtain 2 times higher the mobility (380 cm^2/Vs) than that of Si p-MOSFET (200 cm^2/Vs).

4. Summary

We have developed a microwave plasma heating technique to rapidly heat the transition metal. W/SiO_2 layers were deposited on Ge/Si heterostructures. The heat treatment can reduce dislocations when the peek temperature is from 700˚C to 800˚C, and the mixing between Si and Ge layers do not occur. We have fabricated p-MOSFETs on Ge/Si substrates heated up to 750˚C and realized higher mobility of about 380 cm^2/Vs than that of Si p-MOSFET.

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