Materials Sciences and Applications, 2016, 7, 326-347
Published Online June 2016 in SciRes. http://www.scirp.org/journal/msa
http://dx.doi.org/10.4236/msa.2016.76030

Electrical Homo-Junction Delineation Techniques: A Comparative Study

Nicolas Vivet, Mélanie Diogo, Amandine Aubert, Tony Moinet, Fabien Allanic, Raphael Perdreau, Jean-Paul Rebrassé

Failure and Technology Analysis Laboratory (LAT), ST Microelectronics, Tours, France
Email: nicolas.vivet@st.com

Received 21 March 2016; accepted 21 June 2016; published 24 June 2016

Abstract

In active semiconductor devices, the junction characteristics are critical for the electrical performance. As an alternative of the atomic force microscopy (AFM)-based electrical techniques which provide unique junction characterization, other methods are dedicated for the delineation of the electrical junction such as the wet chemical etching, the electrochemical plating method, the Seebeck effect imaging (SEI) method, the electron-beam induced current (EBIC) technique and the secondary electron potential contrast (SEPC) method. The aim of this paper is in the one hand to compare these five techniques in term of sample preparation, spatial application range, spatial resolution, simplicity and information displayed. In the other hand, this review aims to provide some guidelines for the appropriate delineation method(s) selection. It was confirmed that chemical based techniques are the simplest junction delineation methods but exhibit some drawbacks in term of spatial resolution and reproducibility. Despite of a limited spatial resolution, it was evidenced that EBIC can provide accurate electrical characterization of the junction. Finally, it was demonstrated that SEPC is the most promising technique providing the higher spatial resolution. The effect of the sample preparation method has been described. Even if the comparison was mainly based on homo-micro-Silicon junctions (n-p and n-p-n-p), the results were also discussed for short SiC junctions. The importance of the analysis context was considered in this paper and analysis flow was suggested for specific analysis cases.

Keywords

Junction Delineation, Silicon, Silicon Carbide, Electron Beam Induced Current, Seebeck Effect Imaging, Secondary Electron Potential Contrast

1. Introduction

Electrical homo-junctions are elementary "building blocks" of most semiconductor electronic devices such as

How to cite this paper: Vivet, N., Diogo, M., Aubert, A., Moinet, T., Allanic, F., Perdreau, R. and Rebrassé, J.-P. (2016) Electrical Homo-Junction Delineation Techniques: A Comparative Study. *Materials Sciences and Applications*, **7**, 326-347.
http://dx.doi.org/10.4236/msa.2016.76030

diodes, transistors, solar cells, and integrated circuits. As illustrated in **Figure 1**, an anisotype homo-junction corresponds to the junction of two layers of semiconductor of opposite carrier and specific doping parameters. The physical interface between these two layers is called "metallurgical junction" and can be characterized by its localization and dimensions through two parameters: the junction depth (X_j), and the lateral diffusion (X_L). By joining these two layers, electrical phenomena occur, leading to a space charge region (SCR—only containing ionized donor or acceptor impurities) which is characteristic of the doping profile and the metallurgical characteristics. Finally, this is the distribution of this SCR as a function of bias-voltage which leads to the electrical properties of the junction. The SCR is generally deduced from simulation tools and the dimensional junction parameters. Since the electrical performance and behavior of the electrical junction are governed by the previously discussed junction characteristics, their knowledge is critical at various levels: design, research and development (R & D), front-end manufacturing, failure analysis and also benchmarking. Indeed, a wrong localization of a junction can lead to electrical failure, and a wrong junction depth or concentration value can also lead to unexpected electrical characteristics [1]. So, the availability of accurate junction characterization methods is of key importance for the design of new devices on one side and for the characterization of a wide range of failure mechanism on the other side.

Many experimental techniques have been developed for the junction characterization and can provide information about the localization, the dimensions and the doping profile. Among them, the atomic force microscopy (AFM)-based electrical techniques provide unique junction characterization (dopant distribution, junction delineation) through high-resolution (~tens of nm) electrical mapping. Examples of the electrical signals are electrostatic force, capacitance, and electrical current between the tip and sample, which are used for mapping the local surface potential, carrier concentration, and conduction path in the applications of scanning Kelvin probe force microscopy (SKPFM), scanning capacitance microscopy (SCM), and conductive AFM (C-AFM) or scanning spreading resistance microscopy (SSRM), respectively [2]-[4]. Moreover, other complex techniques like secondary ion mass spectrometry (SIMS) or electron holography were reported to provide respectively accurate doping profile and high spatial resolution [5] [6]. When the aim is to quickly delineate a junction and determine its position and depth, without quantitative doping profile information required, other simple and versatile methods are also available. One of the simplest 2D delineation methods of silicon junction is based on wet-chemical etching of doped regions and subsequent observation using an optical microscope or a scanning electron microscope (SEM). The electrochemical plating of metal, such as copper, has been used for years for the junction delineation of many semiconductors such as silicon [7] or germanium [8]. The Seebeck effect imaging (SEI) which is mainly used in electrical-fault localization was also reported to be a barely used alternative way for the junction delineation [9]. While these last techniques investigate the physical nature of the junction (metallurgical junction), other advanced methods focus on the electrical nature of the junction. Indeed it has been demonstrated that Beam-induced current techniques such as electron beam induced current (EBIC) or optical beam induced

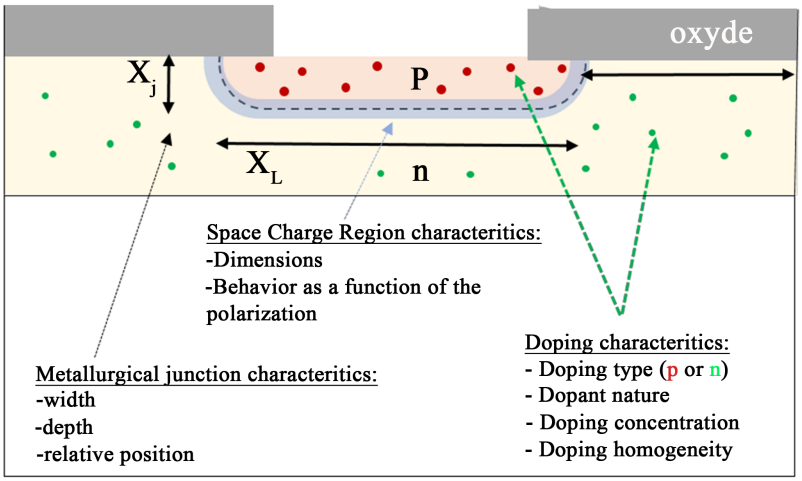

Figure 1. Description of the main parameters describing an electrical anisotype (p-n) homo-junction. Dotted line corresponds to the metallurgical junction, while the thick blue delimitation illustrates the SCR. Green and red circles represents respectively n and p type dopant.

current (OBIC) can provide 2D specimen current mapping (id. mapping of the SCR) [9]. Moreover, the secondary electron potential contrast (SEPC) in a SEM has been used for years for qualitative mapping of doped regions in various semiconductors thanks to a high level of accuracy in the delineation of the electrical junction [10]. For all of these techniques, the sample preparation is a critical step, because it influences the quality of the delineation. Typical cross-sectional methods involve cleavage, Focused Ion Beam (FIB) cross-section, die or molded mechanical polishing with or without FIB finishing.

The present paper aims to compare the five mentioned junction delineation techniques (wet chemical etching, electrochemical plating, SEI, EBIC, and SEPC) on silicon samples (n-p and n-p-n-p junctions) as a function of the sample preparation method in term of quality of the delineation, spatial resolution, simplicity and information displayed. The determination of the dopant concentration is not addressed in this paper, but depending on the technique, information about isotype homojunction (for example n-n+ junction) will be detailed. Since these five methods rely on very different mechanisms, the corresponding physical principles will be firstly reviewed. Then the experimental details of each technique will be presented and the respective results will be compared. Even if the comparison is based on silicon junctions, the results will be also discussed for SiC material in order to highlight the junction delineation dependence upon the sample preparation. Based on the comparison and the review of the main key parameters of a junction characterization request (analysis context), an analysis flow (including delineation and sample preparation methods) will be proposed for the most common analysis type requiring a junction delineation (failure analysis, physical analysis and benchmarking analysis).

2. Basics and Experimental

After a quick description of the studied samples characteristics, the basics and the experimental details of each technique will be described.

2.1. Samples

Two silicon samples were studied. The first sample, “n-p” consists on an n-p diode (n-diffusion on a p-doped Silicon substrate) as illustrated on **Figure 2(a)** and **Figure 2(b)**. For all the investigated techniques, the dies (coming from a wafer) have been cleaved and mechanically polished in order to access the p-n junction on the cross section. FIB cross-sections were also realized for all the techniques except for SEI. According to the design information, the expected depth and width of the junction are respectively 8 µm and 100 µm. Spreading resistance profiling (SRP) has been realized on the studied diode in order to determine the electrical carrier concentration in both n and p-regions, allowing potential comparison with other studies. The profile has been acquired on a bevelled sample (bevel angle = 11.54˚) by using a SSM200-NANOSRP system. As illustrated in **Figure 2(c)**, the carrier concentration was estimated to 10^{18} cm^{-3} and 2×10^{16} cm^{-3} in n-region and p-region respectively. The junction depth was also determined (8 µm in good accordance with the expected value) from the point of transition from n-type to p-type silicon. The second silicon sample, named “npnp”, based on a relatively more complex technology. The sample consists on the following stack: n+/p+/p/n/p+, with typical depth and corresponding SRP data are described on **Figure 2(c)** and **Figure 2(d)**. The periphery of the sample is not described for confidentiality purpose. Cross-section were realized either from packaged units (polishing of molded sample = molded CS) or directly from the dies (after resin removal = die CS). Finally, a SiC sample characterized by a 11 µm depth n-doped layer, and 300 nm and 700 nm depth p diffusions (**Figure 2(e)**) was also studied. For each sample, three preparation methods were used: molded CS, die CS and FIB CS, as illustrated on **Figure 2(f)**. The two first methods imply a mechanical polishing with SiC abrasive papers (up to 1 µm grain size). For the FIB CS, a typical ion current of 20 nA is generally used as a first step, followed by a cleaning step at lower current (5 or 7 nA) depending on the process time. The cleavage was not used because we have considered that such sample preparation method is not suitable for small and localized region of interest.

2.2. Chemical and Electrochemical-Based Delineation Methods

The wet-chemical etching of the silicon is a vital process involved in many aspects of semiconductor processing including the surface polishing of silicon wafer to remove mechanical damage, the microdefects characterization for failure analysis but also the silicon junction delineation [11] [12]. Although there is no formal theory of etching, there are several general principles that have been developed leading to a wide variety of etching solu-

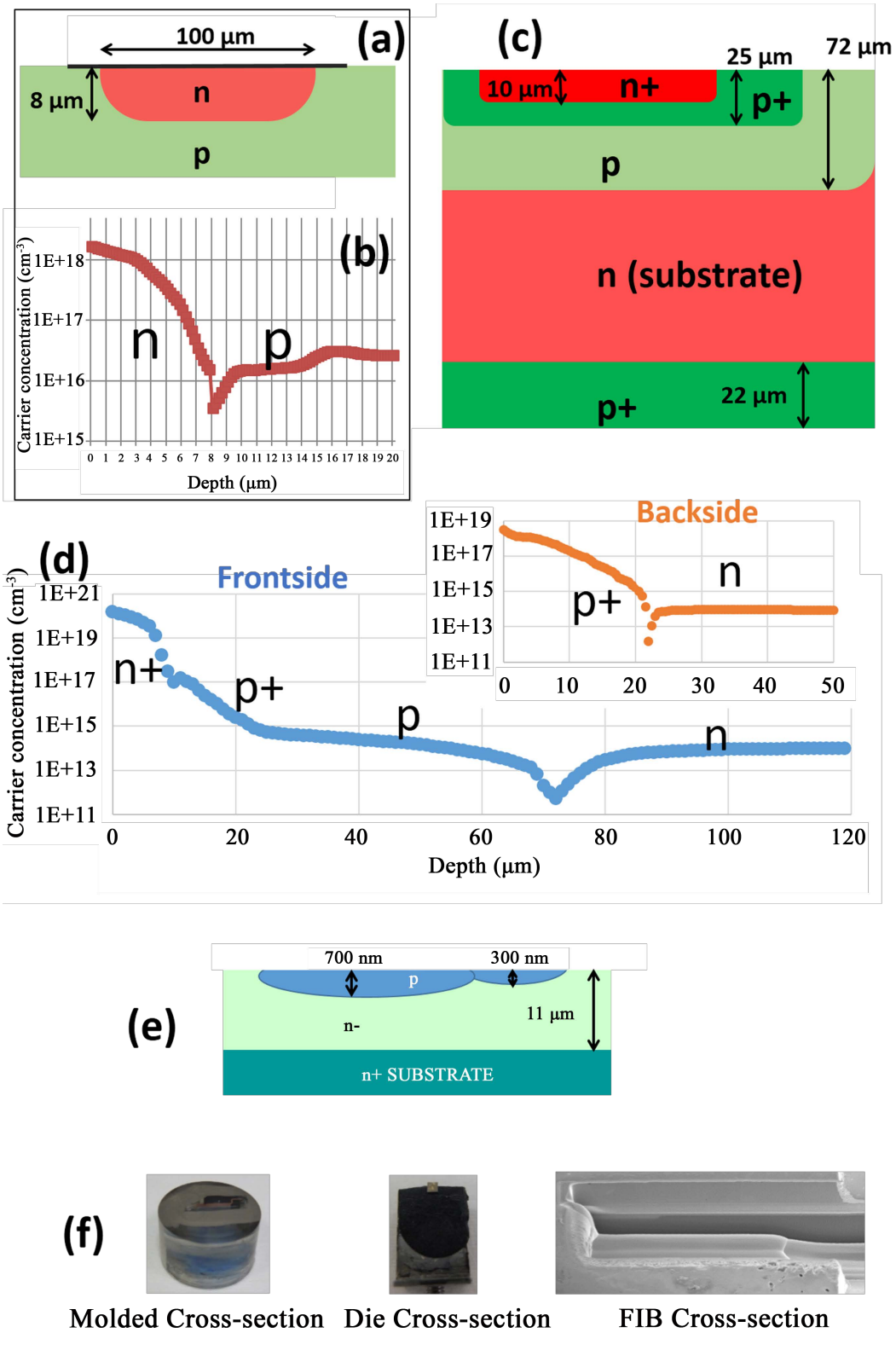

Figure 2. (a) Cross-section view of the n-p diode sample; the top layer corresponds to the metallization; (b) Spreading resistance profile for the n-p diode, junction depth = 8 µm; (c) Cross-section view of the npnp sample; (d) Spreading resistance profiles for the npnp sample for both front and back sides; (e) Cross section view of the SiC unit; (f) Illustration of the three sample preparation methods used in this study.

tions and technical procedures. Among the etching solutions, doping etchant solutions, characterized by a doping-dependent etch rate, can be used for the p-n junction delineation. The corresponding doping etching can be based on the three following attack mechanisms [13] [14]:

1) The different etch rate in p-doped and n-doped areas.
2) The oxidation of silicon at a doping-dependent rate.
3) The plating of material via electrochemical displacement reaction.

2.2.1. Hydrofluoric/Nitric/Acetic Acid System Based Etching Procedure

The most common method for a silicon p-n junction delineation combines the two first mechanisms (see **Figure 3**) by using an acidic mixture of three components: -A first component of the etching solution oxidises the surface (such as nitric acid, hydrogen peroxide, chromium trioxide, potassium permanganate or bromine), while -A second component complexes the oxidized species to make it soluble in the etching solution (such as hydrofluoric acid, chloric acid or sulfuric acid). -A third agent, such as water or acetic acid is normally added as a rate-controlling diluent. The most popular oxidant used is nitric acid, and hydrofluoric acid is almost always used as the dissolving agent.

Even if hydrofluoric/nitric acid systems are the most common doping-etchant, there is not a unique prescription in term of composition (acid ratio) and decoration time leading to an accurate p-n junction solution for a specific sample. Nevertheless the effects of the composition of the decoration solution and the decoration time on the quality of the delineation of the p-n junction have been widely reported in the literature [15]. Based on these results, we have decided to define the optimal composition and decoration time for our sample: height solutions with various ratios of hydrofluoric, nitric and acetic acid were evaluated. The best results have been obtained for the following chemical solution at room temperature: 25 mL of nitric acid, 5 mL of hydrofluoric acid and 40 mL of acetic acid. This optimal solution has been deposited for a period of 5 seconds on the cross-sectioned sample and then rinsed with water. This decoration step has been followed by an optical inspection by using a Leica-DM6000 confocal microscope. The decoration process has been repeated until the junction was clearly delineated.

2.2.2. Electrochemical Plating Method

Based on displacement reaction from a metal-ion-based solution, electrochemical plating technique uses selective deposition of a metal such as copper, silver, gold, platinum or antimony on one side of the junction [16]-[19]. Copper sulphate is the most famous etchant for decorating the n-doped areas [20] [21]. Indeed, when the copper sulphate etching solution is illuminated at the p-n junction, electron-hole pairs are created and a photo-current is produced (displacement of the electrons in the n region while the holes are directed in the p region). Cu^{2+} ions coming from the etching solution recombine with the electrons in the n region and copper metal is clearly visible in the n region (**Figure 4**). In both chemical and electrochemical-based delineation methods, the metallurgical junction observation can be done in a simple optical microscope or in a SEM.

The copper sulfate solution used for this study has been obtained by a mixture of $CuSO_4$, $5H_2O$ (60 $g{\cdot}L^{-1}$) diluted with H_2SO_4 (200 $g{\cdot}L^{-1}$). This solution has been dropped for a period of 30 seconds on cross-sectioned

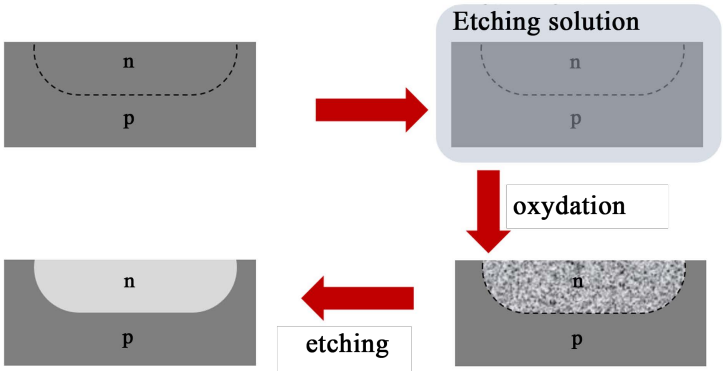

Figure 3. Chemical etching delineation method principle: combination of a two doping dependent rate process: a surface oxidation and an etching.

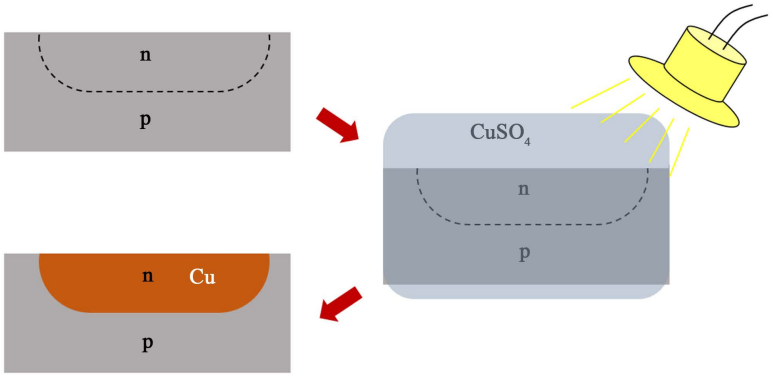

Figure 4. Electrochemical plating technique principle: a mixture containing copper is dropped onto exposed junction; heat lamp is directed onto junction; a battery is formed by the poles of the junctions, with copper solution being the electrolytic solution. The current flow causes the copper in the solution to plate onto the n-region of the junction.

sample illuminated by a lamp. The sample was then quickly rinsed with water and observed with the optical microscope or a SEM. This decoration process has been repeated until the Cu plates on the n-doped area(s). As the decoration time increases, the Cu deposited thickness increases and become less sensitive to the water rinse step. The use of a powerful lamp (halogen lamp) was critical for quick Cu plating. As discussed Section 3.2, we observed that preliminary sample surface deoxidation using hydrofluoric acid can improve this delineation.

2.3. Seebeck Effect Imaging

When a focused laser beam passes over a device, it causes changes in the electrical characteristics through two effects, generation of photo-carriers and heating [9]. If the laser wavelength is chosen to be below the semiconductor bandgap, like in the SEI technique, only heating occurs. The SEI technique is based on the thermoelectric effect and consists in measuring the thermoelectric voltage appearing when a laser beam heats a junction surface. The Seebeck effect can be explained as follows by using a junction of two materials (A-B) submitted to a temperature gradient (**Figure 5(a)**): in the hot region, the electrons are more energetic and therefore have greater velocities than those in the cold region. Consequently there is a net diffusion of electrons from the hot region toward the cold region which leaves behind exposed holes in the hot regions and accumulates electrons in the cold region. The situation prevails until the electric field developed between the hot and cold region prevents further electron motion from the hot to cold region. A voltage gradient, the so-called Seebeck voltage or electromotive force, is therefore developed between the hot and cold regions with the hot region at positive potential. The factor of proportionality S_{AB} is called the relative Seebeck coefficient and depends on the absolute Seebeck coefficient of each material: $S_{AB} = S_A - S_B$. As discussed previously, the Seebeck effect can be observed only if the absolute Seebeck coefficients of each material constituting the junction are (sufficiently) different. This condition is completed in the case of silicon since absolute Seebeck coefficient of p-doped and n-doped Si have been reported to be respectively in the range [10 to 100 $\mu V \cdot K^{-1}$] and [−10 to −100 $\mu V \cdot K^{-1}$], depending on the carrier concentration and temperature [22] [23]. When the circuit is closed, a current will flow in the materials and can be collected through an amplifier. Heat must be removed from the cold junction otherwise the migration of the charge carriers will equalize their distribution in the semiconductor eliminating the temperature difference across the device causing the migration and hence the current to stop. So, the junction delineation is possible by synchronizing the current recording and the laser beam scanning.

An Hamamatsu PHEMOS 1000 IR-Confocal Emission Microscope equipped with a 1300 nm laser (maximum power of 100 mW) has been used for the SEI technique. This equipment is mainly applied for the fault isolation techniques like the emission microscopy (EMMI) or the infrared-optical beam induced resistance change (IR-OBIRCH) [9]. Since the 1300 nm laser has an energy (0.95 eV) below the silicon indirect-bandgap (1.1 eV), the OBIC effect doesn't occur and only Seebeck effect can exist (no electron-hole pair production). Probes have been positioned on each region of the junction of interest. The sample used for this technique was preferentially molded CS. Indeed, the inspection of a FIB CS was not possible because it requires sample tilt, moreover it was difficult to probe on die CS. When the laser scans the sample surface, no bias was applied and the thermoelec-

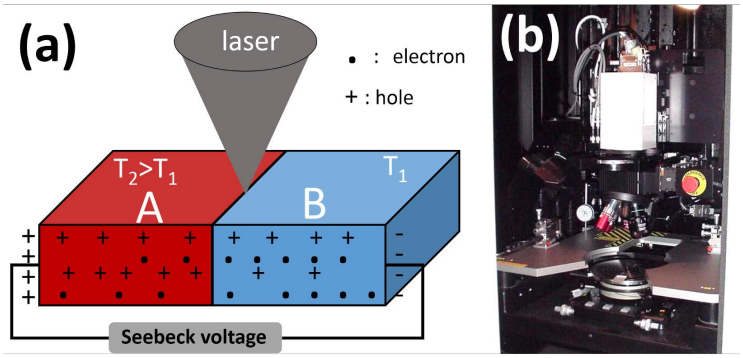

Figure 5. (a) Seebeck effect principle: when scanning the laser across the thermoelectric junction (A-B) a net diffusion of electrons occurs from the hot region toward the cold region. The resulting voltage gradient is called Seebeck voltage; (b) PHEMOS 1000 equipment used for the SEI technique.

tric-current has been recorded through a current amplifier. The signal to noise ratio was greatly improved by using a lock-in unit in the current mode of the equipment with good sample focalization. Optimized parameters are: scan speed of 72 seconds and integration of 3 pictures. The laser power must be reduced as a function of the magnification in order to prevent heating and damage of the region of interest. The pattern image has been also recorded and superposed to the thermoelectric current map providing the accurate localization of the junction.

2.4. Electron Beam Induced Current

The EBIC technique is a specimen current imaging technique using the intensity of the electrical current induced in the specimen by the illuminating electron beam (the so-called EBIC current) [10] [24] [25]. It can be used to determine the localization of junctions (p-n or Schottky) or detect defects in semiconductors like dislocations. The EBIC process can be resumed as follow (**Figure 6(a)**): When an electron beam, such as that in a SEM, strikes a p-n junction, it will generate electron-hole pairs within the beam's interaction volume. Many of these pairs simply recombine and their charge is cancelled. However, if pair production occurs near the SCR (id. depletion region) the carriers are separated by the junction potential before recombination and a net current is produced. If the p- and n-sides are connected in a circuit, the corresponding EBIC current (typically in nA or µA range) can be measured using a suitable current amplifier. The output of the amplifier can be used as an input to the SEM imaging system visualizing the EBIC current value related to the position of the electron beam which is scanned over the sample. The same effect can be achieved by using a laser beam rather than an electron beam, leading to the OBIC technique. Contrarily to the SEI, it requires laser beam energy larger than studied semiconductor band gap able to generate e-h pairs [9].

A Kleindiek system (**Figure 6(b)**) including two micromanipulators for electrical probing and a current amplifier has been installed on a SEM (FEI NOVA 630) for the EBIC investigations. The measurement has been performed in the plan view mode (i.d. junction was perpendicular to the electron beam) by placing a probe in each side of the junction. Thanks to the knowledge of the relative position of the probes and the EBIC signal intensity (bright/dark) it is possible to conclude about the junction nature. Moreover, experimentally it is also possible to qualitatively compare the doping concentration of the two regions constituting a junction because the SCR is systematically more extended on the less doped area as the voltage increases. Whatever the cross section preparation method, the sample was not metallised because it imply short-circuit of the junction and disappearance of the EBIC signal. Because of the charging effects, it was difficult to apply this technique on molded CS. Concerning the SEM operating conditions, the optimal signal to noise ratio has been obtained for an acceleration voltage of 20 kV and an electron beam current of 0.77 nA respectively. The working distance was fixed to about 8 mm; and the "lower stage when venting chamber" option of the SEM was switched OFF for easier probe installation. In order to avoid some artefacts, the CCD camera was switched OFF. The scanning was done perpendicularly to the junction with a scanning rate of 45 µs per pixel in order to obtain a better signal to noise ratio. In the case of EBIC on FIB-CS samples, counterweights were installed on the micromanipulators in order to facilitate the accurate probe positioning. Since the EBIC signal is highly dependent on the surface quality, the die cross-sectioned samples have been perfectly polished. Moreover a thin glass lamella was sometimes put between the orthogonal stub and the sample in order to prevent parasitic current.

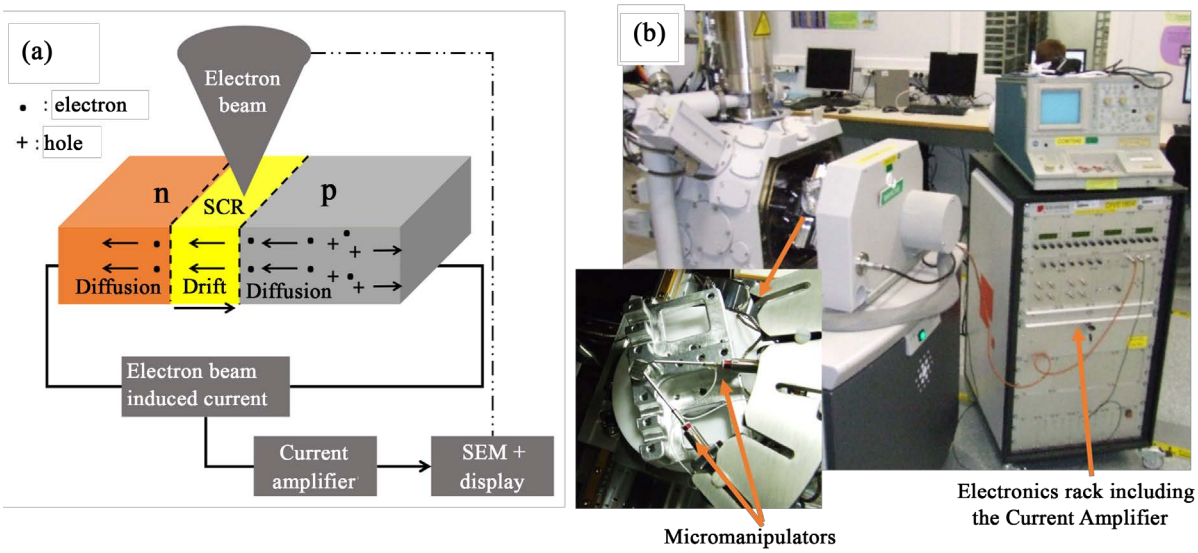

Figure 6. (a) EBIC experimental schematic principle; (b) SEM equipped with 2 micromanipulators for electrical probing and Kleindiek EBIC amplifier for junction delineation on a FIB CS (sample tilted at 52˚).

2.5. Secondary Electron Potential Contrast

The SEPC technique, also named doping contrast method, is an attractive alternative method for the delineation of electrical junction which is based on a dopant contrast visible on a SEM at low accelerating voltage (~1 kV). The SEPC in the SEM has been used for years for the qualitative mapping of doped regions in different semiconductors such as silicon, indium, phosphide, gallium arsenide, diamond and zinc telluride [26]. The comprehension of the physical mechanism of SEPC contrast formation was subject to numerous investigations [27]. Generally it was concluded that the SEPC contrast arises as a consequence of the potential contrast due to the built-in potential (V_{bi}), which produces a stray electric field irradiating from the surface of the sample. As illustrated in **Figure 7**, along the trajectory towards the detector, the low-energy SE (few eV) are either accelerated or retarded by the local electric field, depending on the emission site. Close to the SCR the electric field is very intense and the electric field lines are closed loops. Therefore SE emitted in the p-region either impinged into the n-region, or if they have sufficient initial kinetic energy, they are deflected in a direction perpendicular to the axis of the detector. Similarly, electrons emitted in the n-region would be either attracted towards the surface of the sample, or deviated with a large horizontal component of the velocity. These effects, both result into the reduction of the number of SE collected by the detector. In summary, the SEPC image of unbiased junction is expected to consist of bright zones, corresponding of p-doped regions, of dark zones corresponding to n-doped regions, and of a still darker area corresponding to the SCR [28]-[30].

The built-in potential (V_{bi}) in anisotype junctions, can be expressed as a function of the intrinsic carrier density (n_i) and the concentration of acceptors and donors (N_A and N_D respectively) by [28]:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge.

Forisotype homo-junctions V_{bi} basically depends on the logarithm of the ratio of the doping concentrations according to:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N^{(1)}}{N^{(2)}}\right) \tag{2}$$

where $N^{(1)}$ and $N^{(2)}$ represent the higher and the lower doping concentration, respectively. It is interesting to point out that the V_{bi} for the case of isotype junction not depends on the material on which the junction is built, but only on the adjacent dopant levels.

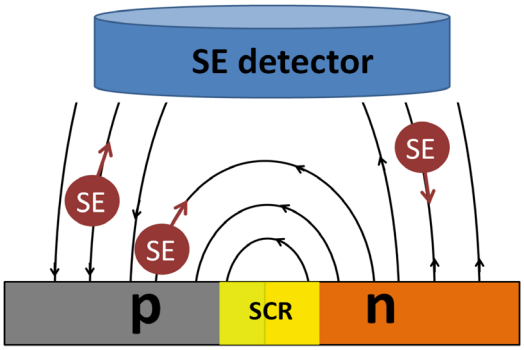

Figure 7. SEPC principle: the electric field lines are represented (from [28]). Close to the space charge region (SCR) the electric field lines are open loops and point in opposite directions. The electric field accelerates secondary electrons (SE) emitted from p-region and retards SE emitted from n-region. So the resulting SEPC image consists in a bright region corresponding to the p-region, a dark region corresponding to the n-region, and a still darker area corresponding to the SCR.

In other words, SEPC technique could be able to delineate anisotype (p-n for example), junctions and isotype junctions (for example n-n+ or p-p+), but, experimentally p-p+ junctions decoration were rarely reported. The SEPC images have been acquired with a dual-beam FIB-SEM equipment (FEI Strata DB 400-S) and with a SEM equipment (FEI Nova 630). The technique has been applied on both mechanical and FIB CS. In the first case, the CS was not metallized. In the other case, a FIB cross section has been realized (ion beam current of 21 nA) on the surface of a metallized sample. Final ion-beam polishing has been realized at lower ion beam current (up to 1 nA), resulting into a perfectly smooth surface. The effect of experimental parameters such as the working distance, the acceleration voltage, the electron beam current or the choice of the detector on the SEPC contrast have been yet reported in the literature [31]. It has been evidenced that a through the lens SE detector (or in-lens detector) provides a better SEPC contrast rather than a lateral Everhart Thornley SE detector. Contrast in this in-lens collection system microscope was also reported to increase in magnitude at shorter working distance. Moreover it was reported that best SEPC contrast is observed for a very low acceleration voltage, typically in the range 0.5 - 2 kV, depending on the author and the material. Indeed, at higher voltage, the equilibrium carrier distribution is modified and the local potential is drastically altered, consequently the electric field at the surface is distorted and the SEPC contrast is noticeably reduced. Based on these results and our own optimization procedure, the SEPC maps have been acquired for the differently prepared samples at the beam accelerating of 2 kV or 3 kV (depending on the SEM equipment used), an electron beam current of about 1 nA, and a working distance of 5 mm. The effect of the SEM operation mode (standard field free or magnetic immersion mode) and the selected detector (lateral or through the lens detector) on the SEPC images have been investigated in this study for both mechanically and FIB cross sectioned samples.

In summary the delineation can be realized either by obtaining a contrast between the doped areas (chemical based methods, SEPC) or by highlighting the delimitation between the doped areas (SEI on the metallurgical junction or EBIC on the SCR).

3. Results

The performance of each of the above-mentioned characterization methods in the delineation of the electrical junction is assessed here by the analysis of the Silicon based junction samples. Since many configurations (2 Si samples, 4 sample preparation methods and 5 junction decoration techniques) were tested, we have decided to illustrate only main results. For each technique the following items were reviewed: the junction decoration description, the influence of the experimental parameters, the sample preparation dependence and the spatial resolution of the delineation. The junction depth values were summarized on **Table 1**. At the end of this section SEPC results for SiC sample will be presented as a function of the sample preparation method.

3.1. Wet Chemical Etching Method for Si Samples

Figure 8(a) and **Figure 8(b)** shows the optical view of the die cross-sectioned samples after chemical-decora-

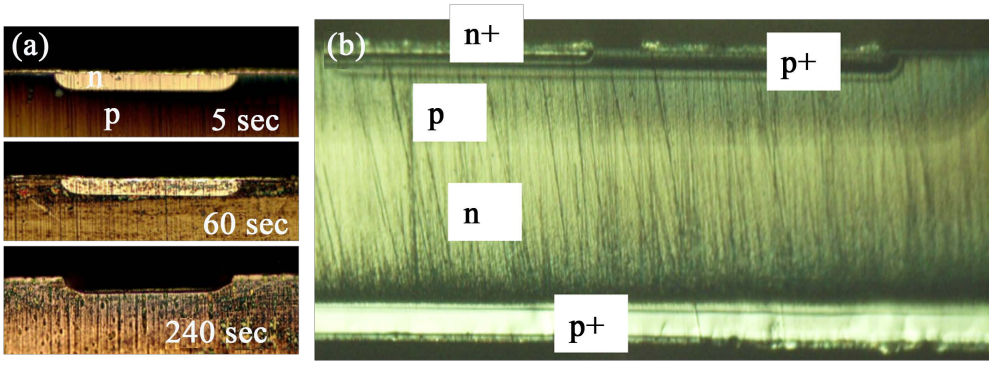

Figure 8. (a) Comparison of the np junction delineation for various decoration time, from 5, 60 and 240 seconds (die CS). Since 240 seconds, the n-doped area was totally etched; (b) Junction delineation result of the npnp unit (die CS) after 5 seconds.

Table 1. Junction depth values of the Si studied samples prepared by die CS deduced from the average of 5 measurements. Values in parenthesis correspond to the standard deviation, illustrating that SEPC technique provided the higher accuracy. The asterisk symbol indicates that the isotype junction was not delineated by the corresponding techniques.

Sample	Studied diffusion area	Junction depth (µm)					
		Chemical etching method	Electrochemical plating method	SEI	SEPC	EBIC	Spreading resistance for reference
n-p	n	9.1 (1.1)	9.2 (1.0)	8.3 (2.1)	8.0 (0.1)	8.4 (1.3)	8.0
	n+	10.4 (1.0)	10.9 (1.4)	9.2 (2.3)	9.8 (0.2)	10.3 (1.5)	10.0
n-p-n-p	p+ (front side)	23.3 (1.5)	(*)	(*)	(*)	(*)	25.0
	p	72.6 (2.1)	74.1 (1.6)	74.7 (4.3)	72.5 (0.2)	74.8 (2.6)	72.0
	p+ (back side)	22.9 (1.4)	23.2 (1.3)	24.7 (3.0)	22.4 (0.2)	23.1 (1.7)	22.0

tion process. In both cases anisotype junctions are clearly delineated. For the npnp sample, the isotype junction (p-p+) is also highlighted on the die CS since the etching rate is sensitive to the doping concentration. As illustrated in **Figure 8(a)**, for the np unit, by increasing the decoration process up to 60 seconds we have observed the broadening of the delineation; and since 240 seconds, the n-doped area was totally etched. The delineation quality was comparable whatever the sample preparation method. The measured junction dimensions were summarized on **Table 1**. For example, the junction width and depth of sample np were measured to 96.9 µm and 8.1 µm respectively. Even if these results are close to the expected values (100 µm and 8 µm respectively), it's important to note that the accuracy of these measurements is limited by the quite broad junction delineation.

3.2. Electrochemical Plating Method for Si Samples

The application of the Copper sulphate based etching procedure during 60 seconds on the cross-sectioned samples is illustrated on **Figure 9** Copper plating is visible on every n regions and we have observed thicker deposition on more doped area (n+ area on **Figure 9(c)**). It is interesting to note that quick dipping of the sample into a hydrofluoric acid (HF) solution before the delineation generally improves the quality of the copper plating. This additional step permits to remove the native oxide formed by the contact of silicon and air. Of course isotype p-p+ junction was not delineated. Good and reproducible results were obtained whatever the sample preparation method. However, as observed on **Figure 9(b)**, material redeposition can occur on the FIB CS during the process. For process time larger than 60 seconds, such redeposition hide the region of interest and induce measurement mistakes. The measured junction dimensions are in good accordance with expected values (**Table 1**), but the accuracy of these measures is limited by the large size of the Cu particles, which delineate the junctions.

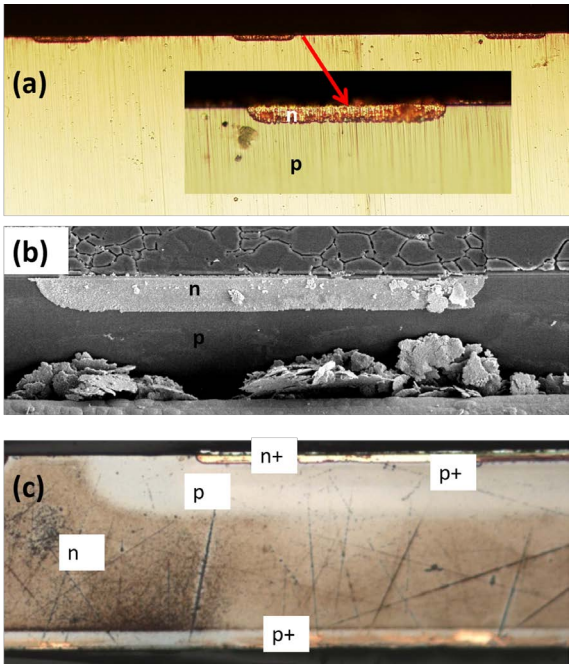

Figure 9. Junction decoration results after 60 seconds of the Cu-SO4 staining method. (a) Die CS of the np unit; (b) FIB CS of the np unit; (c) Molded CS of the npnp unit. Cu metal is only plated on the n-doped region (and on the top-metallization layer).

3.3. EBIC for Si Samples

For the EBIC method, to be able to locate the junctions, it was necessary to overlay the EBIC signal image with the regular SEM image, as presented in the **Figure 10**. The EBIC signal mainly consists either on a bright or a dark and quite broad region which corresponds to the SCR respectively. For the npnp sample, by positioning probes on n+ and p+ areas, all the anisotype junctions were evidenced while, as expected, isotype junction (p-p+) was not delineated. As illustrated in **Figure 10(a)** and **Figure 10(b)**, similar results were obtained by using die and FIB CS preparation. For the die CS preparation, a perfectly polished sample (up to 1 µm SiC polishing paper) was necessary since EBIC signal is highly dependent on the surface quality. Despite of the broad junction delineation (corresponding to the SCR and not to the metallurgical junction), which reduces the accuracy of the spatial measurements, the width and depth of the junctions were roughly estimated from the intensity profile analysis (**Table 1**). The results are in good accordance with expected results. The extension of the SCR as a function of the polarization was not addressed in this paper.

3.4. SEI for Si Samples

The **Figure 11** shows the laser pattern and SEI images of the Si studied samples. The anisotype junctions were delineated through thick delimitation. Bright signal corresponds to positive current flow, while dark signal correspond to negative current flow. For example, in the case of the np unit, by taking into account the relative position of the probes it was possible to conclude that the electrons goes from the bottom of the sample toward the top of the sample (metallization), confirming that the sample consists in a n diffusion into a p-substrate. In the same way, the npnp sample design was also confirmed. By changing the laser beam position relative to the junction(s), we observed the inversion of the current flow (becoming negative), demonstrating the Seebeck nature of the signal : in fact when the laser beam crosses the junction, the polarity of the Seebeck voltage is inverted since the induced temperature gradient is in opposite direction. For both samples, by adding a bias voltage of few volts between the probes, the SEI signal was progressively hidden by a signal localized close to the probes. This signal corresponds to an optical beam induce resistance change (OBIRCH) signal which comes from the current variation at the interface between the sample and the probes. In the studied case, since the thermal conductivities of both p-region and n-region of Silicon are almost similar, the OBIRCH signal is negligible. This result illus-

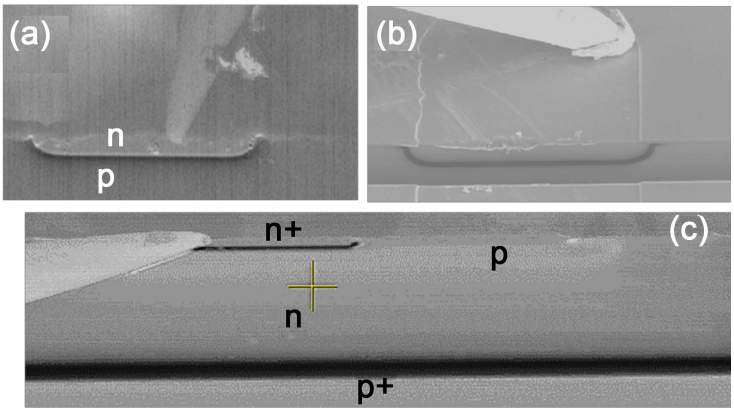

Figure 10. Cross-section view EBIC images superposed to the SEM images. (a) Die CS np unit: a first probe is visible on the center of the picture while the other is localized on the bottom part of the substrate; (b) FIB CS np unit: only one probe was used for this configuration, since the stub supporting the sample was used as grounded reference; (c) Die CS npnp: a first probe was positioned on n+ frontside area while the second is localized on the p+ backside area.

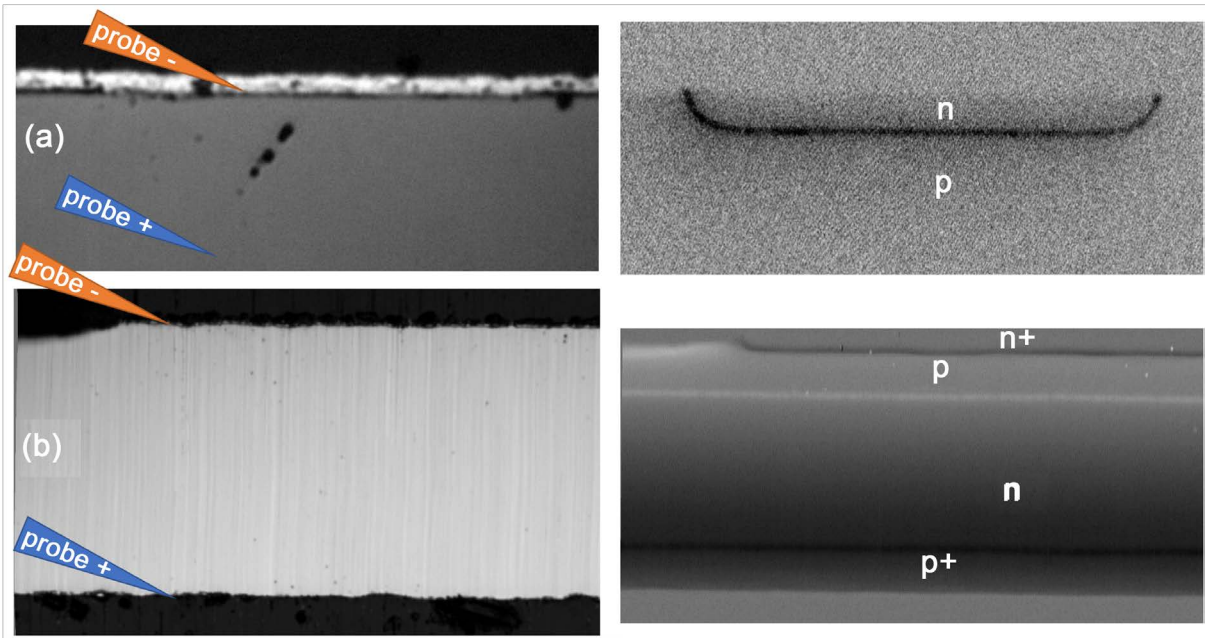

Figure 11. Laser pattern (on the left) and SEI images (on the right) of the studied samples. (a) In the n-p sample, the probe (+) was in contact with the metallization layer while the probe (−) was contacted on the substrate. The SEI image consists on a dark signal (negative flow); (b) In the npnp sample, the probe (+) was in contact with the upper metallization layer while the probe (−) was contacted on the lower metallization. The SEI image consists from top to bottom: on a dark signal (n+/p junction), followed by a bright signal (p/n junction), and finally a dark signal (n/p+ junction).

trates that the SEI contribution is always present in thermal laser stimulation investigations but can be sometimes hidden by other electrical contribution such as OBIC or OBIRCH signals [32]. As discussed in Section 2.3, only die CS was used for SEI evaluation because it provides easier probe positioning versus molded CS. As illustrated in **Figure 11**, the SEI delimitation is quite thick, and consequently the spatial resolution of this technique is reduced. Since our PHEMOS 1000 equipment is not submitted to metrology, the values presented on **Table 1** are not certified, but are close to the expected ones.

3.5. SEPC for Si Samples

SEPC images of Si samples prepared either by die or FIB CS are presented in **Figure 12**. For the die CS, the

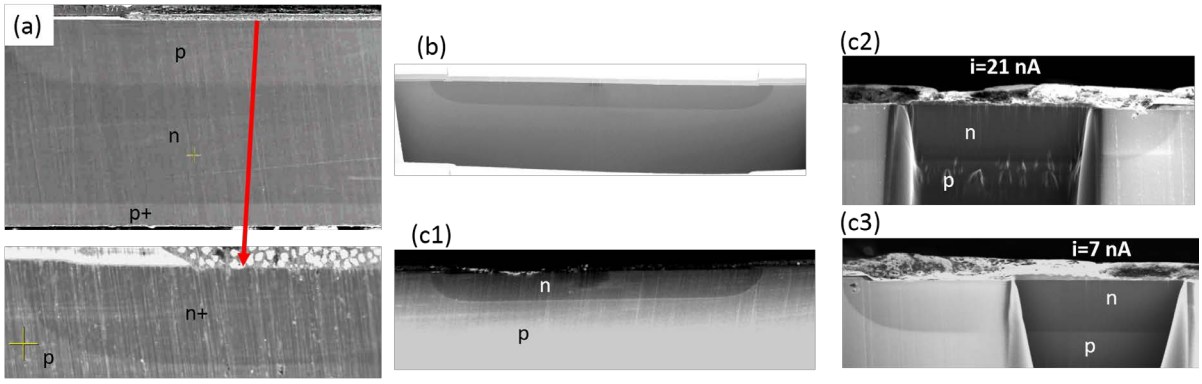

Figure 12. SEPC images recorded in magnetic immersion mode with the TLD detector at 2 kV for: (a) the die CS npnp unit. The isotype junction p-p+ was not delineated; (b) the FIB CS np unit; and (c1) the die CS np unit after mechanical polishing, and after FIB polishing at 21 nA (c2) and 7 nA (c3).

benefit on the SEPC contrast of a FIB polishing step was evaluated with various ion beam current values. The FIB finishing was realized on a non-metallized unit at tilt = 0˚. As expected p doped areas appear bright, while n regions appear dark. For the npnp sample the isotype p-p+ junction was not delineated (**Figure 12(a)**). The effect of the SEM operation mode (standard field free mode and magnetic immersion mode) and the selected detector (lateral-ETD or through the lens detector-TLD) was studied for both die and FIB CS preparation. As illustrated in **Figure 13**, whatever the sample preparation method, in Field free operation mode, higher SEPC contrast has been obtained by using the in-lens detector rather than the lateral detector. As suggested by Buzzo *et al.* [27], this is due to the preferential collection by the in-lens detector of SEs produced from the near surface region of specimens and the suppression of the contribution from SEs produced by scattering from the lens, pole-piece and chamber walls (detected by the lateral detector). Moreover, we observed that SEPC contrast is significantly improved by using the magnetic immersion mode. Recent SEM equipment's are generally equipped with a magnetic immersion lens system increasing detection efficiency with highest resolution (also called Ultra High Resolution—UHR mode). An additional benefit from using this magnetic immersion mode includes high-efficiency SE imaging, and consequently higher SEPC contrast. Indeed almost all secondary electrons escaping the sample are forced back into the SEM's final lens where they can be detected. As illustrated for the np unit (**Figure 12(b)** and **Figure 12(c1)**), the SEPC contrast appears quite comparable for both FIB and die CS. A complementary FIB polishing step on the die CS improves the polishing quality (more visible for lower ion beam current), and SEPC contrast is slightly enhanced (**Figure 12(c2)** and **Figure 12(c3)**). The width and the depth of the junctions were accurately measured on the SEPC images under optimal conditions and are in good agreement with the expected results. Higher spatial accuracy was obtained by using FIB CS preparation or FIB polishing rather than mechanical die CS preparation method since FIB provides smoother surface (no polishing scratches).

3.6. SEPC Results for SiC Sample

Even if this study was mainly focused on the delineation techniques for silicon samples, we have decided to quickly discuss SEPC results for SiC sample, especially in term of sample preparation dependence. As illustrated in **Figure 2(e)**, the studied sample consists in short p diffusions localized on an n-doped layer (11 µm thick). Chemical based method was not efficient to delineate the junctions because SiC doesn't exhibit doping dependent etching rate [33]. Since the sample exhibits very short (300 nm and 700 nm depth) anisotype (p/n-) junctions, SEI and EBIC method were not evaluated. Finally only SEPC method was able to address both anisotype (p/n+) and isotype (n−/n+) junctions delineation for this sample. SEPC investigations have been yet reported and well described for SiC by Buzzo *et al.* [28]-[30], and the corresponding contrast has been reported to be superior to the one generally obtained for Si. This result relies on the difference of built in potential (V_{bi}) existing on the various samples. In the one hand, according to Equation (2) V_{bi} is inversely proportional to the square of the intrinsic carrier density (n_i). In the other hand, at room temperature, n_i is smaller for SiC (10^{-8} cm^{-3}) compared to Si (10^{10} cm^{-3}); so it justifies the superior contrast observed in wide band gap semiconductor like SiC. Our SEPC optimal conditions appear similar to the ones used for Si samples. As illustrated in **Figure 14**,

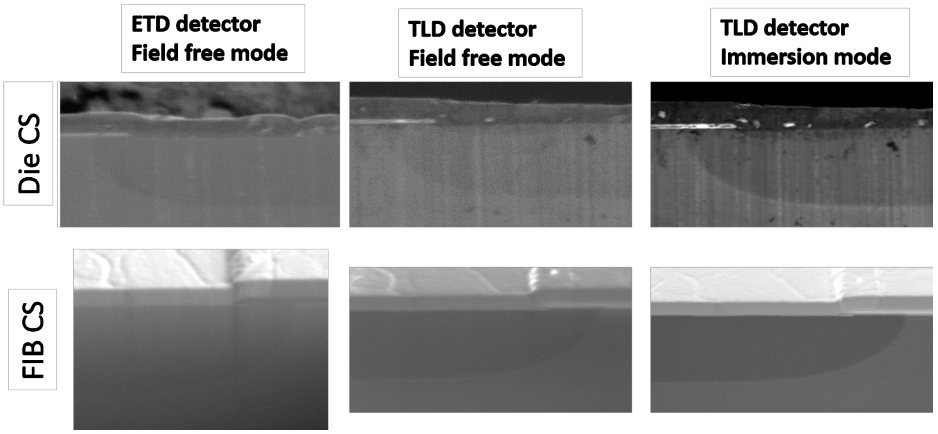

Figure 13. Illustration of the effect of the SEM operation mode (Field free or magnetic immersion mode) and the selected detector (lateral = ETD, and through the lens = TLD) on the SEPC image for the np unit prepared either by die CS or FIB CS (electron acceleration voltage = 2 kV). Higher contrast has been systematically obtained by using magnetic immersion mode and TLD detector.

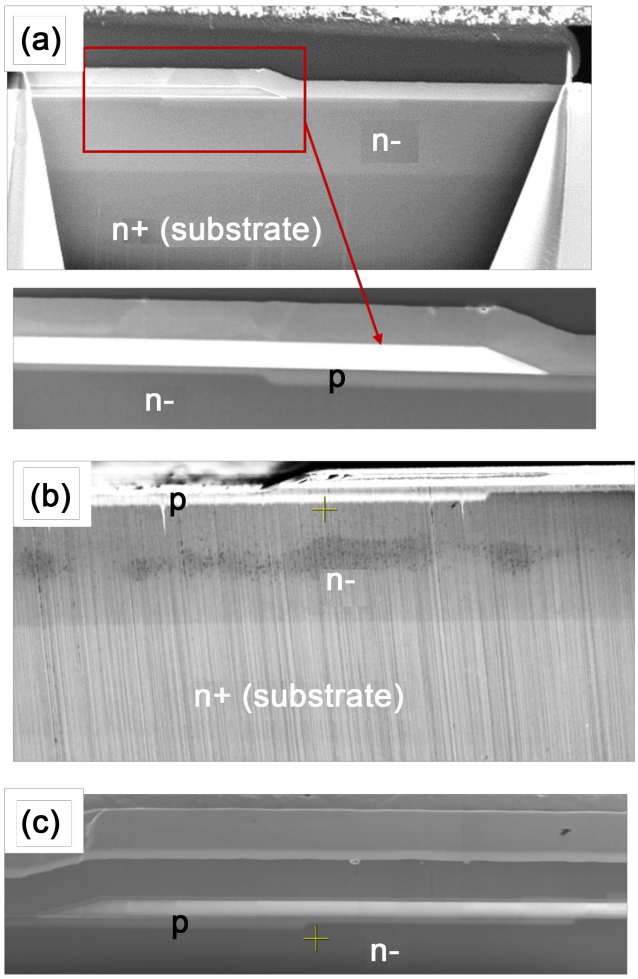

Figure 14. SEPC images (3 kV, 0.64 nA) of the SiC sample obtained in magnetic immersion mode with the TLD detector for: (a) molded CS preparation after 7 nA FIB finishing; (b) die CS preparation and (c) FIB CS preparation. For the two MECA CS preparation methods, both isotype (n−/n+) and anisotype (p/n−) junctions are delineated. On the contrary only anisotype junction is visible for FIB CS.

junctions were delineated but result was highly dependent on the sample preparation method. Molded CS was firstly evaluated and not provided distinguishable delineation. FIB finishing (20 nA ion beam current) was then applied on a metallized molded CS unit without providing good result. It was necessary to reduce the ion beam current to 7 nA (or lower) of the FIB finishing in order to obtain good SEPC contrasted image delineating both isotype and anisotype junctions (**Figure 14(a)**). As observed in **Figure 14(b)**, the die CS preparation method (not metallized sample) provided similar results: all junctions delineated. On the contrary, by using FIB CS only anisotype junctions were delineated, while the isotype junction was not observed (**Figure 14(c)**). Since mechanical polishing process is the same for molded and die CS, we can estimate that the sample surface polishing quality is comparable, and consequently the absence of SEPC contrast on molded unit is not due to an insufficient surface quality, but probably rather to charging effects (higher for molded CS). Then by using ionic polishing process on the metallized molded CS unit, the charging effects were reduced and surface quality was improved (mainly for low ion beam current) leading to delineation of all the junctions. Concerning the charging effects, we can mention the contradictory paper of Hsieh [34] which illustrates SEPC contrast enhancement by using sample charging. The sample preparation method including only FIB CS, even with cleaning steps at low ion beam current, was not able to delineate the isotype n−/n+ junction. Similar result was reported for FIB CS SiC samples and was attributed to the introduction of an amorphous dead layer of few nanometers during the FIB process [29] [35]. This last assumption implies a progressive reduction rather than a cancellation of the SEPC contrast, explaining why isotype junctions are hidden (very low contrast) while anisotype junction are delineated. Since the SEPC contrast depends on the relative doping level of both areas constituting the junction (Equation (2)), it can explain that we have yet observed isotype junction delineation on other FIB CS prepared samples (other design, not described here). So, other investigations will be necessary to accurately investigate the SEPC contrast as a function of the doping concentration. About the spatial resolution, we can mention that FIB CS based preparation methods provide higher accuracy thanks to a better quality surface.

4. Discussion

Based on the previous results, the five junction delineation techniques will be first compared. Then in order to help analyst to choose the appropriate delineation method(s), the links existing between the analysis context and the appropriate experimental set-up will be reviewed. Finally since it is sometimes necessary to use more than one delineation method, analysis flows, only based on the methods addressed in this paper, will be defined for the junction characterization in almost all the types of analysis.

4.1. Comparison of the Five Delineation Techniques

The dimensions of the electrical junction were deduced from the average of five measurements on a same sample, and have been compared in **Table 1**. The comparison was realized on a die CS because this is the only sample preparation method which is applicable for the five delineation techniques. SEM and Optical measurement accuracy is guaranteed to be lower than 5% by tool supplier and metrology verification. However, the delimitation area between two doped areas is not similar for all the techniques, and consequently, it was necessary to calculate the standard deviation (**Table 1**) to compare obtained values with a reference (spreading resistance measurement). All the techniques provide quite comparable measurements, and largest mismatch with expected values not exceed 15%.

The advantages and drawbacks of each technique will be now reviewed, in term of experimental set-up parameters and junction delineation performances based on the point of view of failure and technology analyst. The comparison of the techniques is summarized in **Table 2**. The Chemical Etching Delineation (CED) method is favoured in most part of the laboratories due to its quick and simple experimental procedure. Large inspection area is convenient for many analysis like the global check of unlocalized failure analysis case, or the inspection of a benchmarked (design unknown) unit composed of multiple junctions. Moreover, anisotype and isotype junctions (of both types, for example p/p+ and n/n+) are delineated. However, due to the difficulty in controlling the etching process, this technique doesn't provide reproducibility and accurate quantitative information. For example, junction delineation of short junction (5 µm deep or lower) must be realized very carefully with short process time. Moreover, the presence of various defects such as point defects and dislocations can also affect the etching behaviour and the delineation quality. The electrochemical plating approach exhibits the same advantages than the CED, in term of time-efficiency and simplicity to set-up, but it is also limited in term of spatial

Table 2. Delineation techniques comparison. (1) Chemical method is not always reproducible, or delineation is sometimes difficult to interpret. (2) SEPC: Experimentally p/p+ isotype junction delineation was rarely reported.

	Chemical etching method	Electrochemical plating method	SEI	SEPC	EBIC
Junction delineation type	Metallurgical		electrical		
Delineation display	Highlight etched n doped region	Highlight n doped regions covered by Cu	Delimitation of the metallurgical junction	Highlight p doped regions in bright and n doped regions in dark	Space charge region mapping
Spatial delineation range	HIGH	HIGH	HIGH	LOW (because of SEM imaging)	LOW (because of SEM imaging + probe positioning)
Applicable on multiple junctions design	YES	YES	LIMITED multiple probing configurations required	YES	LIMITED multiple probing configurations required
Require preliminary sample design informations	NO	NO	YES for probe positioning	NO	YES for probe positioning
Spatial resolution	LOW	LOW	LOW	HIGH	LOW
Applicable on short junction (1 µm depth) characterization	LIMITED	NO (large size of the Cu particles)	NO (due to probing)	YES	NO (due to probing)
Junction nature determination	Limited (highly dependent on etching duration)	YES (Cu deposition on n doped areas)	YES	YES	YES
Isotype delineation	LIMITED (1)	n+ = thicker Cu deposition	NO	LIMITED (2)	NO
Other available information(s)	NO	NO	NO	Quantitative approach yet reported	SCR mapping under polarization; diffusion length determination…
Sensitivity to the experimental set up	HIGH	MEDIUM	LOW	LOW	LOW
Sensitivity to the polishing quality	LOW	LOW	MEDIUM	MEDIUM	HIGH
Destructive method on the studied CS	YES	YES	NO	NO	NO
Require Expensive tool	NO	NO	YES	YES	YES
Require specific tool except SEM	NO Common chemical solutions		YES	NO	YES Probing + EBIC ampli
Easy to implement	YES	YES	YES	YES	NO
Safety constraint level	HIGH	HIGH	LOW	LOW	LOW

resolution. One important consideration which should be mentioned, is that this method can inform about the nature of the electrical junction thanks to the Cu plating which occurs only in the n-region. Before copper delineation, an immersion of the sample in hydrofluoric acid is often needed to provide a better delineation [18]. In summary, the CED and electrochemical plating methods only require standard chemical solutions and inspection

tools such as an optical microscope or a SEM which are almost systematically available in failure or technological analysis laboratories. In both cases, the delineation is very sensitive to the experimental set-up while the polishing quality is not critical. Moreover, these methods are destructive (or require further polishing step) and imply the higher safety restrictions due to the use of acid solutions.

Thanks to a standard Confocal Emission Microscope including a laser, quite systematically used for fault isolation (such as ohmic shorts or opens) in failure analysis laboratories, it is possible to delineate electrical junctions through the OBIC or SEI technique, depending on the laser wavelength. The SEI technique is applicable on both die and molded CS, and probes must be carefully positioned. Contrarily to the previously discussed chemical based methods, it doesn't damage the sample, allowing further complementary analysis on the same sample. The spatial resolution of the SEI images is limited by the laser wavelength (1300 nm in the present study) and the IR-Camera pixel size (in the range [0.14 - 14] µm depending on the optical objective). The spatial delineation range is comparable to the one of the chemical techniques since it is based on optical inspection (optical objectives from 5× to 150×). Since SEI technique is based on the probing of the region of interest, it implies two main limitations: first, some preliminary sample design information are necessary for appropriate probe positioning. Second, depending on the sample design, it is sometimes necessary to use multiple probe configurations in order to delineate all the junctions constituting the sample. Despite of these drawbacks, this technique exhibits advantages: in the one hand it relies on a common tool in failure analysis laboratories, and in the other hand it is able to determine the doping nature of the junction by taking into account the sign of the current flow and the relative positions of the probes.

EBIC and SEPC techniques require a SEM equipment which is now present in most of the laboratories. High quality polishing of the non-metallized sample is also required in both cases. As a comparison, a standard SEM working at low acceleration voltage (Field Emission Gun source) is needed for SEPC, while EBIC measurements require a specific, (quite expensive) and dedicated system (including the probes and the EBIC amplifier) and a certain practicability for the required accurate probe displacement. As presented in the Section 2, SEPC and EBIC delineate the electrical junction, inform about junction nature and are not destructive. The spatial delineation range is limited for the two techniques by the SEM imaging. For EBIC, the accuracy of the delineation is better with good focusing and low energy electron beam (limiting the beam sample interaction volume), but it remains a "thick" delimitation (corresponding to the SCR). Among the five studied techniques, the SEPC is the one provided the higher spatial resolution, allowing very short junction delineation (1 µm deep or lower). The EBIC technique exhibits the same drawbacks than SEI concerning its application on multiple junctions design sample and unknown design unit study since probing is required. Despite of this drawback compared to SEPC, the EBIC remains a powerful technique for junction characterization since it was reported that junction characteristics such as minority carrier diffusion length (L) and surface recombination velocity can be determined, under certain assumptions, by studying the EBIC signal as a function of the acceleration voltage [36]. Indeed, the diffusion follows the equation exp (-x/L), and the reciprocal to the slope of a EBIC lines can plotted on a logarithmic axis gives L, indicating the scale over which minority carriers have influence (away from electric fields). The SEPC technique is also a promising technique, for example the quantitative interpretation of the SE signal and the SEPC under polarization (bias voltage) were yet investigated. In fact, new studies have been recently published with the aim to establish a quantitative conversion of the SEPC into the local carriers density, and, finally into the dopant profile [29]. Such approach requires normalization of the contrast profile leading to quantitative results independent of the contrast and brightness settings of the microscope. The quantitative interpretation of the SE signal was yet reported by studying p-type Si samples with doping levels from 10^{16} to 10^{20} at cm^{-3} [37]. Moreover, SEPC studies were realized by applying a voltage bias across the specimen in situ in the SEM [37] [38]. The contrast was reported to decrease linearly with forward biasing of the junction and increase with reverse biasing. This method can provide a better signal to noise ratio and only requires a probe system, like the one used for the EBIC measurement. Finally, as discussed and illustrated in section 3.6, the SEPC technique can also provide delineation of isotype junctions, even if the corresponding contrast is generally lower than the one observed on anisotype junctions [29]. Based on the previous discussion, **Table 3** summarizes the compatibility between the sample preparation methods and the delineation techniques. Even if all the combinations are almost possible (except SEI on FIB CS for sample support geometry constraint), it appears that optimal sample preparation depends on the selected delineation technique. Only CED method is applicable in any cases. For the other techniques, the main limitation concerns sample probing difficulty or charging effects on insulated samples.

Table 3. Compatibility matrix between the sample preparation methods and the delineation techniques. (1) Some material redeposition can occur during the process, hiding the ROI; (2) Corresponds to sample probing difficulties; (3) Corresponds to charging effects on the non-metallized molded samples. For this last point, FIB finishing on the molded CS is an efficient alternative way.

	Chemical etching method	Electrochemical Plating method	SEI	SEPC	EBIC
Applicable on FIB CS	YES	LIMIITED*(1)	NO	YES	LIMITED*(2)
Applicable on die CS	YES	YES	LIMITED*(2)	YES	YES
Applicable on molded CS	YES	YES	YES	LIMITED*(3)	LIMITED*(3)

4.2. Linking Analysis Context, Requested Information, Sample Preparation and Appropriate Delineation Method(s) for an Analysis Flow Construction

The knowledge of the advantages and drawbacks of each delineation method is not sufficient to choose the appropriate one(s). Indeed the sample details and the requested information are the other main and linked elements required for doing the right selection. Moreover, the combination of some techniques is sometimes necessary for a complete junction characterization leading to the construction of an analysis flow.

4.2.1. Appropriate Method(s) Selection Process

As illustrated on **Figure 15**, the selection process of the appropriate delineation technique(s) and corresponding sample preparation method(s) requires consideration of the two following questions: Q1: "what are the Expected results?" and Q2: "what are the sample characteristics?"

The first question was yet answered in **Figure 1** and can be separated into four levels: the junction delineation observation; the junction dimensions determination; the SCR characterization and the doping concentration characterization. The question Q2 is vast because it corresponds to the analysis context description and mainly contains the following information's: the sample technology (Si, SiC, GaN…), the available sample number; the sample type (die, package…); the package type (if applicable); sample design known or unknown; the design dimensions; the electrical design; the diffusion characteristics. Since our study not includes some other wide deployed delineation techniques like SCM or SIMS, it is not possible to build an exhaustive diagram including all the possibilities. This methodology aims to help the selection (delineation method + corresponding sample preparation method) by identifying some incompatibilities with the analysis context. For example, in the case of a magnetic sample (die or package) the SEPC method will not be selected. Indeed, this method generally requires a SEM working in the magnetic immersion mode and the applied magnetic field will disturb the SEM images and will attract the magnetic sample toward the polar piece (critical risk of SEM damage). Other example: if the studied sample design includes a metallic barrier above the junctions of interest, all the methods based on the electrical effects of dopant (EBIC, SEPC) will not be applicable as soon as this barrier will be present. At the end of this methodology, the analyst can use the guidelines included on the **Table 2** to select one or multiple appropriate delineation solutions. Indeed, sometimes, more than one delineation method is necessary to provide all the expected information's. Then, three main scenarios can occur: 1) if multiple samples are available all the appropriate delineation methods can be evaluated in parallel. 2) If only one sample is available with no specific localized area, it is possible to successively evaluate the various techniques by doing successive polishing steps. 3) The worst scenario corresponds to the analysis of a specific region of interest (ROI) with only one available sample. In this last case, analysis flow must be established in advance, by using, of course, nondestructive delineation techniques (such as SEPC, SEI or EBIC) before the destructive ones (chemical based methods).

4.2.2. Analysis Flow Building (One Si Sample with a Specific ROI)

An analysis flow (based on the delineation and sample preparation methods of the present study) will be now suggested for the main kinds of analysis for the worst scenario (3) on a Si sample. First, in failure analysis (FA) the goal is to determine the cause of an electrical failure, which can be related to junction characteristics. Such defect can be a parasitic junction, or junction dimensions out of specifications. In this category, by definition, the accurate position of the junction is unknown. Before doing the physical analysis at the origin of the electrical failure, a preliminary defect localization step (using for example Emission microscopy or Optical Bean induce

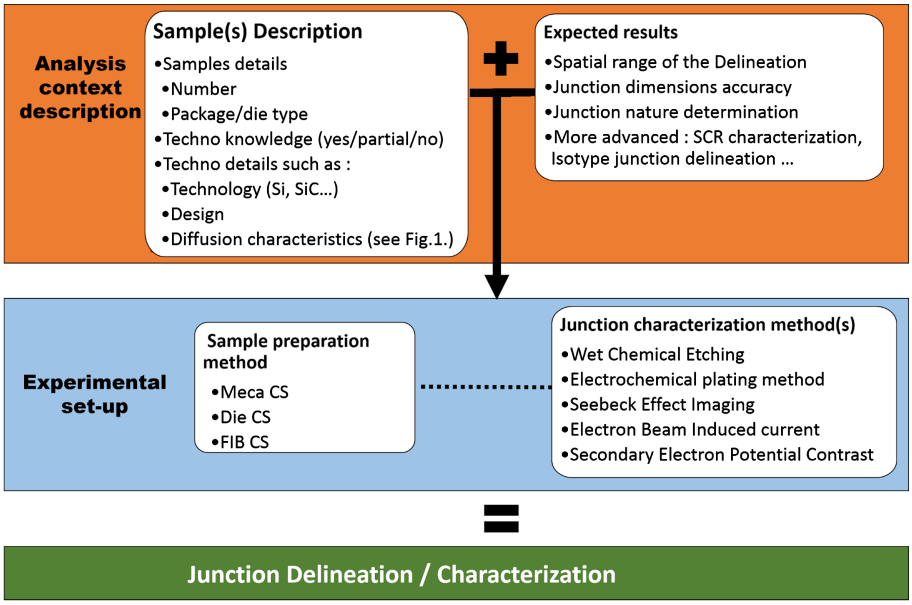

Figure 15. Schematic representation of the selection process of the appropriate(s) junction delineation/characterization methods (only based on the methods addressed in this paper).

resistance change-OBIRCH techniques) is generally realized. Depending on the spatial accuracy of the defect localization and the ROI dimensions, the sample preparation could be different: a FIB CS if the defect is accurately localized, and a die CS if large field of view is required. First, SEPC (nondestructive step) will be used to delineate the junction(s) and determine the junction nature. Then, if it is necessary to check the extension of the SCR as a function of the polarization in order to understand the failure mechanism, EBIC technique could be used. At last, the analyst could use chemical based methods as final destructive steps. In a standard technological analysis (TA), the position of the junction of interest is known, and one of the tasks is to accurately measure the junction dimensions in respect with the specifications. As yet described for a FA, depending on the dimensions of the ROI, FIB or die CS will be prepared. Then SEPC technique will be used in order to provide accurate junction dimensions measurement. A FIB finishing, if applicable, could be realized on the die CS in order to improve the polishing quality and the SEPC contrast. If isotype junction is also present on the ROI and was not delineated by SEPC technique (for example p−p+), further destructive chemical step could be finally realized. Finally, junction delineation could be required for benchmarking or teardown analysis (BA). This last case corresponds to the highest level of expected information's since sample design is unknown. A die CS will be generally prepared in order to provide large field of view. The SEPC technique will be then used to delineate the junction (position, dimensions, junction nature). Thanks to the knowledge of the junction position, it is then possible to use the probing based methods (SEI, EBIC). As yet discussed, EBIC can provide electrical description of the junction(s). As usual, the destructive chemical based methods are eventually used to confirm the previous results and to provide complementary information's, mainly on isotype junction(s). In summary, whatever the analysis type, SEPC technique can be systematically used as a first step. Then the other nondestructive techniques (SEI, EBIC) can be used as complementary steps. Finally, results are confirmed and sometimes completed by using chemical based methods. Of course, these analysis flows can be adjusted regarding the analysis constraints, for example: if only a molded CS is available, FIB finishing will be realized before SEPC investigations, and EBIC measurements will be very difficult. At last, if other quantitative information, like the doping profile are necessary, probe microscopy methods or others advanced techniques mentioned in the Introduction could be implemented with preliminary consideration about their position on the analysis flow.

5. Conclusion

This work was focused on the comparison of five experimental techniques allowing the delineation of electrical anisotype homojunction when quantitative doping profile information is not required: the CED method, the

electrochemical plating method, the SEI technique, the EBIC technique and the SEPC technique. As explained in the Basics section, these techniques rely on very different physical or chemical mechanisms resulting in both advantages and drawbacks for the purpose of this paper. This study done on a silicon n-p and n-p-n-p junctions confirmed that CED method remains as the simplest junction delineation methods but exhibits some drawbacks in term of spatial resolution and reproducibility. It was also concluded that this CED method can be combined with the electrochemical plating of metal (such as copper) approach in order to reach supplementary information about the nature of the studied junction thanks to the Cu plating which occurs only in the n-region. In spite of a limited spatial resolution, it was evidenced that EBIC technique can provide additional knowledge concerning the electrical characterization of the junction. Finally, SEPC imaging appeared as the most promising technique, able to delineate both anisotype and isotype junctions with high spatial resolution. Moreover, actual investigations hold the promise of turning this technique into a quantitative analysis tool thanks to 2D dopant profiles. SEPC results were also presented for SiC sample illustrating the critical impact of the sample preparation method on the delineation result. This discussion aims to provide some guidelines to analyst for the appropriate delineation method(s) selection. The links existing between the analysis context and the appropriate experimental set-up of a junction delineation were highlighted. Finally, the analysis flows suggested for the delineation of a specific ROI on only one available Si sample demonstrates that SEPC is a key nondestructive technique. Further investigations are ongoing in order to accurately check the influence of the doping level on the junction delineation efficiency (detection threshold determination for example). Delineation methods are also under evaluation for GaN junctions.

Acknowledgements

The authors would like to acknowledge the members of the French ANADEF user group on EBIC technique who considerably contributed to the experimental set up optimization. Special thanks to Dr. S. Nizou for fruitful discussion about chemical etching delineation methods. Part of this work was funded by the French government in the EURIPIDES/CATRENE SAM3 project: Smart Analysis Methods for advanced Microsystems and Materials.

References

[1] Schmich, E., Lautenschager, H., Frieß, T., Trenkle, F., Schillinger, N. and Reber, S. (2008) *N*-Type Emitter Epitaxy for Crystalline Silicon Thin-Film Solar Cells. *Progress in Photovoltaics*: *Research and Applications*, **16**, 159-170. http://dx.doi.org/10.1002/pip.783

[2] Nonnenmacher, M., O'Boyle, M.P. and Wickramasinghe, H.K. (1991) Kelvin Probe Force Microscopy. *Applied Physics Letters*, **58**, 2921-2923. http://dx.doi.org/10.1063/1.105227

[3] Kikukawa, A., Hosaka, S. and Imura, R. (1995) Silicon *pn* Junction Imaging and Characterizations Using Sensitivity Enhanced Kelvin Probe Force Microscopy. *Applied Physics Letters*, **66**, 3510-3512. http://dx.doi.org/10.1063/1.113780

[4] Williams, C.C. (1999) Two-Dimensional Dopant Profiling by Scanning Capacitance Microscopy. *Annual Review of Materials Science*, **29**, 471-504. http://dx.doi.org/10.1146/annurev.matsci.29.1.471

[5] Dau, W.D., Schwander, P., Baumann, F.H., Hoppner, W. and Ourmazd, A. (1999) Two-Dimensional Mapping of the Electrostatic Potential in Transistors by Electron Holography. *Physical Review Letters*, **82**, 2614-2617. http://dx.doi.org/10.1103/PhysRevLett.82.2614

[6] Twitchett, A.C., Yates, T.J.V., Dunin-Borkowski, R.E., Newcomb, S.B. and Midgley, P.A. (2006) Three-Dimensional Electrostatic Potential of a Si *p-n* Junction Revealed Using Tomographic Electron Holography. *Journal of Physics*: *Conference Series*, **26**, 29-32. http://dx.doi.org/10.1088/1742-6596/26/1/007

[7] Turner, D.R. (1959) Junction Delineation on Silicon in Electrochemical Displacement Plating Solutions. *Journal of the Electrochemical Society*, **106**, 701-705. http://dx.doi.org/10.1149/1.2427475

[8] Ratcliffen, S. and Hughes, J.E. (1961) The Copper Staining of *p-n-p* Alloyed Junction Transistor Sections. *British Journal of Applied Physics*, **12**, 193-194. http://dx.doi.org/10.1088/0508-3443/12/4/316

[9] Cole, E.I. (2005) Beam-Based Defect Localization Methods. In: Electronic Device Failure Analysis Society Desk Reference Committee, *Microelectronics Failure Analysis Desk Reference*, 5th Edition, ASM International, Materials Park, Ohio, 406-416. https://books.google.fr/books?id=MyVHpqi1SXwC&pg=PT140&lpg=PT140&dq=Microelectronics+Failure+Analysis:+Desk+Reference&source=bl&ots=TbrfdQHucm&sig=jA8XsmpG4V3TuYcSm9vGM0JY_PA&hl=fr&sa=X&ved=0ahUKEwj4063Y-7HNAhWFthoKHVX9DLYQ6AEIZzAH#v=onepage&q=Microelectronics%20Failure%20Analysis%3A

%20Desk%20Reference&f=false

[10] Parish, C., Batchelor, D., Progl, C. and Russell, P. (2007) Tutorial: Electron Beam-Induced Current in the Scanning Electron Microscope. *Microscopy and Analysis*, **21**, 11-13.

[11] Beck, F. and Wilson, S.S. (1998) Integrated Circuit Failure Analysis: A Guide to Preparation Techniques. John Wiley & Sons, Hoboken, 57-77.

[12] Kulkarni, M.S. (2003) A Review and Unifying Analysis of Defect Decoration and Surface Polishing by Chemical Etching in Silicon Processing. *Industrial & Engineering Chemistry Research*, **42**, 2558-2588. http://dx.doi.org/10.1021/ie020716y

[13] Mills, T. and Sponheimer, E.W. (1982) Precision VLSI Cross-Sectioning and Staining. 20*th Annual Reliability Physics Symposium*, San Diego, March 1982, 214-220.

[14] Hu, S.M. and Kerr, D.R. (1967) Observation of Etching of *n*-Type Silicon in Aqueous HF Solutions. *Journal of the Electrochemical Society*, **114**, 414. http://dx.doi.org/10.1149/1.2426612

[15] Madou, M.J. (2009) Manufacturing Techniques for Microfabrication and Nanotechnology. CRC Press, Boca Raton, 240.

[16] Subramanyan, R., Massoud, H.Z. and Fair, R.B. (1988) Accurate Junction Depth Measurements Using Chemical Staining, Semiconductor Fabrication: Technology and Metrology. ASTM STP, Philadelphia, 990. https://books.google.fr/books?id=4GacVDYcoi8C&pg=PA126&lpg=PA126&dq=subrahmanyan+junction+massoud&source=bl&ots=kGbZBgF9xV&sig=RPDsxoduazsRXXo8JUz_p-toXxc&hl=fr&sa=X&ved=0ahUKEwjoscb1_rHNAhUC0xoKHVVWCCcQ6AEIJjAA#v=onepage&q=subrahmanyan%20junction%20massoud&f=false

[17] Spinella, C. (1997) Chemical and Electrochemical Staining for Two-Dimensional Dopant Concentration Profiling on ULSI Silicon Devices. *MRS Proceedings*, **469**, 323. http://dx.doi.org/10.1557/proc-469-323

[18] Wu, C.P., Douglas, E.C., Mueller, C.W. and Williams, R. (1979) Techniques for Lapping and Staining Ion-Implanted Layers. *Journal of the Electrochemical Society*, **126**, 1982-1988. http://dx.doi.org/10.1149/1.2128839

[19] Lehmann, V. (2002) Electrochemistry of Silicon, Instrumentation, Science, Materials and Applications. Wiley-Vch, Weinheim.

[20] Nizou, S., Vervisch, V., Etienne, H., Ziti, M., Torregrosa, F., Roux, L., Roy, M. and Alquier, D. (2006) Deep Trench Doping by Plasma Immersion Ion Implantation in Silicon. *AIP Conference Proceedings*, **866**, 229-234. http://dx.doi.org/10.1063/1.2401501

[21] Yamauchi, T., Tsumori, Y., Nakashizu, T., Esaka, H., Takao, S. and Shinoyama, S. (1992) Application of Copper-Decoration Method to Characterize As-Grown Czochralski-Silicon. *Japanese Journal of Applied Physics*, **31**, L439. http://dx.doi.org/10.1143/JJAP.31.L439

[22] Yamashita, O. (2004) Effect of Metal Electrode on Seebeck Coefficient of *p*- and *n*-Type Si Thermoelectric. *Journal of Applied Physics*, **95**, 178-183. http://dx.doi.org/10.1063/1.1630361

[23] Wagner, M. (2007) Simulation of Thermoelectric Devices. Ph.D. Thesis, Vienna University, Austria. http://www.iue.tuwien.ac.at/phd/mwagner/

[24] Hontgas, C.H. (2007) Investigation of PN Junction Delineation Resolution Using Electron Beam Induced Current. Ph.D. Thesis, University of Central Florida, Orlando.

[25] Peng, L.-M., Chen, Q., Liang, X.L., Gao, S., Wang, J.Y., Kleindiek, S. and Tai, S.W. (2004) Performing Probe Experiments in the SEM. *Micron*, **35**, 495-502.

[26] Sealy, C.P., Castell, M.R. and Wilshaw, P.R. (2000) Mechanisms for Secondary Electron Dopant Contrast in the SEM. *Journal of Electron Microscopy*, **49**, 311-321. http://dx.doi.org/10.1093/oxfordjournals.jmicro.a023811

[27] Chee, A.K.W., Broom, R.F., Humphreys, C.J. and Bosch, E.G.T. (2011) A Quantitative Model for Doping Contrast in the Scanning Electron Microscope Using Calculated Potential Distributions and Monte Carlo Simulations. *Journal of Applied Physics*, **109**, 013109. http://dx.doi.org/10.1063/1.3524186

[28] Buzzo, M., Ciappa, M., Millan, J., Godignon, P. and Fichtner, W. (2007) Two-Dimensional Dopant Imaging of Silicon Carbide Devices by Secondary Electron Potential Contrast. *Microelectronic Engineering*, **84**, 413-417. http://dx.doi.org/10.1016/j.mee.2006.10.055

[29] Buzzo, M., Ciappa, M. and Fichtner, W. (2006) Imaging and Dopant Profiling of Silicon Carbide Devices by Secondary Electron Dopant Contrast. *IEEE Transactions on Device and Materials Reliability*, **6**, 203-212. http://dx.doi.org/10.1109/TDMR.2006.876605

[30] Hyun, M.S., Yoo, J.H., Kwak, N.-Y., Kim, W., Rhee, C.K. and Yang, J.-M. (2012) Precise Comparison of Two Dimensional Dopant Profiles Measured by Low Voltage Scanning Electron Microscopy and Electron Holography Techniques. *Applied Microscopy*, **42**, 158-163.

[31] Buzzo, M., Ciappa, M., Stangoni, M. and Fichtner, W. (2005) Two-Dimensional Dopant Profiling and Imaging of 4H

Silicon Carbide Devices by Secondary Electron Potential Contrast. *Microelectronics Reliability*, **45**, 1499-1504. http://dx.doi.org/10.1016/j.microrel.2005.07.069

[32] Glowacki, A. and Boit, C. (2005) Characterization of Thermoelectric Devices in ICS as Stimulated by a Scanning Laser Beam. 43*rd Annual IEEE International Reliability Physics Symposium*, San Jose, 17-21 April 2005, 450-457.

[33] Zhuang, D. and Edgar, J.H. (2005) Wet Etching of GaN, AlN, and SiC: A Review. *Materials Science and Engineering*: *R*: *Reports*, **48**, 1-46. http://dx.doi.org/10.1016/j.mser.2004.11.002

[34] Hsieh, Y.W., Russell, J.D. and Chen, P.Y. (2008) SEM Si Doping Contrast Enhancement Using Sample Charging. *ISTFA*, Portland, 2-6 November 2008, 510-514.

[35] Kazemian, P., Mentink, S.A., Rodenburg, C. and Humphreys, C.J. (2007) Quantitative Secondary Electron Energy Filtering in a Scanning Electron Microscope and Its Applications. *Ultramicroscopy*, **107**, 140-150. http://dx.doi.org/10.1016/j.ultramic.2006.06.003

[36] Ong, V.K.S. and Wu, D. (2001) Determination of Diffusion Length from within a Confined Region with the Use of EBIC. *IEEE Transactions on Electron Devices*, **48**, 332-337. http://dx.doi.org/10.1109/16.902735

[37] Elliot, S.L., Broom, R.F. and Humphreys, C.J. (2002) Dopant Profiling with the Scanning Electron Microscope—A Study of Si. *Journal of Applied Physics*, **91**, 9116-9122. http://dx.doi.org/10.1063/1.1476968

[38] Tsurumi, D., Hamada, K. and Kawasaki, Y. (2012) Energy-Filtered Secondary-Electron Imaging for Nanoscale Dopant Mapping by Applying a Reverse Bias Voltage. *Japanese Journal of Applied Physics*, **51**, 106503. http://dx.doi.org/10.7567/JJAP.51.106503