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Effect of Sub-Grains and Crystal Defects on Monolike Si Solar Cell Performance

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ABSTRACT

This paper investigates crystalline orientation in monolike silicon wafers and its effect on solar cell performance. Monolike silicon wafers from two different bricks cut from interior and corner region of an ingot were compared. The mono grain in the interior brick is nearly perfect, but there are some large oblong shaped sub-grains in the corner brick. The large sub-grains at corner brick wafers are oriented at (311), instead of (100) orientation. The (311) grains contain high density of dislocation and cannot be effectively textured by alkaline solution, therefore lowering the cell efficiency significantly. There is about 0.86% (abs) cell efficiency reduction on the monolike cells that contain large sub-grains.

Keywords: Monolike; Defects; Grain Orientation; Cell Efficiency

1. Introduction

Cast monolike silicon solar cells are a new type of photovoltaic (PV) cell that has drawn a lot of attention in PV industry recently [1-3]. Instead of pulling single crystalline silicon by Czochralski method, single crystalline silicon is grown from the melt by casting in monolike silicon wafers. The cast monolike silicon has an advantage of high cell efficiency close to cells made on Cz wafers, but at a cost similar to that of multicrystalline silicon wafers. There has been significant progress in monolike cell technology in the past few years. Cell efficiency of ~20% has been reported for the monolike cells fabricated with standard cell processing techniques [4]. It is anticipated that the efficiency of monolike cells can be further improved after optimizing cell processes [5].

Monolike silicon wafers are grown by casting from a seeded layer at the bottom of the crucible by heat exchange method [1,6]. Ideally, silicon grows vertically from bottom up in the same (100) orientation as the seeded layer, therefore creating single crystalline structure. However, due to the fast cooling at crucible walls, random nucleation may happen near the crucible walls, forming multicrystalline silicon around the perimeter of the ingots. Additionally, there may be silicon grains nucleated from the seed interfaces. The multicrystalline grains in the monolike silicon wafers degrade the wafer quality and bring up challenges in cell processing. For examples, the multicrystalline grain regions cannot be effectively textured with conventional alkaline solution. Variations in multicrystalline grain areas will also lead to a wide range of cell efficiency in a production line. It is therefore critical to control the non-mono grain regions and to optimize monolike cell process. In this paper, we study the crystalline structure of monolike silicon and its effect on cell performance.

2. Experimental Methods

Monolike silicon wafers of 156×156 mm^2 were withdrawn from different locations, an interior and a corner, of a large industrial ingot (840×840 mm^2). Wafers were cut by diamond wire sawing to a nominal thickness of 200 μm.

Solar cells were processed with a standard full aluminum back surface field (Al BSF) technology. First, wafers were treated in heated KOH solution to remove up to 5 μm sawing damage layer followed by KOH/IPA solution for texturing. After cleaning with 10% HF and 20% HCl solution, wafers were processed with phosphorous diffusion in a POCl$_3$ tube furnace for a final sheet resistance of 65 Ω/sq followed by edge-isolated in acid solution and cleaning in 10% HF to remove phosphosilicate glass (PSG). Cells were coated with ~80 nm SiN$_x$ antireflection layer in a low frequency PECVD reactor. Electrical contacts were screen printed with DuPont PV17F Ag paste for front gridline and Monocrystal PASE-1203 Al paste for rear contact. The cell contacts were finally fired in TPSolar IR belt furnace.

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Cell efficiency was measured by an automated I-V tester. Cell internal quantum efficiency (IQE) was determined by combination of wavelength-dependent spectral response and external surface reflectance measurements. Cells were further evaluated by a scanning Kelvin probe system assisted with local illumination [7]. The Kelvin probe is a non-contact, non-destructive method for measuring surface potential of a material. With a spot illumination, the Kelvin probe measurement provides local surface potential that is similar to an open circuit voltage (V_{OC}) at a small spot size. A map of surface potential distribution can indicate local variation in cell performance. The I-V test was taken at 1sun condition with Xe lamp, and the Kelvin probe was analyzed at an intensity of 100 mW/cm^2 with 30 mm^2 spot size. Solar cell performance was modeled using PC1D solar cell modeling software [8]. Inputs for modeling include phosphorus diffusion profile measured by spreading resistance analysis (SRA) as well as cell IQE and external reflectance curves.

Crystalline silicon structures from different grains in monolike silicon wafers were measured by X-ray diffractometer. Dislocation densities were further analyzed by optical microscopy after polishing and etched by Yang etching [9]. Surface textures were also analyzed by optical microscopy and the surface topography was measured by white light interferometer.

3. Results and Discussions

A series of monolike wafers were processed with standard Al BSF technology. **Figure 1** shows a comparison of average cell efficiency and V_{OC} for two different cells from interior and corner bricks. It can be seen that there is a clear difference in cell performance. A higher efficiency and also higher V_{OC} is observed on the interior brick cells, but a lower efficiency and lower V_{OC} on the corner brick cells. The average cell efficiency is 17.42% for the interior cells, and 16.56% for the corner cells. There is a 0.86% (absolute) difference between the two types of cells. The V_{OC} has a similar trend, with 623 mV for the interior cells and 618 mV for the corner cells.

As the V_{OC} represents an average value of full-sized cells which cannot show a spatial variation, therefore full-sized cells were further measured by a scanning Kelvin probe system. **Figure 2** shows the representative surface potential maps and their corresponding optical images for the two cell types. It can be seen that there is a higher and more uniform surface potential distribution on the interior brick cells (**Figure 2(a)**), but a lower and non-uniform distribution on the corner brick cells (**Figure 2(b)**). In fact, the corner brick cells exhibit a very low surface potential on a large portion (lower half) of the cells. Comparing to the optical images in **Figures 2(c)** and **(d)**, it can be seen that there is a good match be-
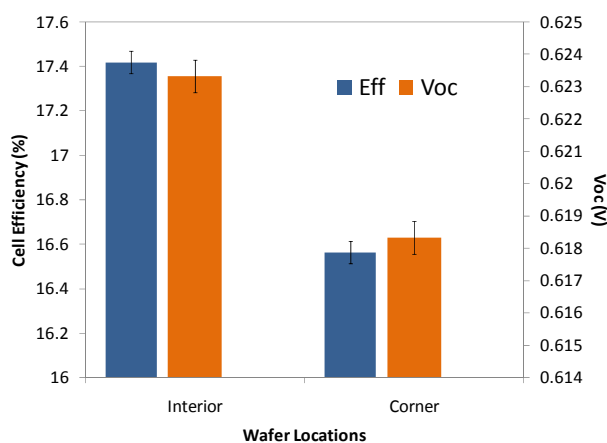

**Figure 1. Comparison of cell efficiency and V_{OC} of cells from an interior and a corner bricks.**

tween the grain structure and surface potential. Grain structures vary by wafer location. The sub-grains on the interior brick cells (**Figure 2(c)**) are relatively small and have almost no effect on the surface potential. On the other side, there are several large oblong shaped sub-grains on the corner brick (**Figure 2(d)**), which affect the surface potential greatly. Large sub-grains show a much lower surface potential than the majority of the mono grain region.

The reasons for surface potential variation were analyzed by X-ray and dislocation density measurements. It is found that the mono grain has exactly the same crystalline orientation as silicon seeds at (100) orientation, but the sub-grains on the corner brick wafers are mostly (311) orientated. It is also found that several large (311) grains are closely packed but separated by the grains with seed orientation. It can be seen that the (311) orientation is outgrown from (100) surface. The special (311) grain orientation from the Si seed is interesting. Generally, it is known that there are several favorable growth orientations, such as (100), (110), (111), (311) and (533), in the cast multicrystalline silicon wafers [10,11]. However, there are only fewer growth orientations in the monolike wafers. The limited growth orientation is important for monolike wafers, but it may also create some large sub-grains on the wafers, as shown in **Figure 2(d)**.

The dislocation densities at different grains are measured by optical microscopy after polishing and etching. **Figure 3** shows the dislocation pit images at various regions. Generally, the dislocation density is fairly uniform within grain, but significantly different from grain to grain. There is a very low density of dislocations in the (100) grain (**Figure 3(a)**), but a high density of dislocations in the (311) grain (**Figure 3(c)**). There is also a sharp transition of dislocation density at the grain boundary (**Figure 3(b)**). It is clear that the dislocation density is highly related to the grain orientations. Certain grain

(a)

(b)

(c)

(d)
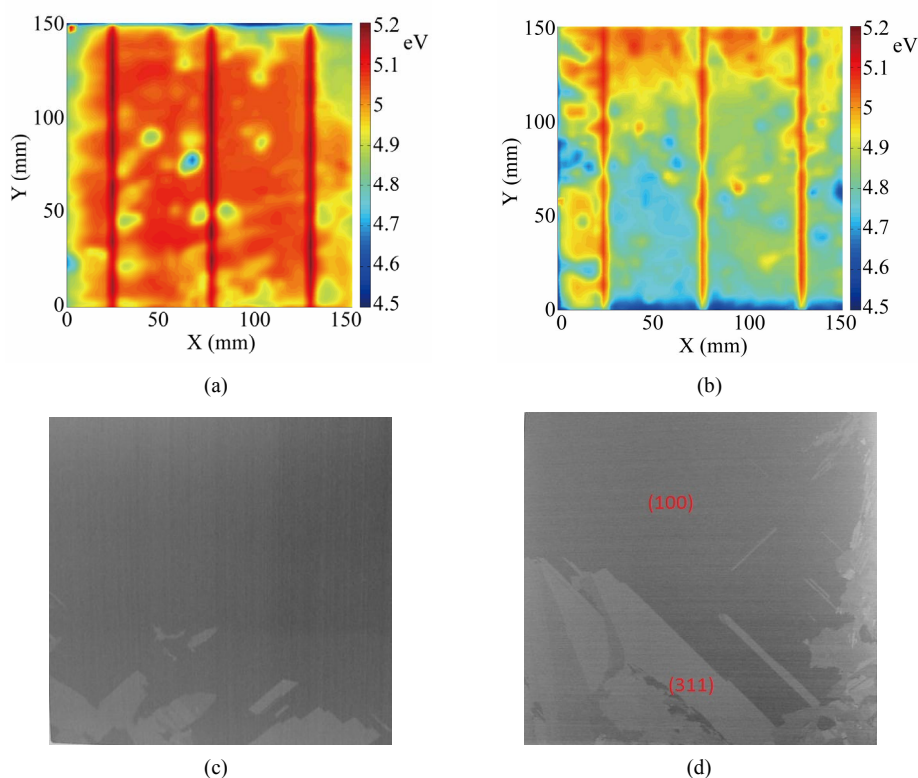
Figure 2. Representative surface potential maps for (a) interior brick cells and (b) corner brick cells, and (c) and (d) their corresponding optical images.

(a)

(b)

(c)
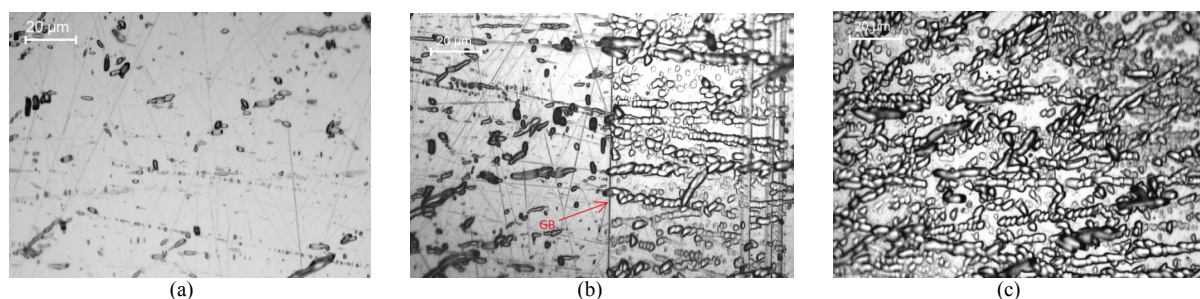
Figure 3. Optical images of dislocation pits at (a) (100) grain; (b) (100)/(311) grain boundary, and (c) (311) grain.

orientation tends to encompass more dislocations than others.

Figure 4 shows the surface textures for different grains. After alkaline texturing, there are many small but uniform pyramid-type structures on the (100) grain (**Figure 4(a)**). However, there are only long shingle or leaf-like structures on the (311) grains (**Figure 4(b)**). All etched shingle surfaces tilt in the same orientation. Surface topographical measurements indicate there is a 8 μm peak to valley height variation and also approximately 14˚ inclined angle on the etched surface (**Figure 4(c)**). All ridges and troughs are located in the same zones but separated in a certain distance. The repeated ridges and troughs are probably related to the special pattern created by the diamond wire sawing process in the silicon

wafering. The long shingle surface is created by anisotropic etching in alkaline solution. It is known that the alkaline etch is highly selective for crystalline silicon, and the ratio of etch selectivity can be up to 600 for the (100)/(111) orientations and 400 for (110)/(111) orientations [12]. Due to this etch selectivity, pyramid texture structures can be formed on (100) type wafers, but perpendicular trenches are created on (110) type wafers. The long shingle structure is therefore the outcome of selective etch along (110) plane surface. Since the original surface is (311) oriented, the etched surface is then inclined to the top surface. The large planar surface in this case is obviously undesirable to cell performance due to its high reflectivity.

The effect of dislocation and texture on the cell per-
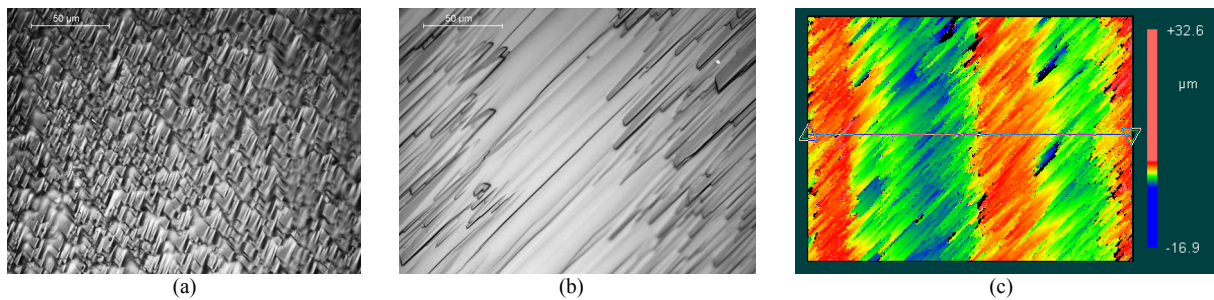
Figure 4. Optical images of textured surfaces for (a) (100) surface; (b) (311) surface, and (c) surface topographical map on (311) surface.

formance is simulated by PC1D. Two representative cells from the interior and corner bricks were chosen for modeling. There are four distinct cell regions that may be classified which have individual effects on cell performance. Monolike silicon wafers may have 1) (100) oriented, textured single crystalline regions; 2) (100) oriented, textured single crystalline regions displaying dislocation patterns; 3) (311) oriented, planar single crystalline regions; and 4) planar, multicrystalline regions possessing many crystal orientations. Inspection of the representative interior brick cell reveals the following region ratio: 70% region 1, 15% region 2, and 15% region 3. Similar inspection of the representative corner brick cell reveals the following ratio: 36% region 1, 25%, region 2, 22% region 3, and 17% region 4. IQE and external surface reflectance curves were collected for each region of the representative cells and are shown in **Figure 5**. Qualitative inspection of IQE curves shows that regions 2 and 4 have significant degradation of long wavelength response which may be consistent with low minority carrier bulk lifetime (τ_{bulk}). Low surface reflectance is necessary for efficiency light trapping and high short circuit current (J_{SC}). Comparison of textured and planar external surface reflectance curves shows a large difference in light trapping especially at short and long wavelengths. No difference in external surface reflectance was observed comparing textured regions 1 and 2 or planar regions 3 and 4, respectively. Thus, curves representing the difference between textured and planar regions are compared.

Short and long wavelength IQE fitting using PC1D is necessary to derive the front and back surface recombination velocities (FSRV and BSRV, respectively) for accurate modeling of solar cell current and voltage parameters. FSRV is influenced by emitter quality and front surface passivation while BSRV is influenced by Al-BSF quality and τ_{bulk}. Using PC1D, BSRV is only accurate when τ_{bulk} is known. The variable defect densities observed for monolike wafers indicates that τ_{bulk} will also vary widely across the wafer. In order to model this variation in τ_{bulk} for the monolike Si wafers, BSRV is derived for a control cell made on Czochralski-grown Si
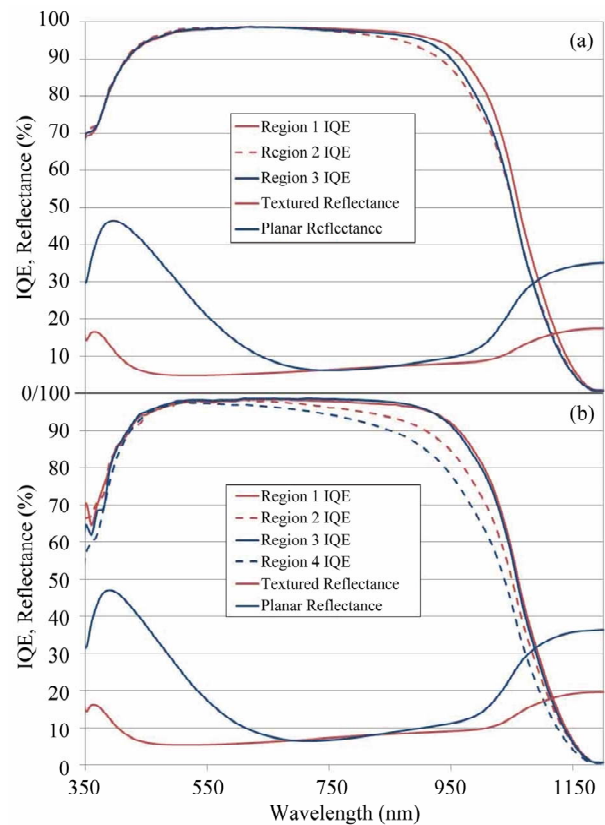
Figure 5. IQE and external surface reflectance curves collected for each region identified in (a) interior and (b) corner brick cells.

wafer with a known final τ_{bulk} and this value for BSRV is applied to the monolike cells. The modeled Czochralski cell was processed identically to the monolike cells, receiving the same front surface texture, phosphorus diffusion, and SiN$_x$ antireflection coating. The Czochralski cell was printed with the same Ag and Al metallization pastes and fired at the same peak wafer temperature. Final τ_{bulk} for this device was 250 µs, and IQE fitting using PC1D revealed a BSRV of 330 cm/s. Using the SRA profile for phosphorus-diffused emitter, FSRV was determined at 1.1 E5 cm/s. The combination of these parameters leads to an accurate determination of final V$_{OC}$,

J_{SC}, and efficiency for this device, which matched the experimental I-V data. Since the Czochralski cell and the monolike cells were processed identically, the value of 330 cm/s BSRV was applied to determine local variation in τ_{bulk} for the representative monolike cells modeled here.

Table 1 summarizes the PC1D modeling parameters derived from fitting IQE curves of **Figure 5**. Goodness of fit was determined based on minimization of error between experimental and PC1D calculated IQE curves between 400 and 600 nm for FSRV and between 700 and 1100 nm for BSRV and τ_{bulk}. Based on fixed BSRV of 330 cm/s, the value for τ_{bulk} which minimized fitting error is shown for each region of the interior and corner brick cells. In order to understand the impact of each cell region identified above, modeled current, voltage, and efficiency are shown for each region based on PC1D modeling inputs. The modeled I-V parameters for each cell region simulate a hypothetical cell made exclusively of material characteristic of individual regions. The large difference in τ_{bulk} for each region has a direct impact on hypothetical cell performance. In **Table 2**, modeled and experimental I-V parameters are compared for each cell type. The modeled parameters are calculated from summation of parameters derived in **Table 1** accounting for the areal contribution of each region. Agreement between experimental and modeled I-V parameters in **Table 2** validates the model inputs.

Table 1. PC1D modeling parameters for monolike cells from interior and corner brick regions.

Ingot Position	Wafer Region	τ_{bulk} (μs)	V_{OC} (mV)	J_{SC} (mA/cm^2)	Eff. (%)[a]
Interior	1 (70%)	125	626	36.8	18.0
	2 (15%)	20	610	36.1	17.4
	3 (15%)	40	613	33.0	16.0
Corner	1 (36%)	70	624	36.4	17.6
	2 (25%)	13	611	35.3	16.7
	3 (22%)	70	621	33.4	16.1
	4 (17%)	7	602	31.6	14.8

Fixed PC1D Inputs	
Bulk Resistivity/Thickness	1 Ω-cm; 180 μm
Back Surface Reflectance	63%
Series Resistance	0.8 - 0.9 Ω-cm^2
FSRV/BSRV	1.1 E5 cm/s; 330 cm/s
Emitter Profile	SRA measured input
Ext. Surface Reflectance	Experimental

[a]Based on fill factor of 78.3% for interior cell and 77.5% for corner cell.

Table 2. Comparison of modeled and experimental V_{OC}, J_{SC}, and efficiency for monolike cells from interior and corner brick regions.

Ingot Position	Data Origin	V_{OC} (mV)	J_{SC} (mA/cm^2)	Eff. (%)[a]
Interior	Modeled	621	36.1	17.6
	Experimental	624	35.8	17.5
Corner	Modeled	616	36.4	16.6
	Experimental	619	36.4	16.6

[a]Based on fill factor of 78.3% for interior cell and 77.5% for corner cell.

Monolike silicon wafers are a new type of wafers which shows a high promise for solar cell manufacturing. Specially oriented silicon wafers can be created from a seeded growth technology. However, some unfavorable multicrystalline may be also formed on monolike silicon wafers. Our results clearly indicate the detrimental effect of non-mono grains on the monolike silicon cells. There is no standard classification method for monolike silicon wafers yet, but it's highly desirable to have over 90% monolike region on the monolike wafers [10]. A large variation in the percentage ratio of multicrystalline grain regions will further increase cell efficiency distribution in a production line. It should be noted that effect of multicrystalline grains may be alleviated by an optimized texturing. Generally, an alkaline solution is used to texture (100) oriented single crystalline silicon wafers, and acidic solution for multicrystalline silicon wafers. For monolike silicon wafers which contain a majority of (100) grain, an alkaline texturing may be still appropriate. However, if there is a significant amount of non-mono grains on the wafers, a texturing optimization that includes a two-step texturing or some other special chemical [13] may be required.

4. Conclusion

The cell efficiency of monolike silicon solar cells is affected by the multicrystalline grain regions, especially the (311) oriented grains. There is relatively low density of dislocations in the mono (100) grain, but a significant higher density of dislocation in (311) grains. The (311) grains result in long leaf-like or shingle surface after alkaline texturing. PC1D modeling indicates a large variation in τ_{bulk} across monolike silicon wafer surface most likely due to variation in dislocation density. Both dislocation and large planar surface affect the cell efficiency by 0.86% (abs) decrease compared to the cells fabricated on more uniform mono wafers.

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