Journal of Power and Energy Engineering, **2014, 2, 1-10**
Published Online February 2014 (http://www.scirp.org/journal/jpee)
http://dx.doi.org/10.4236/jpee.2014.22001

Scientific Research

Paralleled DC-DC Power Converters Sliding Mode Control with Dual Stages Design

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Received December 27th, 2013; revised January 27th, 2014; accepted February 4th, 2014

ABSTRACT

This paper proposes the new cascaded series parallel design for improved dynamic performance of DC-DC buck boost converters by a new Sliding Mode Control (SMC) method. The converter is controlled using Sliding Mode Control method that utilizes the converter's duty ratio to determine the skidding surface. System modeling and simulation results are presented. The results also showed an improved overall performance over typical PID controller, and there was no overshoot or settling time, tracking the desired output nicely. Improved converter performance and robustness were expected.

KEYWORDS

DC-DC Converters; Paralleled Converter; DC-DC Control; Efficiency Improvement of DC-DC; Sliding Mode Control (SMC); Hyper Plane Design; Variable Structure Control (VSC)

1. Introduction

Power electronics is the process and control of the flow of electric energy from a given source to a load in a shape that is optimally suited for its use. Modern electric systems demand high quality, reliable, efficient and light weight power supplies.

Higher power converters, such as the ones used in Electrified Vehicles (EVs) and aircraft power units, are also in increase demand as a result of the green acts taken on by many countries. The improvement in power switching devices such as the IGBTs and MOSFETs made the power electronics more appealing to many applications. Higher switching frequency, higher power capability and improved efficiency are the main reasons for the expanded application [1].

Paralleled DC-DC converters are used in telecommunication industry widely and operated under closed loop control to regulate the output voltage [2]. The nonlinearities of the DC-DC converters are due to interaction among the converter components and the switching nonlinearity behaviors. However, linearized average model is commonly used for converter analysis [3-9]. A drawback of the linearized model is that it cannot predict the dynamics of the converter in a saturation region [2]. For standalone converters, many nonlinear control approaches have been studied and proposed: Lyapunov based controllers [10-13], variable structure controllers VSC [14-16], feedback linearization method [17] and Fuzzy logic controllers [18]. In [19], the sliding mode control is used and the results are shown for all types of converters (Buck, Boost and Buck-Boost). The results of this type of control where the state space averaging is applied to sliding mode control PWM converters, showed a good result but high ripple content on the buck-boost converter.

For paralleled DC-DC converters control, [2] proposed an Integral Variable Structure Control (IVSC) for N paralleled DC-DC converters. They emphasized that Variable Structure Control was a natural choice since the control and the plant are both discontinuous and have uncertainties. A fuzzy logic controller is proposed in [18] for the master slave concept of the DC-DC control, and the results showed robust and improved performance over classical linear control. In [20], the control is based on a steady-state DC model and a small-signal model, which showed that current sharing can be achieved without a

dedicated current sharing controller. [21-43] explored many of the concepts mentioned above and some of the chaotic behaviors of the converters. The papers are added for the readers' convenience to further explore the concept of the DC-DC converter control and behavior.

In this paper, we will introduce a concept to improve the output quality and simplify the paralleled converters control to a simple single like converter. We will use a Sliding Mode Controller (SMC) with the Variable Structure Surface Design concept developed in [44] to control the converter. A comparison with a PID controller is presented.

2. Modeling of Buck Boost Converter

In this section a model for N paralleled buck boost converters to supply a common load is developed. **Figure 1** shows a commonly used buck-boost configuration for paralleled converters supporting a single load.

This paper will introduce a new approach to controlling the converter to reduce the output harmonics and simplify the control to an equivalent of a single converter. First a single converter model is given by the following equations:

$$\dot{i}_l = (1-s_1)\frac{v_c}{L} + \frac{S_1}{L}E \tag{1}$$

$$\dot{v}_c = -(1-s_1)\frac{i_l}{C} - \frac{v_c}{RC} \tag{2}$$

The above equations show the model that the first section of the converter associated with, the switch s_1 takes on the values $[0\,1]$. The current is the inductor current associated with the first inductor L_1 and V_C is the capacitor voltage as a result of the contribution of all other converters. For multi converters the output current i_o is the sum of all individual inductor currents and is given by the following equation.

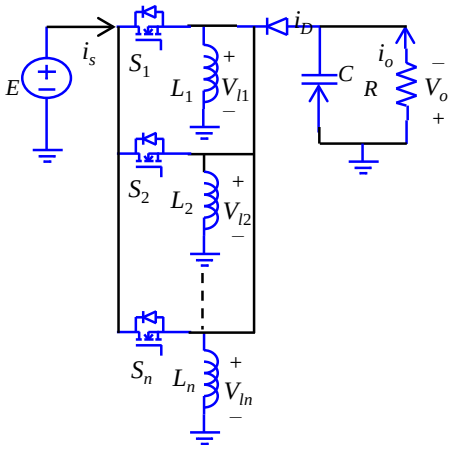

Figure 1. Paralleled buck-boost converter.

$$i_o = \sum_{n=1}^{m} i_{ln} - i_c \tag{3}$$

The states are the inductor currents and capacitor voltage as shown in Equation (4).

$$x = \left[i_{ln} v_c\right]^T, n = 1, 2, \cdots, m \tag{4}$$

m: number of converters

Using Equation (3) and based on Equations (1) and (2) we can formulate the following relation. Given that the capacitor voltage is the same as the output voltage $V_c = V_o$.

The derivative of the output current given by Equation (3) is shown in Equation (5)

$$\dot{i}_o = \dot{i}_{l1} + \dot{i}_{l2} + \cdots + \dot{i}_{lm} - \dot{i}_c \tag{5}$$

Substituting Equation (1) into Equation (5) and collecting the terms we get Equation (6) interim of the derivative of the load and capacitor currents.

$$\dot{i}_o = \frac{v_c}{l}\left(\sum_{n=1}^{m}(1-s_n)\right) + \frac{E}{l}\left(\sum_{n=1}^{m}(s_n) - \dot{i}_c\right) \tag{6}$$

where S_n is the state of the n^{th} switch.

We determine from **Figure 1** that the output voltage is equivalent to the capacitor voltage and the relation can be written in Equation (7)

$$v_c = v_o = i_o R \tag{7}$$

Taking the derivative of Equation (7) we get the following relation

$$\begin{aligned}\dot{v}_c &= \frac{Rv_c}{l}\left(\sum_{n=1}^{m}(1-s_n)\right) + \frac{RE}{l}\left(\sum_{n=1}^{m}(s_n) - \dot{i}_c\right) \\ &= \frac{mRv_c}{l} + \sum_{n=1}^{m} s_n\left(\frac{ER}{l} - \frac{R}{l}v_c\right) \\ &= \frac{mRv_c}{l} + \frac{R}{l}(E - v_c)\sum_{n=1}^{m} s_n\end{aligned} \tag{8}$$

With the advancement in switches and their higher switching frequency capabilities we assume an infinite switching frequency. With this assumption we can assume that the rate of change in the capacitor voltage and current are zero, solving Equation (8) we get the following Equation (9)

$$\sum_{n=1}^{m} s_n = m\frac{v_c}{v_c - E} \tag{9}$$

It can be seen that the second term of Equation (9) is related to the duty ratio (d) for the buck boost converter. The duty ration is defined as the turn on time as a percentage of the period defined as T.

$$d = \frac{t_{\text{on}}}{T} \tag{10}$$

Substituting the expression for d into Equation (9) we determine the switching time as follows

$$t_{on} = T\left(\frac{s_1}{m} + \frac{s_2}{m} + \cdots + \frac{s_m}{m}\right) \quad (11)$$

The above equation shows the distribution of the switching time for the m converters, the sum of all the switches contribution is equivalent to the duty ratio or the required on time of an equivalent single switch to provide the desired output. The contribution of each leg is an equal portion of the required output voltage and current.

The control methodology can vary from PID, VSC, Fuzzy logic, SMC or other methods, but the end results is the same as to determine the turn ON time for the switches.

Next an improved performance of the converter to reduce harmonics content is presented. It is proposed to do a harmonic cancelation by shifting the switching sequence of the converters, by imposing t_{delay} on the subsequent converter legs using the following relation

$$t_{\text{delay}}(k) = t_d * \frac{(k-1)}{m} \quad (12)$$

t_d : Delayed time factor (e.g. $10\,n\,sec$)
k : The specific converter $(1, 2, \cdots, m)$
m : Total number of converters $(2, 3, \cdots)$

3. Design of the New Converter Control

In this section we propose a new converter control design to simplify the overall control and improve performance. In DC-DC converters control, the principle is to eliminate the error between the actual output and the desired output value. The control action is taking by switching the control device in this case a MOSFET to apply the input DC voltage to the converter periodically and proportional to the error. In this paper we propose separating the converter into two stages as discussed next.

The design consists of two cascaded stages where the first stage is the control stage shown in **Figure 2** enclosed by the dashed lines and the second stage called the performance stage.

The performance stage represents m number of parallel converters to be controlled to reduce the harmonics contents of the output. This separation gives the designer the freedom to choose the switching frequency to optimize the performance of the converter. This frequency is independent of the control stage and can be optimized.

The converters switching time is determined in advance and the frequency can be optimized to reduce switching losses or improve EMI performance. The simulation will show the performance of the converter with synchronized switching time and also the enhanced performance with the shifted switching time as suggested above in Equation (12).

The control stage as shown enclosed in the dashed line in **Figure 2** is used to control the input voltage to the paralleled converters. In previous converter designs the input voltage always assumed constant and the control was done by switching the converter at variable duty cycles to achieve the desired output values. In this paper we propose the idea of switching the output stage of the converter at an optimal switching frequency and duty cycle while controlling the input stage varying it to achieve the desired output value.

The control of the first stage through S_c, as shown in **Figure 3**, is designed with the assumption that the parallel converters have an equivalent inductor and capacitor values if the control method requires knowledge of the parameters. The control can be done using, Variable structure Control (VSC), SMC, where parameter sensitivity is not an issue, fuzzy logic, PID or any other method desired by implementation engineers as the problem is reduced to a single converter control.

4. Sliding Mode Control of the Converter

In this section we will use sliding mode control to control the converter. The sliding surface used is a unique duty cycle dependent surface developed in [44]. The controller then derived using the sliding surface coefficients. In [44] a Variable Structure Control (VSC) surface design for DC-DC power converters is presented. The design was done for the Buck boost converter and can be extended and applied to all types using the methodology explained in [44].

Consider the linear time invariant system given by

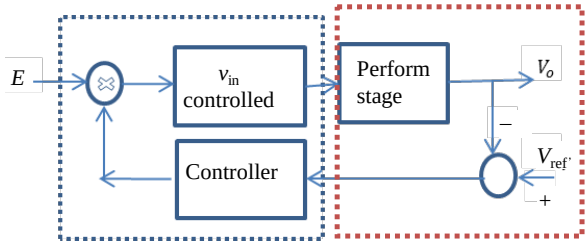

Figure 2. Two stages converter.

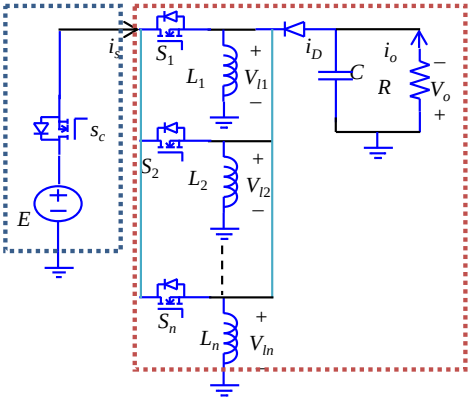

Figure 3. The proposed two stage converter.

Equation (13).

$$\dot{x}(t) = Ax(t) + B(x)u(t) \tag{13}$$

where,

$$x = \begin{bmatrix} x_1 & x_2 \end{bmatrix} = \begin{bmatrix} i_l & vc \end{bmatrix}$$

$$A = \begin{bmatrix} 0 & 1/L \\ -1/C & -1/RC \end{bmatrix};$$

$$B = \begin{bmatrix} \frac{V_{in} - v_c}{L} \\ \frac{i_l}{C} \end{bmatrix}$$

The states are defined as the inductor current and the capacitor voltage which the same as the output voltage.

Given the surface as defined in [14,15].

$$s(x) = Cx \tag{14}$$

taking the derivative of (14).

$$\dot{s}(x) = C\dot{x} \tag{15}$$

Using Equation (13) to Equation (15) we get the equivalent control discussed by Utkin [16,29]. It is developed to derive the sliding mode equations into the manifold $s(x) = 0$ and then the solution to $s(x) = 0$ is called the equivalent control u_{eq}.

$$u_{eq} = -(CB)^{-1} CAx \tag{16}$$

The method in [44] defines the surface in term of the duty cycle and the parameters of the DC-DC converters as in Equation (17).

$$S(x) = Qx_{1e} + Wx_{2e} \tag{17}$$

where

$$x_{1e} = (x_1 - x_{1ref})$$

$$x_{2e} = (x_2 - x_{2ref})$$

Are the errors between the actual values and the desired one. Taking the derivative of Equation (17) we find the value of C, the surface coefficients, as

$$\frac{dS}{dx} = C = \begin{bmatrix} Q & W \end{bmatrix} \tag{18}$$

Using the value of *C* in Equation (18) and the given *A* and *B* coefficients of the system and evaluating Equation (16) to get the equivalent control u_{eq}.

$$u_{eq} = \frac{\frac{W}{C}x_1 - \left(\frac{Q}{L} - \frac{W}{RC}\right)x_2}{\frac{Q}{L}(v_{in} - x_2) + \frac{Q}{C}x_1} \tag{19}$$

The total control of the system consists of two components the equivalent control u_{eq} and corrective control u_c, where the equivalent control is used to reach the surface while the corrective is to keep the system on the surface.

$$u = u_{eq} + u_c \tag{20}$$

For system stability, we need to guarantee the system ends up and stays at the surface regardless of the initial conditions. Using the following Lyapunov function:

$$V(x) = \frac{1}{2}S(x)^2 \tag{21}$$

We need to grantee that the derivative of Equation (21) is negative definite that is $\dot{V} < 0$ for all $S(x) \neq 0$, that from any initial condition. Taking the derivative of (21):

$$\dot{V} = S\dot{S} < 0 \tag{22}$$

With

$$\frac{dS}{dx} = C$$

and

$$\dot{S} = CAx + CBu$$

to grantee Equation (22) holds the corrective control u_c is chosen as follow.

$$u_c = -K \operatorname{sgn}(S) \tag{23}$$

where K is appositive number. Hence the complete control is given by Equation (20) is:

$$u_c = -u = \frac{\frac{W}{C}x_1 - \left(\frac{Q}{L} - \frac{W}{RC}\right)x_2}{\frac{Q}{L}(v_{in} - x_2) + \frac{Q}{C}x_1} - K \operatorname{sgn}(S) \tag{24}$$

where Q and W are the coefficients derived in [2] and given below:

$$Q = \frac{L}{d}$$

$$W = -\left\{ L * \left(\frac{Jdl}{L} - \frac{Cd(d-1)}{LR} + \frac{Cdl(d-1)}{LR} \right) * \left(\frac{C(d-1)}{R} - J + \frac{(d-1)^2}{CJL} \right) \right\} \Big/ \left\{ d * \left(\frac{Cd}{R} + \frac{dl(d-1)}{CJL} \right) * \left(\frac{(d-1)^2}{CL} - J + \frac{CJ(d-1)}{R} \right) \right\}$$

L : Inductor value

C : Capacitor value

R : Load Resistor Value

J : Associated Jordan value associated with the selected eigen values.

L and l: Arbitrary positive numbers

d : Duty ratio

In the next section we will show the results of the application of the hyper plane coefficients in the proposed two stage converter and compare to the results to a conventional PID controller. Although a comparison will show an improvement over the conventional method in term of overshoot and settling time, the main purpose of the application to test the feasibility of the method developed in [44] and introduce the proposed two stage converter.

Figure 4 shows a single Buck Boost converter. **Figure 5** shows paralleled buck boost converters. Both converters, the single or the paralleled are to regulate the output voltage to a desired value v_{ref} and provide loads with the desired currents. **Figure 6** shows the sliding mode controller as given by (24).

In the next section will show and compare the results of using a single converter, parallel converters, paralleled converters with the enhanced mode and the developed hyper plain coefficients method [44].

5. Results

The converter shown in **Figure 4** represent a single Buck Boost converter based on the mathematical model described in (1) and (2). The converter was controlled using a PID control and sliding mode control with the developed hyper plain coefficients and simulated using the following circuit parameters:

$$l = 10 \text{ mh}, C = 10 \text{ μF}, R = 10 \text{ Ω}, E = v_{in} = 50 \text{ V}$$

In the second part of the simulation, the converters are paralleled and the new two mode design is implemented. The same values as the single converter are used with a mismatch of 10% to represent a more realistic situation. However for sensitive applications more precise value components can be chosen. **Figure 5** shows the converters constructing a paralleled structure for the benefits mentioned earlier in the previous sections. The last part of the simulation was done using the delayed switching time as in (12) to further improve the performance.

First part of the simulation is of the single converters with the values given above. The results are shown below in **Figure 7**. The second part is the simulation **Figure 8** is for the paralleled converter with a fixed duty cycle for all the converters in the performance stage. The third part **Figure 9** is the results for the paralleled converters with the proposed switching delay as suggested by Equation (12).

Figure 7 shows the output voltage of a single converter regulated at 80 volts, the output is clearly showing the mount of ripple on the output voltage exceeds 5 V. The increase in the amount of ripples on the system voltage would cause increase losses reducing efficiency and can contribute to the mechanical wear and tear of a system.

Figure 8 shows the improved performance of the system by reducing the output voltage ripple to less than 1 V. This improvement is important as to increase system efficiency and improve its performance. In systems such as electric motors for example, this improvement can translate into increased reliability and reduction in maintenance cost.

Figure 9 shows further improvement in the sense of ripple reduction and more importantly significant reduction in harmonic content of the output. The use of the

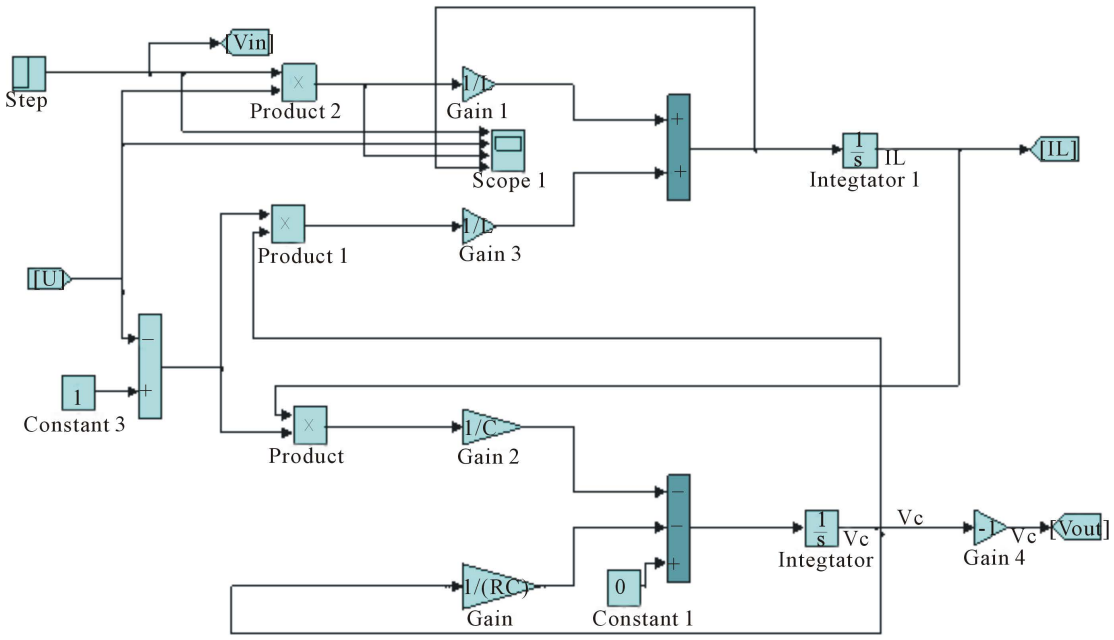

Figure 4. Simulink model of a single buck boost converter.

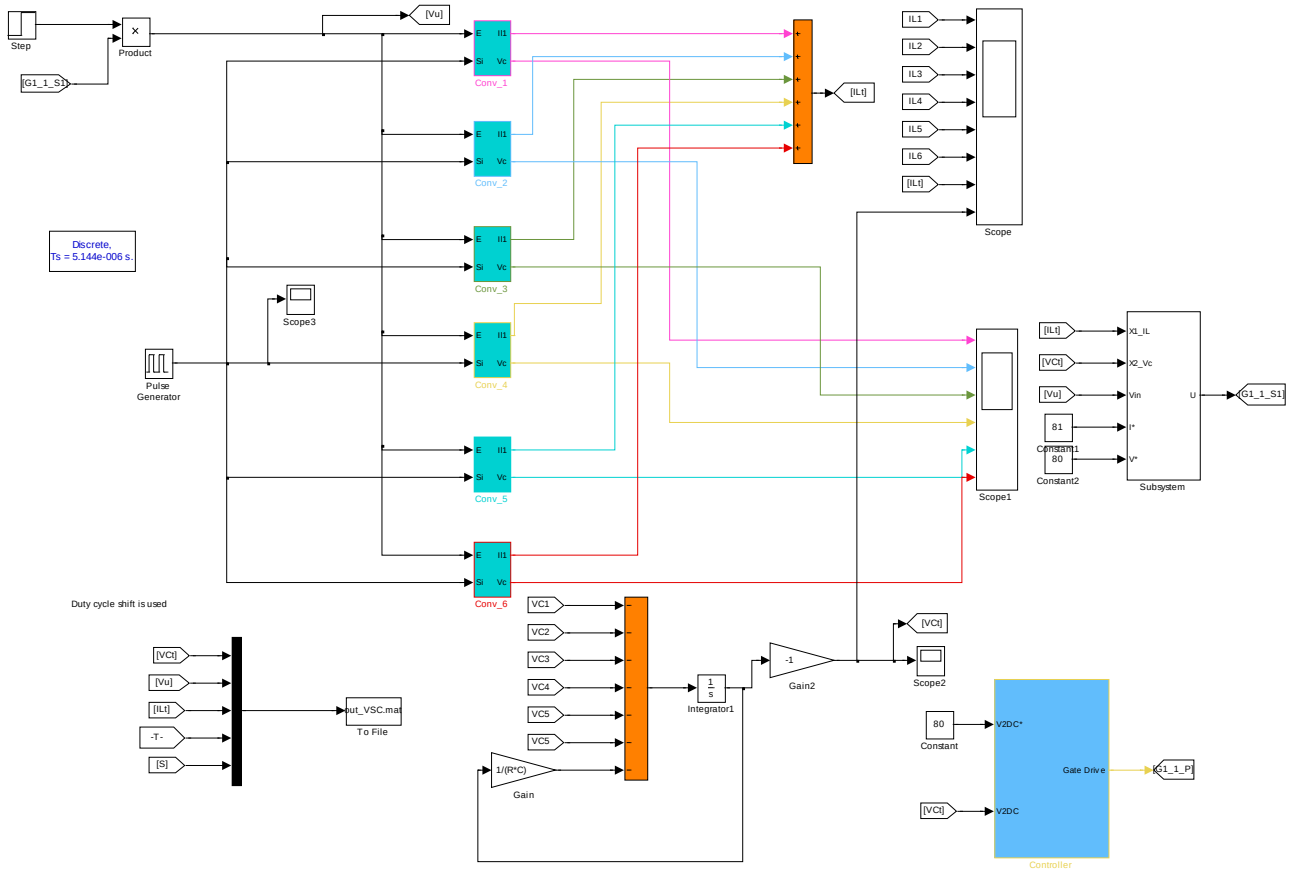

Figure 5. **Simulink model of six paralleled buck boost converters.**

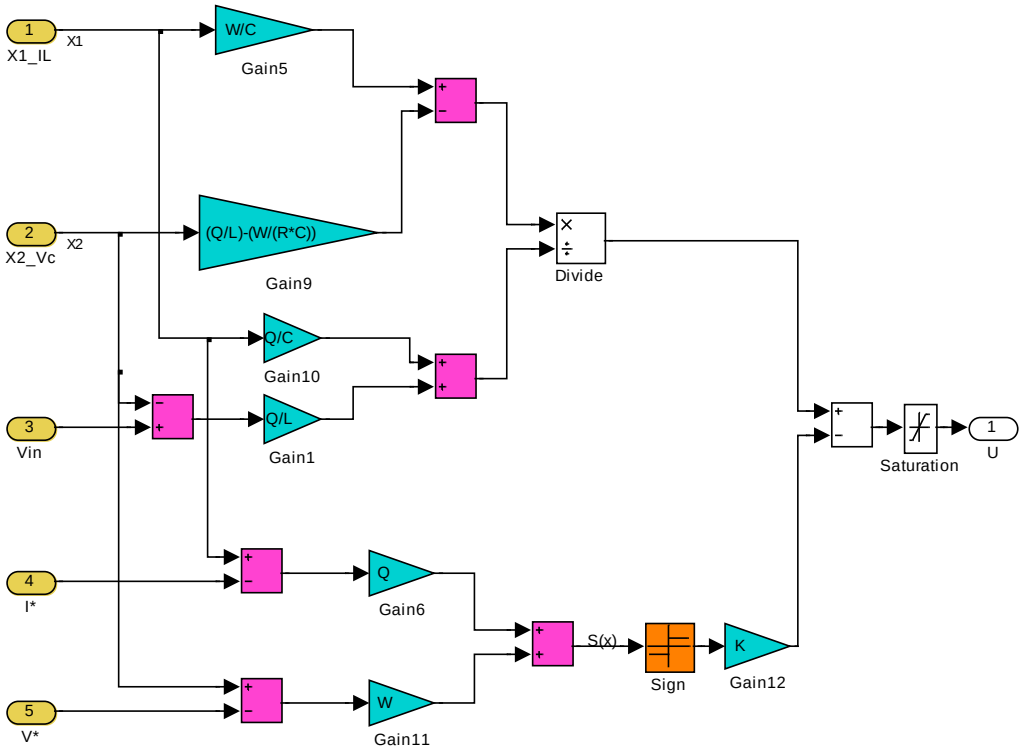

Figure 6. **Simulink model of the control circuit as given in Equation (24).**

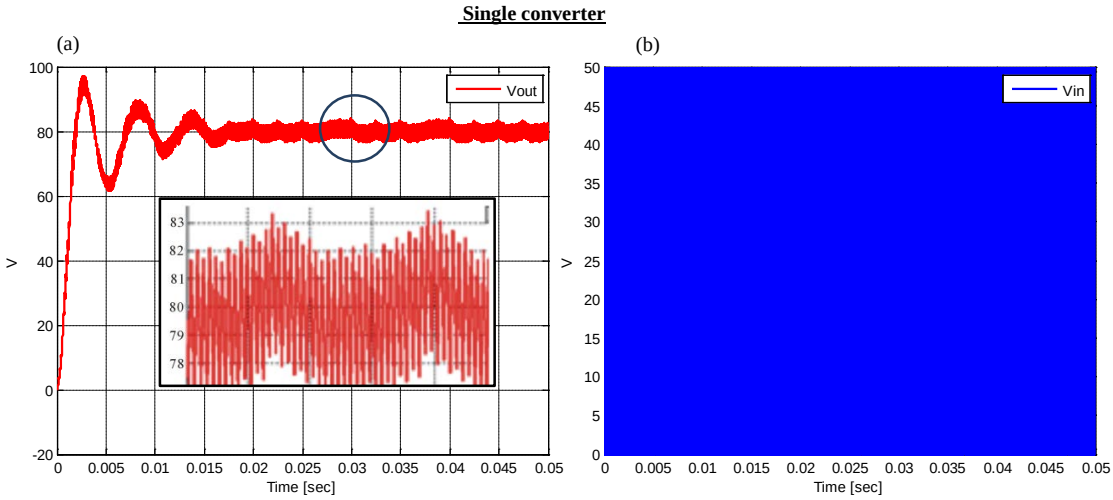

Figure 7. Output voltage, switched input voltage and a close-up of the output voltage of a single buck boost converter.

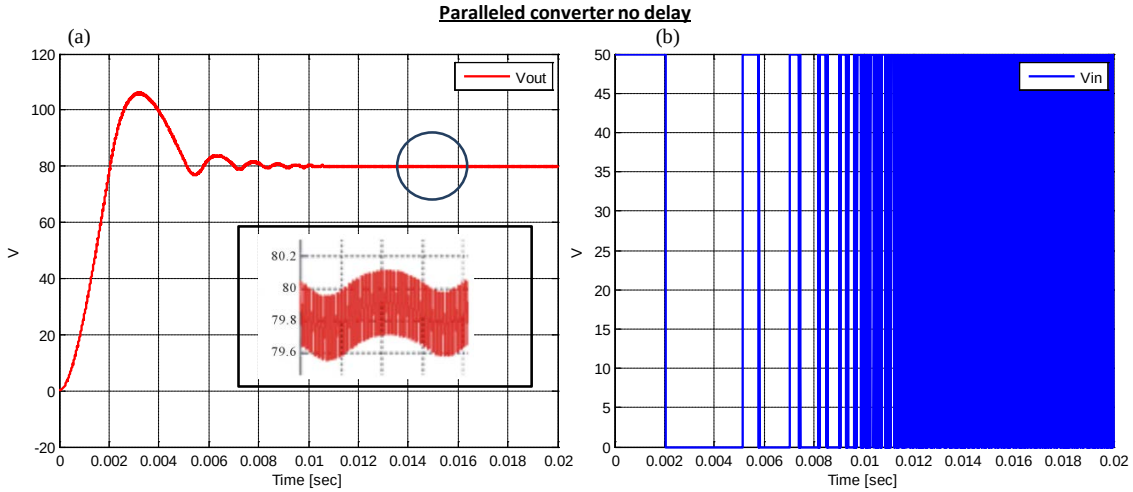

Figure 8. Output voltage, switched input respectively for paralleled converters with constant duty cycle at the performance mode.

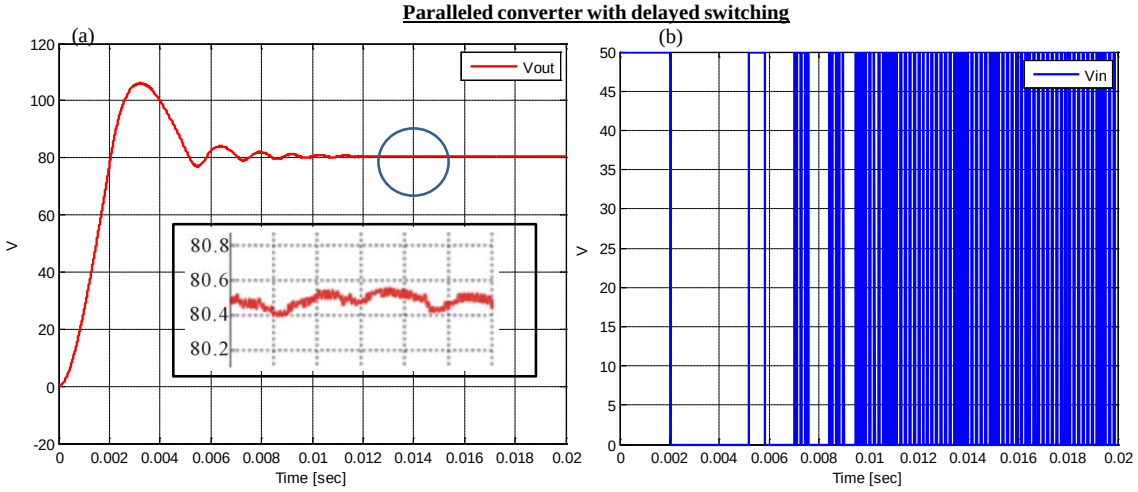

Figure 9. Output voltage, switched input voltage respectively for paralleled converters with enhanced duty cycle at the performance mode.

delayed switching time in the performance stage as suggested by Equation (12) has shown a great deal of improvement. Examining the switched input voltages, it can be seen that the proposed two stage converter has reduced the switching frequency hence reducing the switching losses of the converter in the input stage. The performance stage switching frequency and duty cycle can be optimized to improve the overall efficiency of the system.

Figure 10 shows further improvement on the overall performance of the converters by reducing the ripple and improving the system response to eliminate any overshoot or oscillations. **Figures 11(a)** and **(b)** show he best performance with elimination of ripples and reduction in harmonics content, better system response as the desired voltage is being reached without the overshoot or oscillations.

6. Conclusions

This paper develops a paralleled Buck Boost DC-DC converter with two stages named the control and the performance stages. The control stage performed a manipulation of the input voltage whereas the performance stage was designed to improve further the quality of the output. The quality is measured by reducing the ripples, hence reducing power lost and increasing system reliability.

The converter is controlled using Sliding Mode Control method. The sliding surface in the controlled is developed to be dynamic and duty cycle dependent. This dynamic hyper plane or sliding surface showed an expected improved performance. The results also showed an improved overall performance over typical PID controller, and there was no overshoot or settling time, tracking the desired output nicely. The enhanced mode in combination

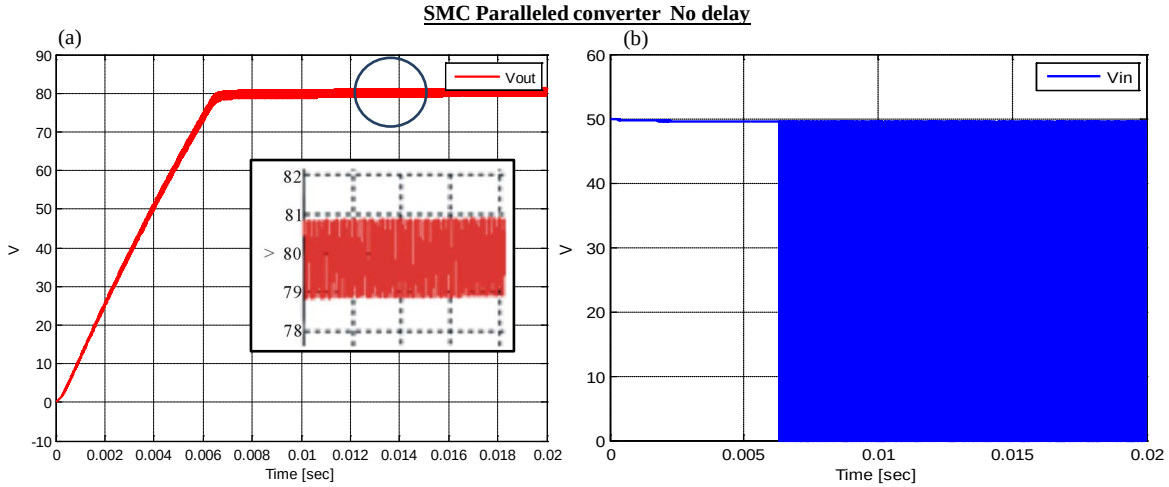

Figure 10. Output voltage, switched input voltage respectively for paralleled converters with constant duty cycle at the performance mode using SMC.

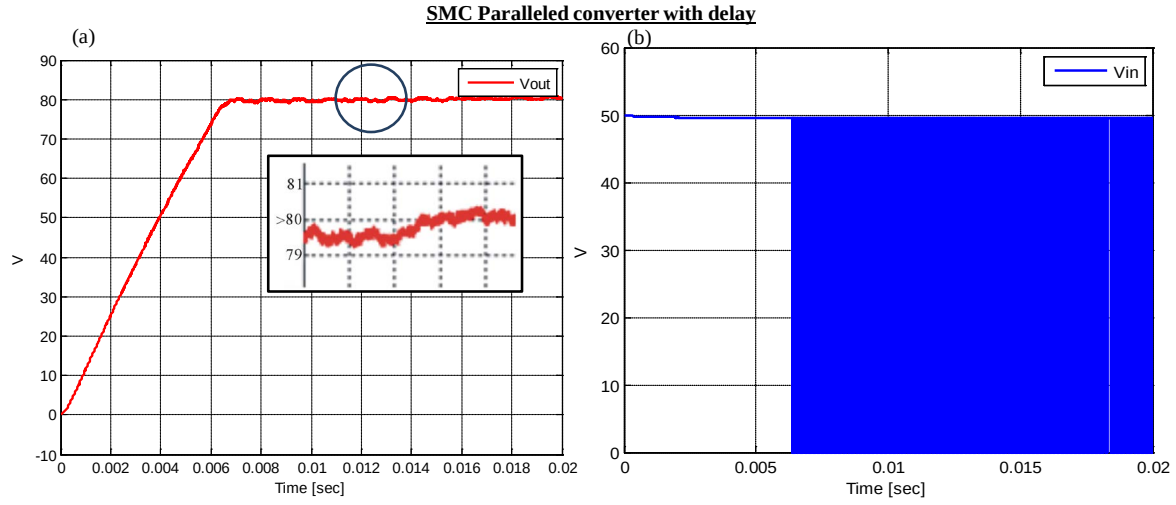

Figure 11. Output voltage, switched input voltage respectively for paralleled converters with enhanced duty cycle at the performance mode using SMC.

with the sliding mode control has shown a reduction in harmonics in comparison to the SMC without the delayed enhanced mode.

With the increasing demand of large power load and the development of distributed power supply system, the importance of research on paralleled power supply modules is increasing, while achieving an equivalent current sharing between the modules is the key element. In future work, the current-sharing control will be presented and compared with other existing ones.

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