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New Control Algorithm for Capacitor Supported Dynamic Voltage Restorer

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ABSTRACT

In this paper, a simple control algorithm for the dynamic voltage restorer (DVR) is proposed to mitigate the power quality problems in terminal voltage such as sag, swell, harmonics, unbalance etc. Two PI (proportional-integral) controllers are used each to regulate the dc bus voltage of DVR and the load terminal voltage respectively. The fundamental component of the terminal voltage is extracted using the synchronous reference frame theory. The control signal for the series connected DVR is obtained indirectly from the extracted reference load terminal voltage. The proposed DVR control strategy is validated through extensive simulation studies using MATLAB software with its Simulink and Sim-power system (SPS) block set tool boxes.

***Keywords*:** *Power Quality, Distribution System, Dynamic Voltage Restorer, Voltage Source Converter, Indirect Control*

1. Introduction

Power quality issues in the distribution system are widely addressed in the literature [1-9] due to the sensitive and critical loads such as precise manufacturing plants, automation etc. A new group of devices based on PWM (Pulse Width Modulated) switching solid state compensators are developed and used for improving power quality in the distribution system under the generic name of custom power devices [3,7]. They are mainly of three categories such as shunt connected distribution static compensator (DSTATCOM), series connected compensator like dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC) which is connected in both shunt and series with the ac mains. The series connected compensator can regulate the load terminal voltage from the "low quality" terminal voltage and protect the critical consumer loads from tripping and consequent loss. The installation of custom power devices at the consumer point is governed by the IEEE standard [10].

A DVR is connected between the supply and the sensitive load so that it can inject a voltage of required waveform. Hence it can protect sensitive consumer loads from supply disturbances. In a capacitor supported DVR, the power absorbed/supplied is almost zero except small losses in the steady state and the voltage injected by the DVR should be in quadrature with the feeder current [3]. The analysis, design and voltage injection schemes of DVR is discussed in the literature [11-17] and the different control strategies are developed in [18-22]. The instantaneous reactive power theory (IRPT) [6], sliding mode controller based [14], symmetrical components based [15] control techniques for series compensators are reported in the literature.

The SRFT (synchronous reference frame theory) based algorithm reported in [21] has the advantage that the calculation is performed in the rotating reference frame. But, the computation involves conversion from stationary frame to rotating frame and then the reference signals from rotating frame to stationary frame. The IRPT algorithm [6] for the reference signal generation involves the conversion from three-phase to two-phase and vice versa. A new control algorithm is developed based on unit templates for the control of a capacitor supported DVR for compensation of voltage sag, swell, harmonics and unbalance in terminal voltage [23]. In this paper, the algorithm is discussed in detail and it is improved by using a PLL (phase locked loop) to extract fundamental component of the terminal voltage. The design of ripple filter is

also investigated for improving the performance of a DVR system. Extensive simulations are performed using MATLAB software with its Simulink and SimPower System (SPS) tool boxes for verifying the proposed control algorithm of DVR.

2. Principle of Operation of DVR

The schematic diagram of a capacitor supported DVR is shown in **Figure 1**. Three voltage sources (v_{sa}, v_{sb}, v_{sc}) represent a 3-phase three-wire supply system and the series source impedances are shown as Z_a (L_a, R_a), Z_b (L_b, R_b) and Z_c (L_c, R_c). The DVR uses a transformer (T_r) to inject a voltage in series with the terminal voltage. A voltage source converter (VSC) along with a dc capacitor (C_{dc}) is used as a DVR. The ripple in the injected voltage is filtered using a series inductor (L_r) and a parallel capacitor (C_r). The load considered is a three phase lagging power factor load.

The ripple filter is designed based on the switching frequency (f_s). It is designed such that the capacitor (C_r) offers a low impedance path for the switching ripple and the series inductor (L_r) provides high impedance for the switching ripple. The reactance given by the capacitor (C_r) and inductor (L_r) at half of the switching frequency (5 kHz) for f_s = 10 kHz *i.e.*, $f_r = f_s/2$ is calculated as,

$$X_{Cr} = 1/(2*\pi* f_r *\mathrm{C_r}) = 1/(2*3.14*5000*C_r) \quad (1)$$

$$X_{Lr} = 2*\pi* f_r *L_r = 2*3.14*5000*\mathrm{L_r}. \quad (2)$$

Considering, X_{Cr} = 3 Ω, C_r = 10.61 μF and X_{Lr} = 100 Ω, L_r = 3.18 mH. These values of ripple filter elements are initially used for simulation and by iteration it is found that, L_r= 3.5 mH and C_r = 10 μF are suitable for minimum ripple in the output of DVR.

Figure 2 shows the phasor diagram of the DVR operation for the compensation of sag in the terminal voltage. The load terminal voltage and current during pre-sag condition are represented as $V_{L(\text{presag})}$ and I_L'. After the sag event, the terminal voltage (V_t) is of lower in magnitude that of pre-sag condition. The voltage injected by the DVR (V_c) is used to maintain the load voltage (V_L) at the rated magnitude and this has two components, V_{cd} and V_{cq}. The voltage in-phase with the current (V_{cd}) is to regulate the dc bus voltage of DVR and also to meet the power loss in the DVR. The voltage in quadrature with the current (V_{cq}) is to regulate the load voltage (V_L) at constant magnitude. The aim of the control algorithm is to achieve these two components of the injection voltage. The sag, swell, harmonic and unbalance in terminal voltage are also compensated by the proposed DVR through extracting the required reference load voltage.

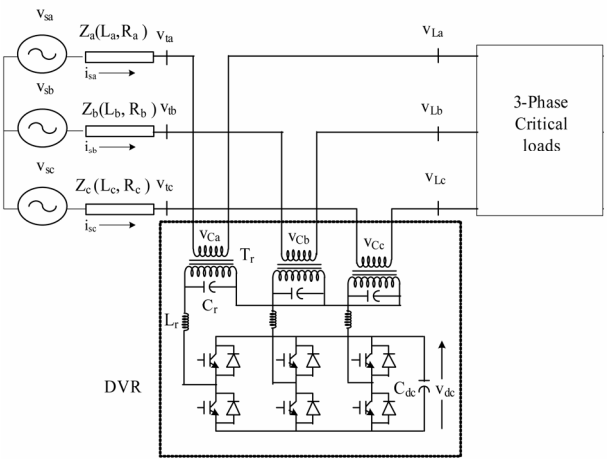


Figure 1. Schematic diagram of capacitor supported DVR for power quality improvement.

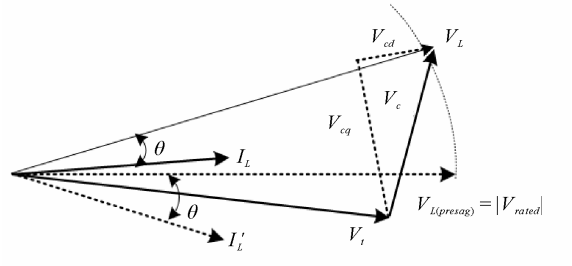


Figure 2. Phasor diagram of capacitor supported DVR.

3. Control Strategy of DVR

The proposed control algorithm is derived from the algorithm presented in [18] in which the shunt compensator is controlled for harmonic current compensation, load current balancing and power factor correction. Here, the sag, swell, harmonic voltage and unbalance in terminal voltage are compensated by controlling the DVR. The load terminal voltage is regulated and the waveform is controlled to sinusoidal. The proposed control scheme is shown in **Figure 3**.

The reference load terminal voltages (v_{La}^* , v_{Lb}^* , v_{Lc}^*) are derived from the sensed supply currents (i_{Sa}, i_{Sb}, i_{Sc}), terminal voltages (v_{ta}, v_{tb}, v_{tc}) and the dc bus voltage (v_{dc}) of DVR as feedback signals. There are two proportional-integral (PI) controllers used to regulate the dc bus voltage of DVR and to regulate the load voltage (v_L).

Three phase in-phase unit voltage templates (u_a, u_b, u_c) are derived from the supply currents (i_{Sa}, i_{Sb}, i_{Sc}) as,

$$i_T = \left(i_{sa}^2 + i_{sb}^2 + i_{sc}^2\right)^{1/2} \quad (3)$$

$$u_a = i_{sa}/i_T;\ u_b = i_{sb}/i_T;\ u_c = i_{sc}/i_T; \quad (4)$$

Moreover, the quadrature unit vectors (x_a, x_b, x_c) are derived from the in-phase unit vectors as,

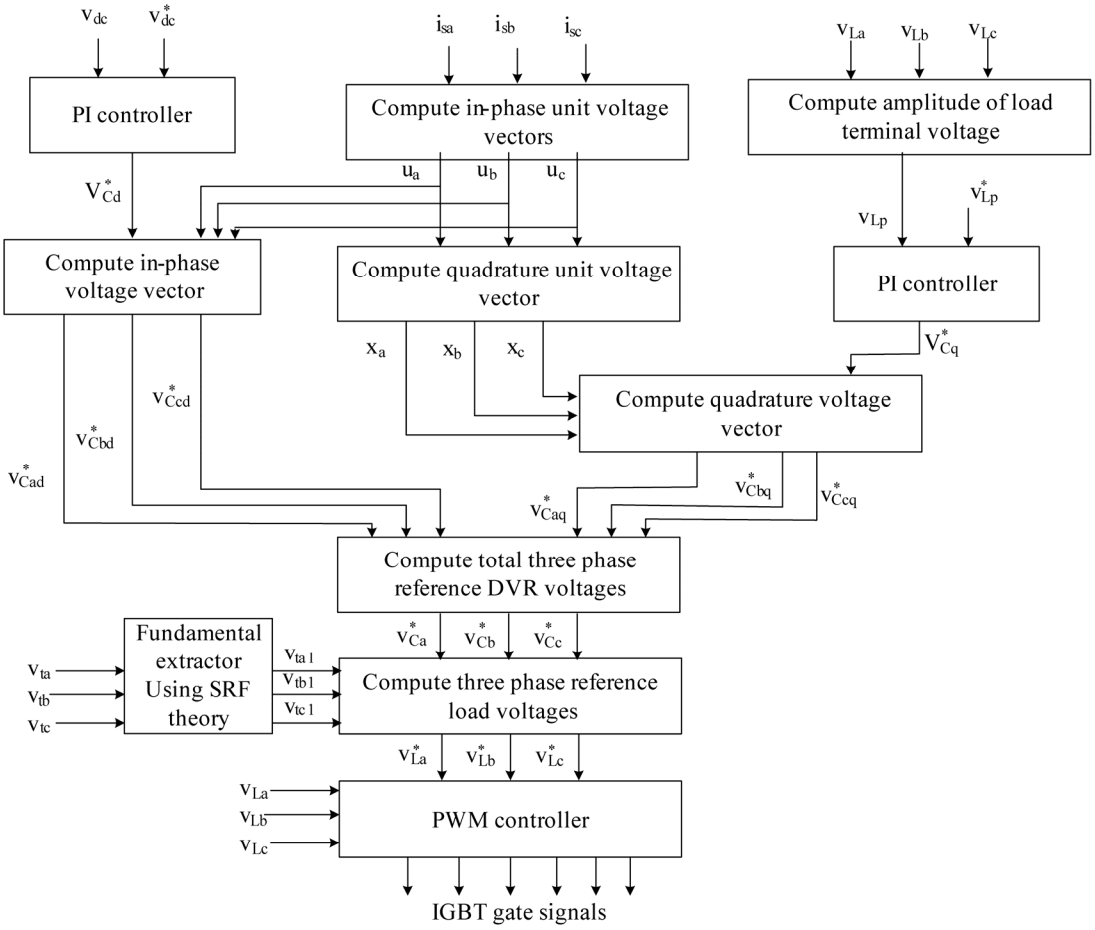


Figure 3. Control scheme of the DVR for power quality improvement.

$$x_a = -u_b/\sqrt{3} + u_c/\sqrt{3}$$
$$x_b = \sqrt{3}u_a/2 + (u_b - u_c)/2\sqrt{3} \quad (5)$$
$$x_c = -\sqrt{3}u_a/2 + (u_b - u_c)/2\sqrt{3}$$

The dc bus voltage of the DVR is regulated using a PI controller over the sensed (v_{dc}) and reference values (v^*_{dc}) of dc bus voltage. This PI controller output is considered as the amplitude (v^*_{Cd}) of the in-phase component of the injection voltages (v^*_{Cad} *, v^*_{Cbd}, v^*_{Ccd}) as,

$$v^*_{Cad} = u_a v^*_{cd} \quad (6)$$

$$v^*_{Cbd} = u_b v^*_{cd} \quad (7)$$

$$v^*_{Cad} = u_c v^{d*}_c \quad (8)$$

A second PI controller is used to derive the amplitude (v^*_{Lp}) of the quadrature component of the injection voltages ($v^*_{Caq}, v^*_{Cbq}, v^*_{Ccq}$) of the DVR by using it over the amplitude of sensed load voltage (V_{Lp}) and reference value (v^*_{Lp}) of the load terminal voltage as,

$$v^*_{Caq} = x_a V^*_{cd} \quad (9)$$

$$v^*_{Cbq} = x_b V^*_{cd} \quad (10)$$

$$v^*_{Ccq} = x_c V^*_{cd} \quad (11)$$

To estimate the positive sequence fundamental component of terminal voltages (v_{ta1}, v_{tb1}, v_{tc1}), the sensed terminal voltages (v_{ta}, v_{tb}, v_{tc}) are required. Two phase unit voltage vectors are derived using a PLL (phase locked loop) over the terminal voltage. The fundamental component of the terminal voltages (v_{ta1}, v_{tb1}, v_{tc1}) are extracted from the sensed terminal voltages (v_{ta}, v_{tb}, v_{tc}) using the synchronous reference frame (SRF) transformation [21]. The reverse of the SRF transformation after filtering the dc component gives the fundamental component of the terminal voltage.

The algebraic sum of the in-phase components (v^*_{Cad}, v^*_{Cbd}, v^*_{Ccd}), the quadrature components (v^*_{Caq}, v^*_{Cbq}, v^*_{Ccq}) and the fundamental of terminal voltages (v_{ta1}, v_{tb1}, v_{tc1}) are taken as the reference load voltages (v^*_{La}, v^*_{Lb},

v_{Lc}^{*}) as,

$$v_{La}^{*} = v_{Cad}^{*} + v_{Caq}^{*} \quad (12)$$

$$v_{Lb}^{*} = v_{Cbd}^{*} + v_{Cbq}^{*} \quad (13)$$

$$v_{Lc}^{*} = v_{Ccd}^{*} + v_{Ccq}^{*} \quad (14)$$

A pulse width modulated (PWM) controller is used over the reference (v_{La}^{*} , v_{Lb}^{*} , v_{Lc}^{*}) and sensed load voltages (v_{La}, v_{Lb}, v_{Lc}) to generate gating signals for the IGBT's (Insulated Gate Bipolar Transistors) of the DVR. The carrier wave (triangular) frequency is set at 10 kHz. The gating pulses switch the IGBT's of the DVR for the compensation of sag, swell, unbalance and harmonics in terminal voltage.

4. MATLAB Based Simulation of the System

Figure 4 shows the MATLAB model of the DVR connected system. The terminal voltage is realized by using a three-phase voltage source and the source impedance is connected in its series. In order to simulate the disturbances at the PCC voltage, an additional load is switched on with a circuit breaker. The load considered is a lagging power factor load. The DVR is connected in series with the supply using an injection transformer. The VSC is connected to the transformer along with a ripple filter. The dc bus capacitor is selected based on the transient energy requirement and the dc bus voltage is selected based on the injection voltage level. The dc capacitor decides the ripple content in the dc voltage. The considered system data are given in Appendix.

The control algorithm for the DVR is modeled in MATLAB and is given in **Figure 5(a)**. The control scheme shown in **Figure 3** is modeled using the tools available in Simulink of MATLAB environment. The fundamental of terminal voltage is extracted using synchronous reference frame theory and the model developed is shown in **Figure 5(b)**. The reference load terminal voltages are derived from the sensed terminal volt-ages, supply currents, load terminal voltages and the dc bus voltage of DVR. A pulse width modulation (PWM) controller is used over the reference and sensed load

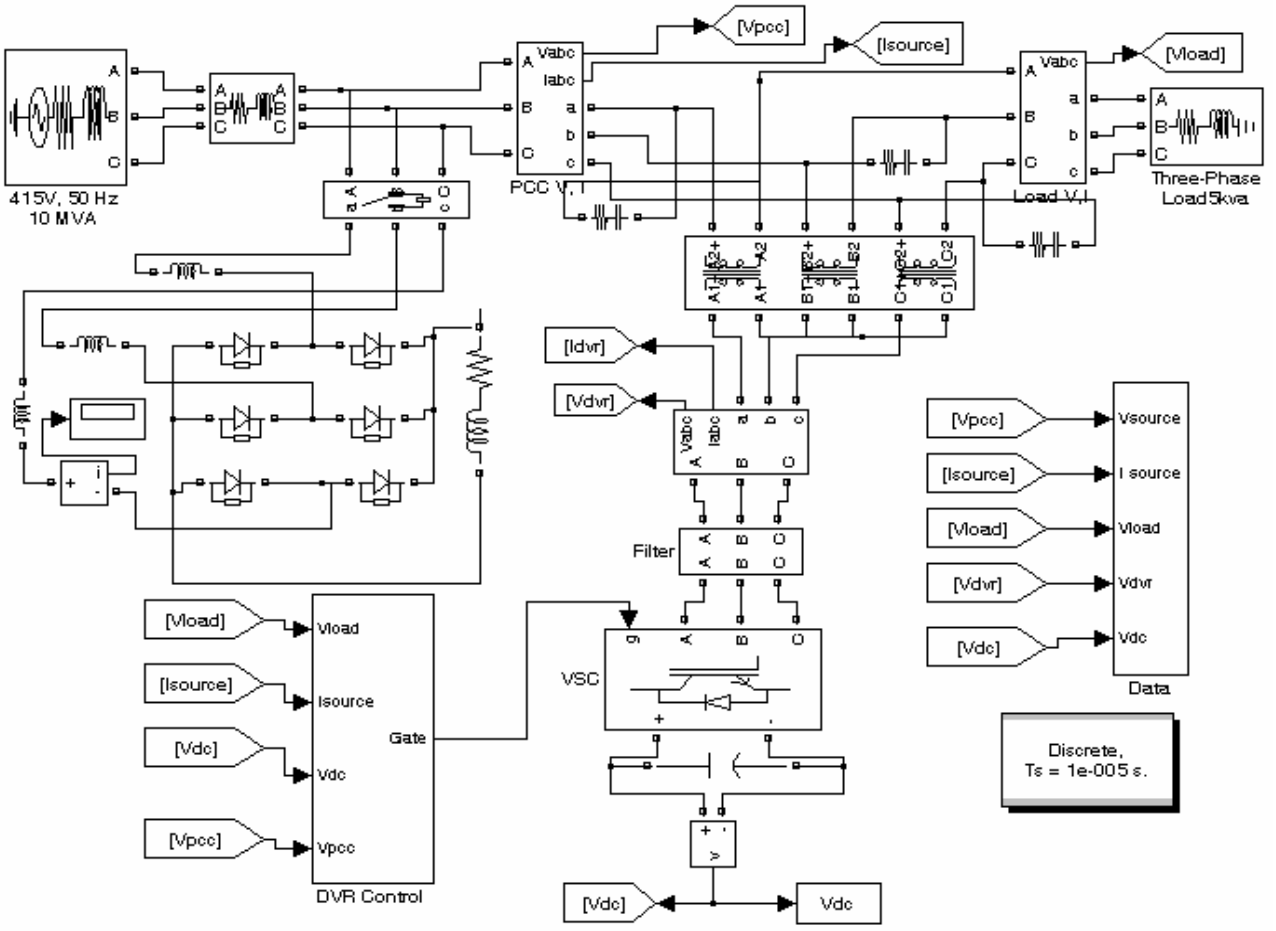
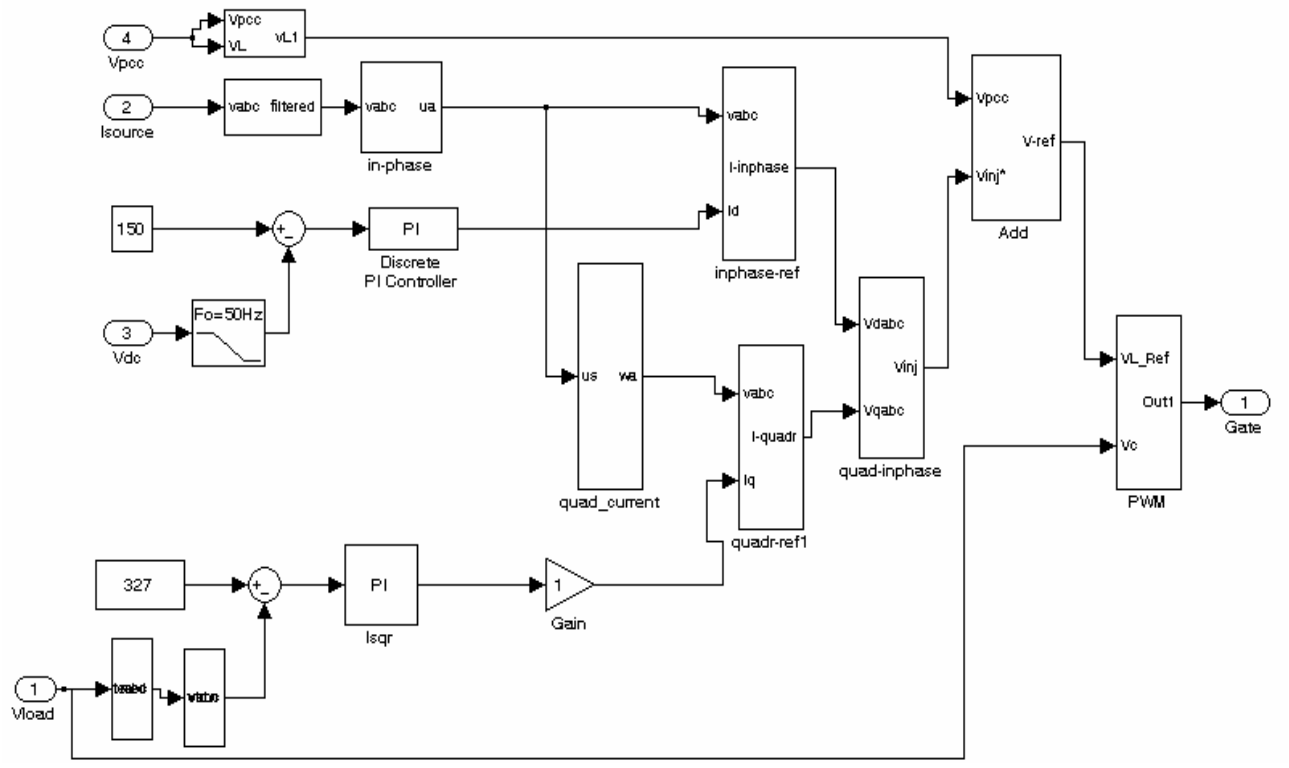
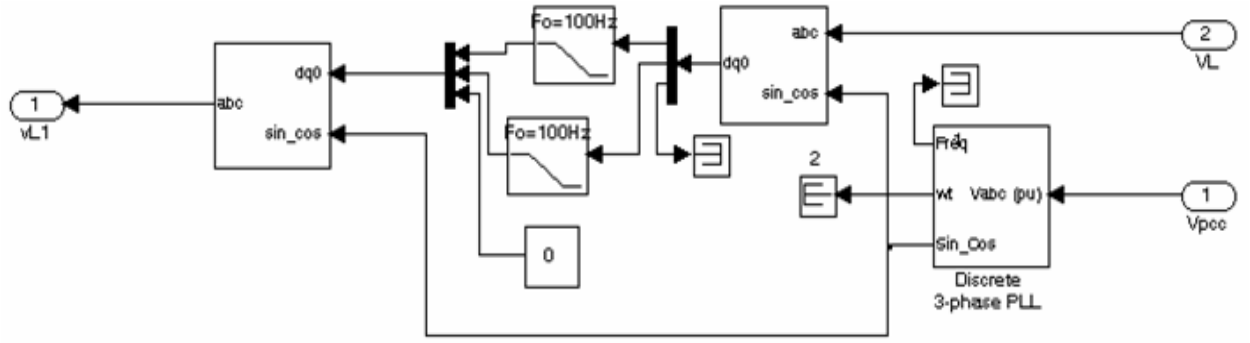


Figure 4. MATLAB model of the DVR connected system.



(a)



(b)

Figure 5. (a) MATLAB model of the control scheme of DVR (b) Subsystem for fundamental terminal voltage extraction using SRF theory.

voltages to generate gating signals for the IGBT's (Insulated Gate Bipolar Transistors) of the DVR.

5. Performance of the System

The performances of the DVR for different supply disturbances are tested under various operating conditions. The proposed control algorithm is tested for different power quality events like voltage sag (**Figure 6**), voltage swell (**Figure 7**), unbalance in terminal voltages (**Figure 8**) and harmonics in terminal voltages (**Figure 9**). **Figure 6** shows balanced sag of 30% in terminal voltage at 0.15 s and occurs for 5 cycles of ac mains. The DVR injects funda mental voltage (v_c) in series with the terminal voltage (v_t). The load voltage (v_L) is regulated at the rated value. The supply current (i_s), amplitude of terminal voltage (V_{Sp}), the amplitude of load voltage (V_{Lp}) and the dc bus voltage (v_{dc}) are also shown in **Figure 6**.

The dynamic performance of the DVR for a swell in terminal voltage is given in **Figure 7**. The load voltage (v_L) is regulated at rated value, which shows the satisfactory performance of the DVR. The supply current (i_s), the amplitude of load voltage (V_{Lp}), the amplitude of terminal voltage (V_{tp}) and the dc bus voltage (v_{dc}) are also shown in the **Figure 7**. The dc bus voltage is regulated at

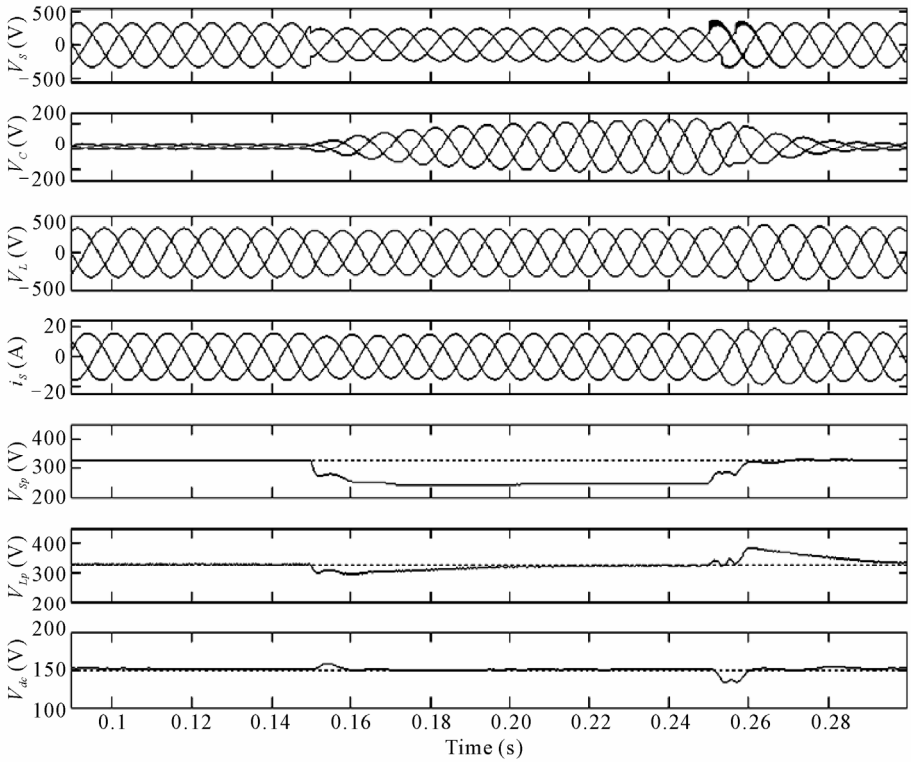


Figure 6. Compensation of PCC voltage sag using DVR.

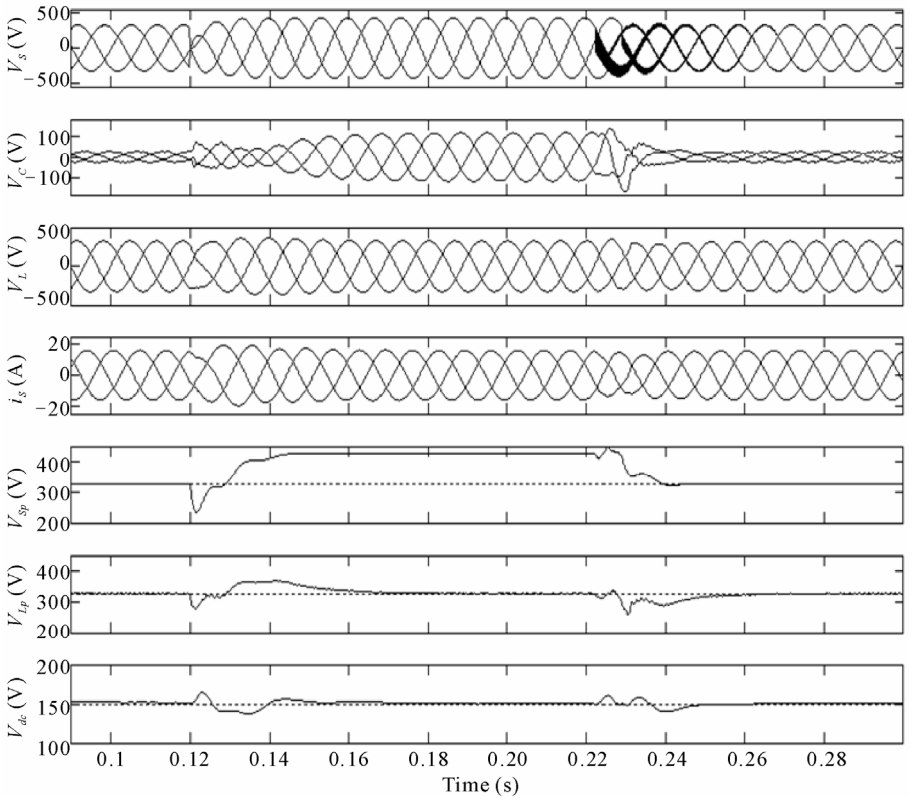


Figure 7. Compensation of supply voltage swell using DVR.

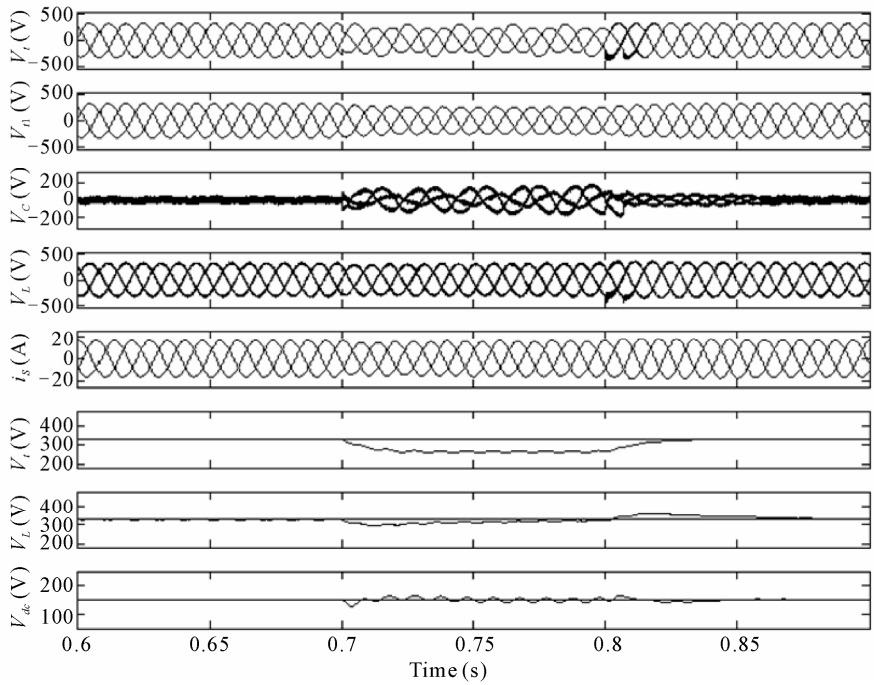


Figure 8. Compensation of supply voltage unbalance using DVR.

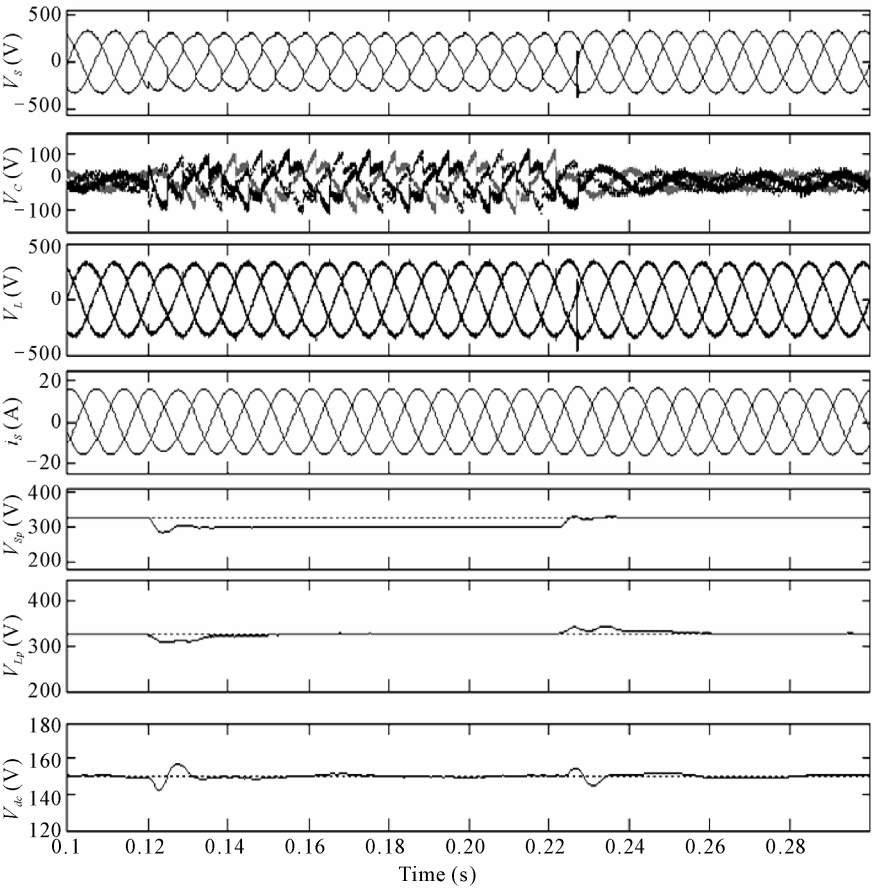


Figure 9. Compensation of supply voltage harmonics using DVR.

the reference value, though small fluctuations occur during transients.

The performance of DVR for an unbalance in terminal voltages is shown in **Figure 8**. The phase voltages at the PCC are different in magnitude at 0.7 s as given in the voltage at PCC (v_t) of **Figure 8**. Now, the DVR injects unequal fundamental voltages (v_c) so that the load voltage (v_L) is regulated to constant magnitude. The supply current (i_s), the amplitude of load voltage (V_{Lp}), the amplitude of terminal voltage (V_{tp}) and the dc bus voltage (v_{dc}) are also shown in **Figure 8** to demonstrate the satisfactory behavior of DVR.

The harmonics compensation in terminal voltage is tested and depicted in **Figure 9**. The voltage at PCC (v_t) is distorted and the load voltage (v_L) is undistorted and constant in magnitude due to the injection of harmonic voltage (v_c) by the DVR. The load terminal voltage (v_L) has a total harmonic distortion (THD) of 1.2% (**Figure 10**) at the time of disturbance and the voltage at PCC has a THD of 7.33% (**Figure 11**). The supply current is also sinusoidal with a THD of 0.14% (**Figure 12**).

6. Conclusions

A new control algorithm based on proportional-integral controllers has been proposed for a capacitor supported dynamic voltage restorer. The proposed algorithm is based on the estimation of in-phase and quadrature component of injection voltages using two PI controllers each for regulating the dc bus voltage of DVR and the load voltage respectively. The reference voltages for the DVR have been obtained indirectly by extracting the reference load terminal voltage. The proposed control algorithm of

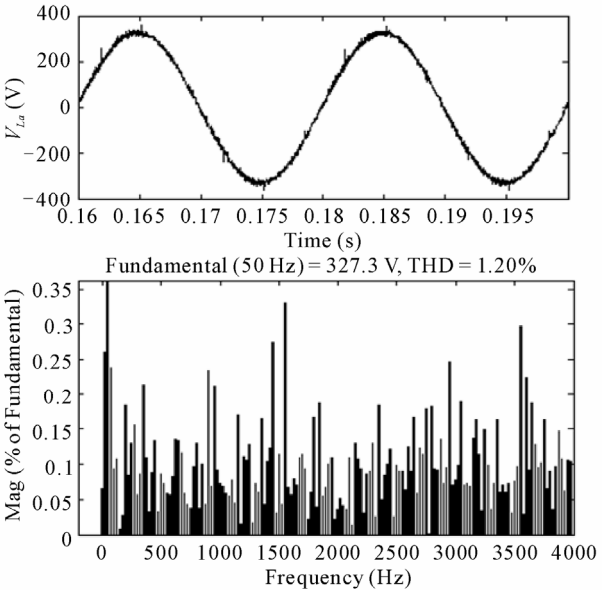


Figure 10. Load voltage along with harmonic spectrum.

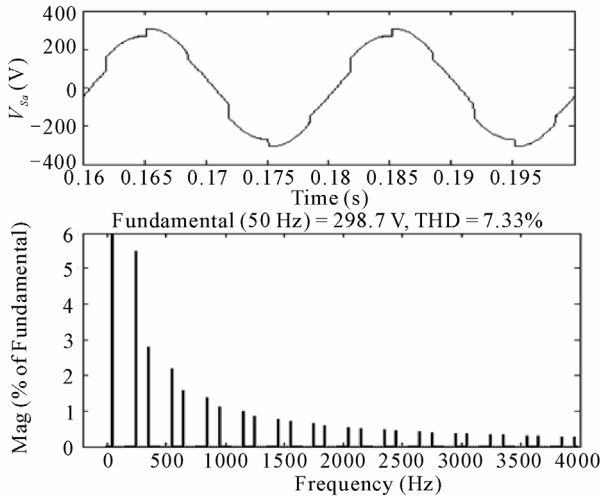


Figure 11. Voltage at PCC along with harmonic spectrum.

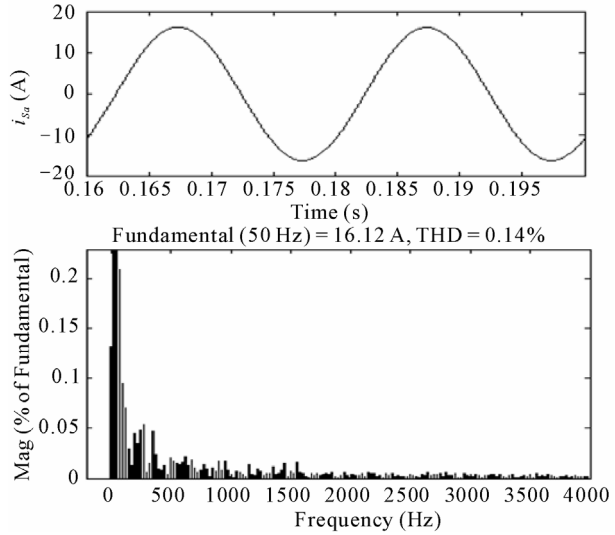


Figure 12. Supply current along with harmonic spectrum.

DVR has been validated through simulation using MATLAB software along with simulink and Simpower system (SPS) toolboxes. The performance of the DVR has been observed to be satisfactory for various power quality disturbances like sag, swell, unbalance and harmonics in PCC voltages. Moreover, it is able to provide a self-supported dc bus of the DVR through power transfer from ac line at fundamental frequency.

REFERENCES

[1] M. H. J. Bollen, "Understanding Power Quality Problems Voltage Sags and Interruptions," IEEE Press, New York, 2000.

[2] J. Schlabbach, D. Blume and T. Stephanblome, "Voltage Quality in Electrical Power Systems," The Institution of Engineering and Technology, Stevenage, 2000.

[3] A. Ghosh and G. Ledwich, "Power Quality Enhancement using Custom Power Devices," Kluwer Academic Publishers, London, 2002.

[4] R. C. Dugan, M. F. McGranaghan and H. W. Beaty, "Electric Power Systems Quality," 2nd Edition, McGraw Hill, New York, 2006.

[5] A. Moreno-Munoz, "Power Quality: Mitigation Technologies in a Distributed Environment," Springer-Verlag London limited, London, 2007.

[6] H. Akagi, E. H. Watanabe and M. Aredes, "Instantaneous Power Theory and Applications to Power Conditioning," John Wiley & Sons, Hoboken, 2007. doi:10.1002/0470118938

[7] K. R. Padiyar, "FACTS Controllers in Transmission and Distribution," New Age International, New Delhi, 2007.

[8] E. F. Fuchs and M. A. S. Mausoum, "Power Quality in Power Systems and Electrical Machines," Elsevier Academic Press, London, 2008.

[9] A. Baggini, "Handbook on Power Quality," John Wiley & Sons, Hoboken, 2008. doi:10.1002/9780470754245

[10] IEEE Standards Office, "lEEE Recommended Practices and Requirements for Harmonics Control in Electric Power Systems," *IEEE Standards* 519-1992, 1992.

[11] M. Vilathgamuwa, R. Perera, S. Choi and K. Tseng, "Control of Energy Optimized Dynamic Voltage Restorer," *Industrial Electronics Society*'99 *Proceedings*, Vol. 2, 1999, pp. 873-878.

[12] I.-Y. Chung, D.-J. Won, S.-Y. Park, S.-I. Moon and J.-K. Park, "The DC Link Energy Control Method in Dynamic Voltage Restorer System," *International Journal of Electrical Power & Energy Systems*, Vol. 25, No. 7, 2003, pp. 525-531. doi:10.1016/S0142-0615(02)00179-5

[13] A. Moreno-Munoz, D. Oterino, M. Gonzalez, F. A. Olivencia and J. J. Gonzalez-de-la-Rosa, "Study of Sag Compensation with DVR," *Proceedings of IEEE MELECON*, *Benalmadena*(*Malaga*), 16-19 May 2006, pp 990-993.

[14] B. N. Singh, A. Chandra, K. Al-Haddad and B. Singh, "Performance of Sliding-Mode and Fuzzy Controllers for a Static Synchronous Series Compensator," *IEE Proceedings on Generation*, *Transmission and Distribution*, Vol. 146, No. 2, March 1999, pp. 200-206. doi:10.1049/ip-gtd:19990072

[15] A. Ghosh, A. K. Jindal and A. Joshi, "Design of a Capacitor-Supported Dynamic Voltage Restorer (DVR) for Unbalanced and Distorted Loads," *IEEE Transactions on Power Delivery*, Vol. 19, No. 1, 2004, pp. 405-413. doi:10.1109/TPWRD.2003.820198

[16] M. R. Banaei, S. H. Hosseini, S. Khanmohamadi and G. B. Gharehpetian, "Verification of a New Energy Control Strategy for Dynamic Voltage Restorer by Simulation," *Simulation Modelling Practice and Theory*, Vol. 14, No. 2, 2006, pp. 112-125. doi:10.1016/j.simpat.2005.03.001

[17] M. R. Banaei, S. H. Hosseini and G. B. Gharehpetian, "Inter-Line Dynamic Voltage Restorer Control Using a Novel Optimum Energy Consumption Strategy," *Simulation Modelling Practice and Theory*, Vol. 14, No. 7, 2006, pp. 989-999. doi:10.1016/j.simpat.2006.06.001

[18] A. Chandra, B. Singh, B. N. Singh and K. AI-Haddad, "An Improved Control Algorithm of Shunt Active Filter for Voltage Regulation, Harmonic Elimination, Power-Factor Correction, and Balancing of Nonlinear Loads," *IEEE Transactions on Power Electronics*, Vol. 15, No. 3, May 2000, pp. 495-507. doi:10.1109/63.844510

[19] A. K. Jindal, A. Ghosh and A. Joshi, "Critical Load Bus Voltage Control Using DVR under System Frequency Variation," *Electric Power Systems Research*, Vol. 78, No. 2, 2007, pp. 255-263. doi:10.1016/j.epsr.2007.02.006

[20] D. M. Vilathgamuwa, H. M. Wijekoon and S. S. Choi, "A Novel Technique to Compensate Voltage Sags in Multiline Distribution System—The Interline Dynamic Voltage Restorer," *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 4, 2007, pp.1603-1611.

[21] S. Bhattacharya and D. Diwan, "Synchronous Frame Based Controller Implementation for a Hybrid Series Active Filter System," *Proceedings of IEEE IAS Meeting* 1995, Hyderabad, 5-7 January 1995, pp 2531-2540.

[22] J. G. Nielsen and F. Blaabjerg, "A Detailed Comparison of System Topologies for Dynamic Voltage Restorers," *IEEE Transactions on Industrial Applications*, Vol. 41, No. 5, 2005, pp.1272-1280. doi:10.1109/TIA.2005.855045

[23] B. Singh, P. Jayaprakash, D. P. Kothari, A. Chandra and K. Al-Hadad, "Indirect Control of Capacitor Supported DVR for Power Quality Improvement in Distribution System," *Power and Energy Society General Meeting—Conversion and Delivery of Electrical Energy in the* 21*st Century*, 2008 *IEEE*, Pittsburg, 20-24 July 2008.

Appendix

Parameters of the DVR connected system
Line Impedance: L_s= 3.5 mH, R_s= 0.01 Ω
Load: 8.5 kVA, 0.707 pf Lag.
Ripple filter: C_r= 1 μF, L_r= 3.1 mH.
DVR:
DC bus voltage: V_{dc} = 150 V.
DC bus capacitance: C_{dc}= 1000 μF.
AC line voltage: V_{LL} = 415 V, 50 Hz.
DC bus PI Controller: K_{p1} = 0.1, K_{i1} = 1.
AC terminal voltage PI Controller: K_{p2} = 0.21, K_{i2} = 2.2.
PWM switching frequency: 10 kHz.
Transformer: 10 kVA, 100 V/400 V

