Image Acquisition Method Based on TMS320DM642

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Abstract

In order to achieve high-speed, real-time and accurate, an image acquisition method based on digital signal processor (DSP) TMS320DM642 is proposed for the paper currency image acquisition [1]. System will be high speed digital signal processing (DSP) technology and complex programmable logic device (CPLD) and CIS acquisition module combination, the structure of acquisition system is given and the time series analysis, during the process of collecting this kind of design has the advantages of simple implementation, high recognition rate [2].

Keywords

Digital Signal Processor (DSP), Image Acquisition System, CIS Sensor, Complex Programmable Logic Device (CPLD), Work Time-Sequence, Programmable Logic

1. Working Principle of Image Acquisition System

In the design of test system hardware circuit, the technologies of CIS Complex programmable logic device (CPLD) and digital signal processor (DSP) are combined [3]. After high speed collection through CIS and conversion with A/D, the bill image data are saved in the DSP space, selected company TMS320C671I as DSP, which used high speed digital signal processing function fully, and the DSP gives the image data a series of disposal in order to realize the recognition and separation. Selected Xilinx Company XC95144 as CPLD, which used high speed logic signal processing function fully, and the CPLD provides the clock and logical signals for the whole system.

The timing of triggering should be consistent with the timing mode set by the DSP processor's video port (configurable video capture interface) to ensure data accuracy [4]. After the completion of a row of data transmission, DSP internal

expansion of the direct memory access interrupt, the data sent to the internal RAM. **Figure 1** shows structure of image acquisition system

2. Design of Time Sequence of Image Acquisition System

2.1. Design of Acquisition Module

The operation of the sensor is such that a line of the bill is photographed by the image sensing element through the lenticular lens by the illumination of the acquisition light source and then the next row of the banknote can be taken as the shift pulse arrives [5]. Banknotes are read line by line, driven by the external timing circuit, each time the shift register to move a row, waiting for one by one to be read, then shift the shift register to a row. This is repeated until all the images are read.

CP is the clock synchronization for each pixel, and SIG is the sampled analog output. SI and CLK signal control SIG analog signal output. The rising edge of SI triggers a line scan and the analog output signal SIG is output on the rising edge of CLK1. In the 65th cycle to collect the first valid signal Pixell, a row of 576 pixels will scan the corresponding sensor sampling level sent through the SIG pin out. The timing shows in **Figure 2**.

2.2. Work Time Sequence of A/D Conversion

The AD9822 is a multiplexed, high-performance 14-bit A/D converter [6]. The three-channel operation mode is used and the conversion frequency could reach 15MSPS. During initialization after DSP is powered on, A/D converter needs to be configured to choose the work mode. For the AD9822 internal register configuration, 3-wire serial communication interface is used.

Figure 3 is the AD9822 register serial write timing diagram. When the strobe signal SLOAD is at the low level, data on the data line SDATA is serially written to the A/D internal register at the rising edge of the clock SCLK. In **Figure 3**, the 16-bit data of SDATA are composed of the selected bits of the read and write operations, the selection bits of the register address and the 9-bit register data.
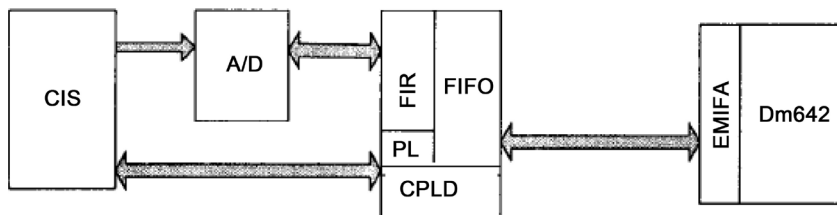

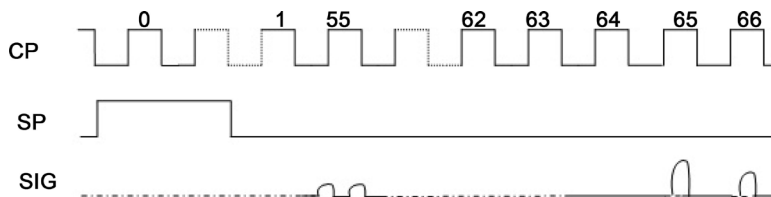**Figure 1.** Structure of image acquisition system.
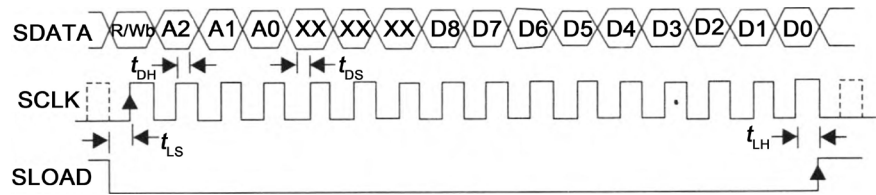

Figure 2. Work time sequence of sensor.
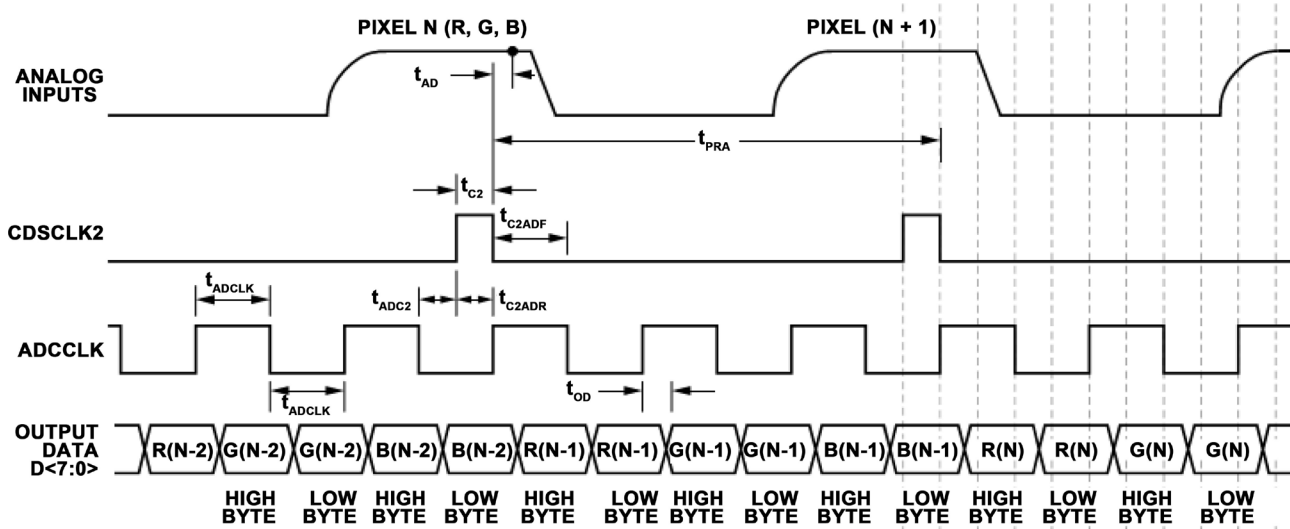
Figure 3. Serial write timing.

Figure 4. 3-channel SHA mode timing.

The system uses a 3-channel SHA mode to transform the data. **Figure 4** is the A/D Conversion Time Sequence of 3-channel SHA mode of AD9822.

2.3. Data Cache Module

As the CPLD and DSP have different global clock, the A/D data collected to the DSP when the rate does not match, prone to data distortion or missing. Asynchronous FIFO (FIFO) can be used to cache data, to ensure the safety of data transmission [7]. There are 36 M4K memory modules in the EP2C5Q208C8 with a total bit count of 165,888 and can be configured for various sizes of memory such as single-port RAM, dual-port RAM and synchronous FIFO [8].

Figure 5 and **Figure 6**, respectively, for the FIFO write timing diagram and read timing diagram. When the write request wrreq signal is valid, write data to the FIFO, when the full flag wfull is high cannot write data, while triggering DSP interrupt, DSP ready to read the data; When the read request rdreq signal is valid, by EDMA Channel, the DSP begins to read the FIFO data, when read empty flag bit rdempty is high cannot continue to read, while FPGA control bit initialization FIFO, ready to write the next line of data.

2.4. Interface Logic and Control Logic

The timing of image acquisition module is uniformly controlled by CPLD [9], that is controlled by the CPLD image sensor CIS sampling timing pulse CP and shift timing pulse SP, while also controlling the AD9822A/D conversion clock,
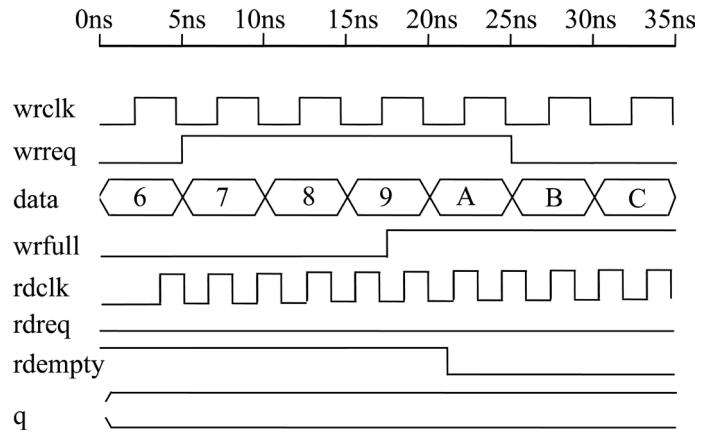
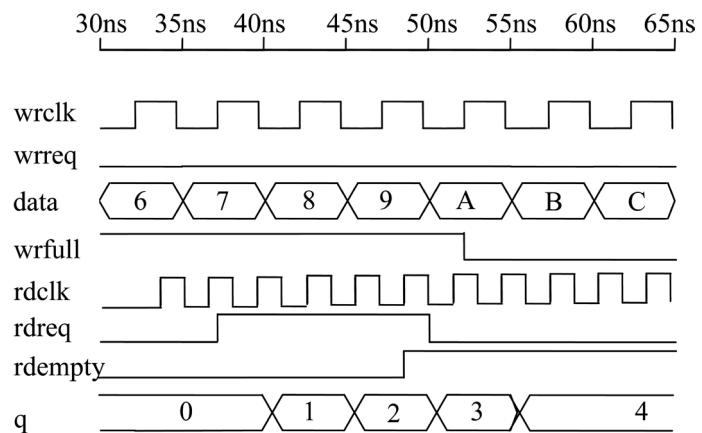**Figure 5.** FIFO writes timing.

Figure 6. FIFO read timing.

the CIS acquisition and AD9822 conversion parallel execution, Improve the image acquisition conversion efficiency. PI240MC-A4 sample CP timing is 5 MHZ clock pulse, and the duty cycle of 25%, shift the SP timing of the cycle is 0.373 ms, the shift output VOUT in the SP low level when the shift output, while providing AD9822 conversion Clock, it and the sampling clock to match the CIS, AD9822 ADCLK conversion clock to 5 MHz, so CIS in image acquisition, AD9822 in the last acquisition of the data conversion, in order to achieve image acquisition and signal conversion in parallel processing. Since the banknote resolution is set to 800×100, a total of 100 lines, image acquisition and AD conversion of the total time will be completed within 37.3 ms. This system uses the programmable logic device XC95144XL-TQ100 to implement the interface logic and control logic [10].

3. Timing Simulation Analysis

In this paper, the work sequence of CIS, A/D, and FIFO is simulated in Quartus II, respectively. For example, Figure 7 shows the sensor timing, timing simulation in figure DSP, the sensor line synchronizing signal and the pixel sync signal is strictly controlled, the output signal of SIG. using DSP hardware resources and strict timing control you can get the desired characteristics, this system can be
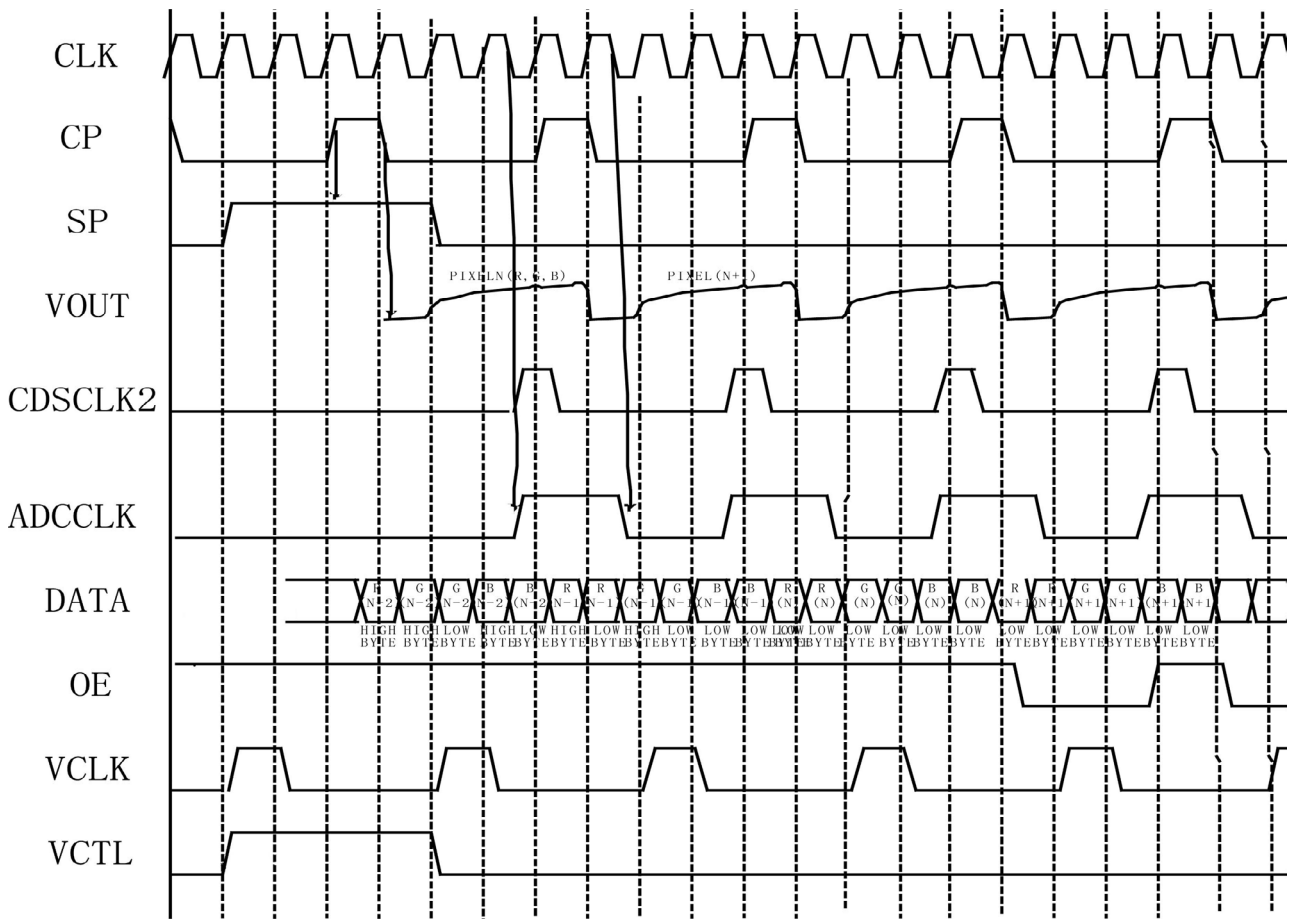
Figure 7. XC95144XL-TQ100 interface time sequence.

very good to complete the work of the image acquisition. To improve the processing function of the system, fully meet the requirements of real-time sorter image processing system.

4. Conclusion

In this paper, the TMS320DM642 chips DSP as the core to complete the design of the image acquisition system. Through the simulation, a careful analysis of the TMS320DM642 image sensor of CIS scanning process, data transmission and other steps of sequential control between ADC and CPLD and DSP, highlights the logic control ability of TMS320DM642 is very good. This system can meet the real-time requirements of the sorter image acquisition, has certain significance for the study of the sorter.

Acknowledgements

CPLD software programming to control the frequency of data acquisition and perform strict frame and field time limits. It not only solves the problems of highly integrated electronic system low power consumption and high stability, but also has the characteristics of high universality and low cost.

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