

# Temperature Dependence of Electrical Properties of Organic Thin Film Transistors Based on pn Heterojunction and Their Applications in Temperature Sensors

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## Abstract

Organic thin film transistors based on an  $F_{16}CuPc/\alpha 6T$  pn heterojunction have been fabricated and analyzed to investigate the temperature dependence of electrical properties and apply in temperature sensors. The mobility follows a thermally activated hopping process. At temperatures over 200 K, the value of thermal activation energy ( $E_A$ ) is 40.1 meV, similar to that of the single-layer device. At temperatures ranging from 100 to 200 K, we have a second regime with a much lower  $E_A$  of 16.3 meV, where the charge transport is dominated by shallow traps. Similarly, at temperatures above 200 K, threshold voltage ( $V_T$ ) increases linearly with decreasing temperature, and the variations of  $V_T$  of 0.185 V/K is larger than the variation of  $V_T$  ( $\sim 0.020$  V/K) in the single layer devices. This result is due to the interface dipolar charges. At temperatures ranging from 100 K to 200 K, we have a second regime with much lower variations of 0.090 V/K. By studying gate voltage ( $V_G$ )-dependence temperature variation factor ( $k$ ), the maximum value of  $k$  ( $\sim 0.11$  dec/K) could be obtained at  $V_G = 5$  V. Furthermore, the pn heterojunction device could be characterized as a temperature sensor well working at low operating voltages.

## Keywords

Organic Thin Film Transistors, pn Heterojunction, Temperature Dependence, Temperature Sensors

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## 1. Introduction

Organic Thin Film Transistors (OTFTs) offer a promising technology for low-cost large-area electronic applications such as active-matrix displays, electronic papers, flexible microelectronics and physical or chemical sensor arrays [1]-[3]. It has been known that temperature is an important physical parameter that is often measured and thermal sensors have a lot of application potentials. The need for reliable, inexpensive and harmless temperature sensors that can be operated simply is also a concern for electronic skins, electronic health monitoring, and de-

tecting patients' body temperatures. However, OTFT-based temperature sensing devices are very sensitive towards a small change in temperature and usually work at highly operating voltages [4]. It is natural that employment of high-k dielectric is one of the most important strategies to reduce operating voltage of OTFT devices [3].

On the other hand, we have reported a kind of organic pn heterojunctions, in which high density of carriers formed a conduction channel at interface [5]-[10]. Ambipolar transport is dependence of the first active layer thickness ( $F_{16}CuPc$ , fluorinated copper phthalocyanine) in an  $F_{16}CuPc/CuPc$  (copper phthalocyanine) heterojunction, and only n-channel operation is observed when  $F_{16}CuPc$  films are over a critical thickness of  $\sim 12$  nm. We have also investigated the temperature dependence of electrical properties of ambipolar OTFTs based on  $F_{16}CuPc/\alpha 6T$  (sexithiophene) pn heterojunction, which hints that the pn heterojunction device has a potential use as a temperature sensor working at low operating voltages without dielectric engineering [9] [10]. In this study, we report on temperature dependence of electrical properties of OTFTs based on  $F_{16}CuPc/\alpha 6T$  pn heterojunction only working at n-channel and their applications in temperature sensors.

## 2. Experimental Details

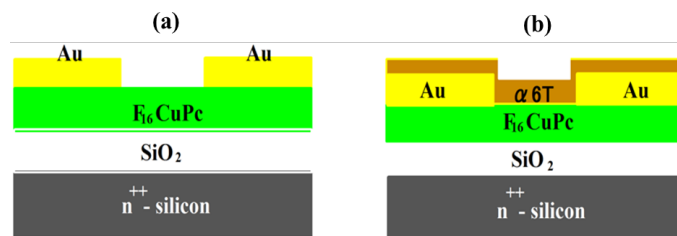
The device configurations are shown in **Figure 1**. First, a top-contact  $F_{16}CuPc$  TFT was fabricated. A heavily n-doped Si substrate acts as the gate electrode with a 300 nm thermally grown  $SiO_2$  layer ( $C_i \sim 10$  nF/cm<sup>2</sup>) as the gate dielectric.  $F_{16}CuPc$  thin films of 20 nm were vacuum-deposited and the substrate temperature was set at 120°C. Au source and drain electrodes of approximately 50 nm were vacuum-deposited through a shadow mask with a channel width of 5 nm and a length of 70  $\mu$ m. Then,  $\alpha 6T$  thin films were vacuum-deposited on the above-mentioned  $F_{16}CuPc$  device at room temperature. The characteristics of the device were *in-situ* measured with a two-channel voltage current source/monitor system (R6245, ADVANTEST) at  $\alpha 6T$  film thicknesses of 0, 1, 2, 3, 5, 7, 10, 15 and 20 nm, respectively, controlled by a shutter. All films were deposited under a base pressure of less than  $1 \times 10^{-3}$  Pa, and thicknesses and growth rates were monitored by a thickness and rate monitor (CRTM-6000, ULVAC). Temperature dependence of electrical characteristics of these devices were measured with R6245 in a cryostat (E202C5L, DAIKIN), which was temperature-controlled from 300 K to 100 K through a cryocooler using a He-gas flowing method.

## 3. Results and Discussion

**Figure 2(a)** shows output characteristics of a sandwich device with  $\alpha 6T$  thin films of 0 nm (namely, the top-contact  $F_{16}CuPc$  TFT), which typically works in an n-channel operational mode. The linear and saturation regions can be observed with the increases of drain voltage ( $V_D$ ) and gate voltage ( $V_G$ ). **Figure 2(b)** shows the same for the sandwich device when  $\alpha 6T$  thin films of 20 nm were deposited. We observe a dramatic difference in the shape and magnitude of the drain current ( $I_D$ ). In the sandwich device  $I_D$  is up to 15.2  $\mu$ A at  $V_G$  and  $V_D$  of 60 V and does not saturate. Furthermore, a large bulk current in the sandwich device at  $V_G = 0$  V could also be observed, which originates from the charge carriers at the interface of  $F_{16}CuPc/\alpha 6T$  [5]-[10]. **Figure 2(c)** shows characteristics of the sandwich device with various thicknesses of  $\alpha 6T$  thin films. Mobility ( $\mu_n$ ) and threshold voltage ( $V_T$ ) were extracted in the linear region as followed [11]:

$$I_D = (W/L)C_i\mu_n(V_G - V_T)V_D(V_G \gg V_D), \quad (1)$$

where  $W$ ,  $L$ , and  $C_i$  are the channel width, channel length, and gate dielectric capacitance per unit area, respectively.



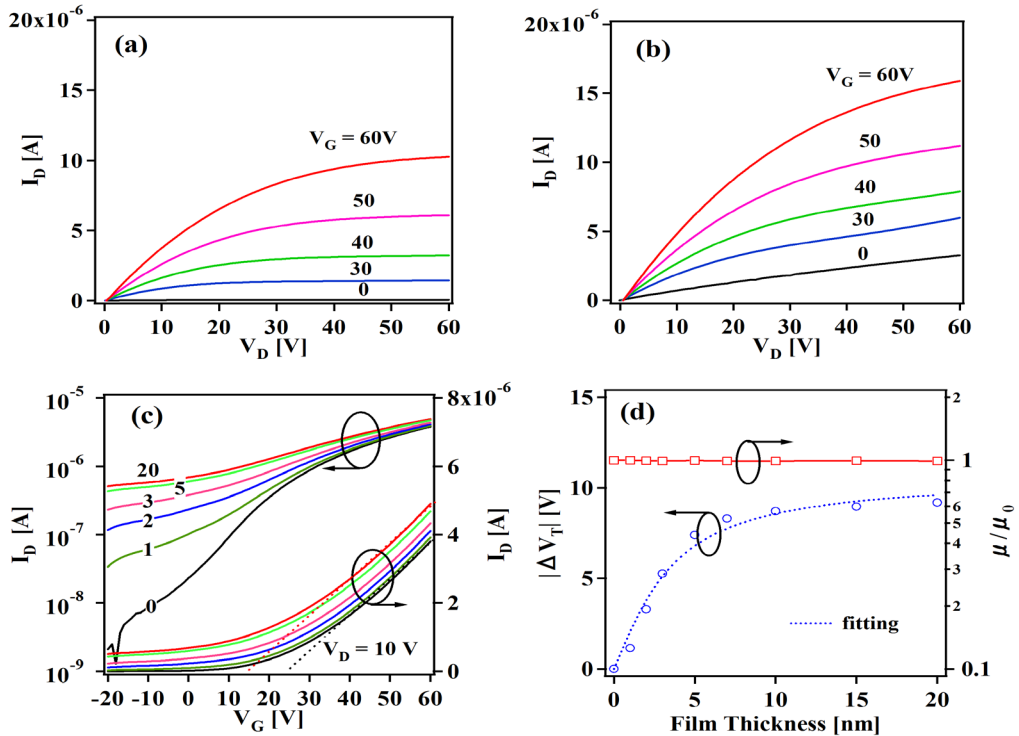
**Figure 1.** Schematic cross sections of (a) a single layer and (b) a sandwich device (the dimensions are not scaled).

The dependence of  $\mu/\mu_0$  and  $V_T$  shift ( $\Delta V_T$ ) on the thickness of  $\alpha 6T$  are shown in **Figure 2(d)**. Obviously,  $V_T$  undergoes a significant shift from +27.13 to +18.10 V with increasing the thickness of  $\alpha 6T$ . When the thickness of  $\alpha 6T$  is more than a critical thickness of 5 - 7 nm,  $V_T$  undergoes hardly any shift. On the other hand, the values of  $\mu_n$  is lightly decreased with increasing the thickness of  $\alpha 6T$  due to the effect of the bulk current. Thus the  $\Delta V_T$  attributes to the increase of  $I_D$  in the sandwich device. It has been known that the bulk current results the organic pn heterojunction interface dipolar, and the electrons and holes are free charges, which are significantly distinguished from ionized impurities, localized in the space charge region for convention inorganic pn junctions, and  $|\Delta V_T|$  is a  $\tan^{-1}$  function of film thickness ( $t$ ) and expressed as following [12]:

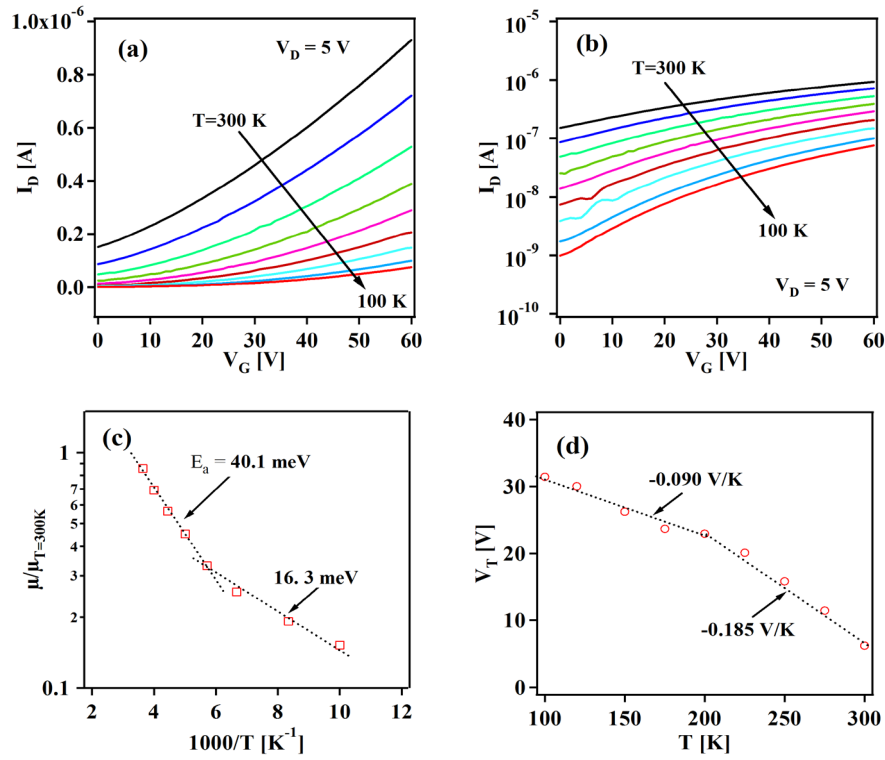
$$|\Delta V_T| = (Q_0/C_i) \tan^{-1}(t/W_d), \quad (2)$$

where  $Q_0$  and  $w_d$  are the total charges density and the full width at half maximum, respectively. The blue dotted line in **Figure 4(d)** is fitted to Equation (2), yielding  $w_d$  and  $Q_0$  of 3.2 nm and  $6.84 \times 10^{-8}$  C/cm<sup>2</sup> ( $4.28 \times 10^{11}$  electrons or holes/cm<sup>2</sup>), respectively. The value of  $w_d$  is in complete agreement with half of the critical thickness of 5 - 7 nm.

**Figure 3(a)** and **Figure 3(b)** show transfer characteristics of another F<sub>16</sub>CuPc/ $\alpha 6T$  TFT in the linear regions at different temperatures.  $I_D$  decrease as the temperature is lowered. Using Equation (1),  $\mu_n$  and  $V_T$  were evaluated from the local slopes of the transfer characteristics in the linear regions. As shown in **Figure 3(c)**, the temperature dependence of mobility can be divided into two regions, and the mobility are clearly thermally activated with thermal activation energy  $E_a$ , which was calculated by Arrhenius behavior as  $\mu \propto \exp(-E_a/k_B T)$  [9]. At temperatures over 200 K, the value of  $E_a$  is 40.1 meV, similar to that of the single layer device [13]. At temperatures ranging from 100 to 200 K, we have a second regime with a much lower  $E_a$  of 16.3 meV, where the charge transport is dominated by shallow traps. The temperature dependence of  $V_T$  for the pn heterojunction device is given in **Figure 3(d)**. At temperatures above 200 K,  $V_T$  increases linearly with decreasing temperature. The variation of  $V_T$  of 0.185 V/K is larger than the variation of  $V_T$  ( $\sim 0.02$  V/K) in the single



**Figure 2.** Output characteristics of a sandwich F<sub>16</sub>CuPc/ $\alpha 6T$  TFT with  $\alpha 6T$  thin films of (a) 0 nm and (b) 20 nm, (c) transfer characteristics of the sandwich device with various thicknesses of  $\alpha 6T$  thin films in the linear regions, and (d) dependence of  $|\Delta V_T|$  and  $\mu/\mu_0$  on the thicknesses of  $\alpha 6T$  thin films, respectively.



**Figure 3.** (a) (b) Transfer characteristics of another  $F_{16}CuPc/\alpha 6T$  TFT in the linear regions at different temperatures, temperature dependence of (c) mobility and (d) threshold voltage of the sandwich  $F_{16}CuPc/\alpha 6T$  TFT, respectively.

layer device [13]. This result is due to the interface dipolar charges [12]. At temperatures ranging from 100 K to 200 K, we have a second regime with much lower variation of 0.090 V/K.

**Figure 4(a)** shows plots of  $\log(I_D)$  as a function of temperature at different  $V_G$  from **Figure 3(b)**, which can be analyzed by Equation (3) as following:

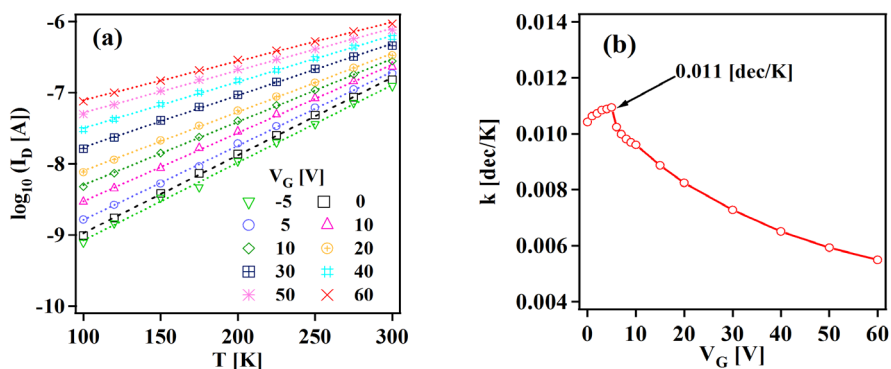
$$\log(I_D) = k * T + c_0, \quad (3)$$

where  $k$  is a  $V_G$ -dependent temperature variation factor,  $d/dT(\log(I_D))$ . Using Equation (3),  $k$  can be calculated for each  $V_G$ , and the result is summarized and shown in **Figure 4(b)**. Increasing  $V_G$ ,  $k$  increases, and then  $k$  decreases when  $V_G > 5$  V. The maximum value of  $k$  ( $\sim 0.11$  dec/K) could be obtained at  $V_G = 5$  V. On the other hand,  $I_D$  at low  $V_D$  and  $V_G$  is comparable to that at high  $V_D$  and  $V_G$  unlike a single layer device. Thus the pn heterojunction device could be characterized as a temperature sensor working at low  $V_D$  and  $V_G$ .

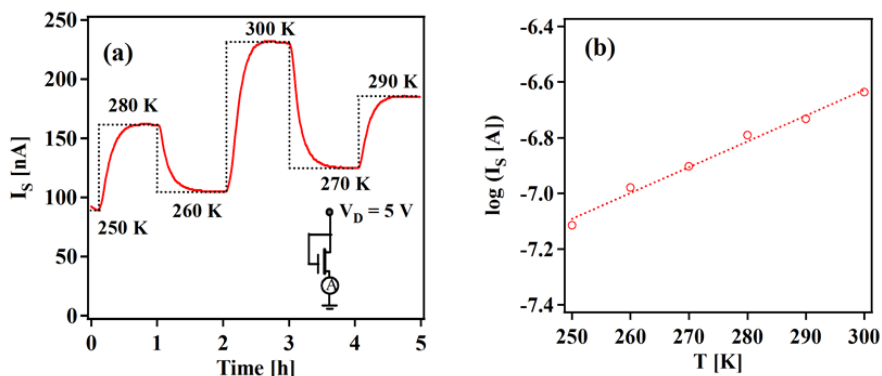
**Figure 5(a)** shows electrical response of a sandwich  $F_{16}CuPc/\alpha 6T$  TFT biased at  $V_D = V_G = 5$  V to temperature cycles, and the measured output current shows over three times of magnitude increase from  $8.91 \times 10^{-8}$  to  $2.83 \times 10^{-7}$  A when the temperature increases from 250 to 300 K. As shown in **Figure 5(b)**, the  $\log(I_s)$  linearly depends on temperatures, and  $k = 9.26 \times 10^{-3}$  dec/K could be obtained when being fitted with Equation (3); this well corresponds to the above-mentioned data. This result shows that the pn heterojunction device may successfully be used as temperature sensing components.

## 4. Conclusion

In this paper, we report on temperature dependence of electrical properties of OTFTs based on an  $F_{16}CuPc/\alpha 6T$  pn heterojunction and their applications in temperature sensors. The mobility follows a thermally activated hopping process. At temperatures over 200 K, the value of  $E_A$  is 40.1 meV, similar to that of the single layer device. At temperatures ranging from 100 to 200 K, we have a second regime with a much lower  $E_A$  of 16.3 meV, where the charge transport is dominated by shallow traps. Similarly, at temperatures above 200 K,  $V_T$  increases linearly



**Figure 4.** (a)  $V_G$  dependence of  $\log_{10}(I_D)$  on the temperatures, and (b) dependence of  $k$  on  $V_G$ .



**Figure 5.** (a) Electrical response of source current ( $I_S$ ) of a sandwich  $F_{16}CuPc/\alpha 6T$  TFT to temperature cycles, and (b)  $\log_{10}(I_S)$  temperature dependence of the sandwich device. The inset of **Figure 5(a)** shows the circuit diagrams of temperature sensor working at  $V_D = V_G = 5$  V.

with decreasing temperature, and the variation of  $V_T$  of  $0.185$  V/K is larger than the variation of  $V_T$  ( $\sim 0.02$  V/K) in the single layer device. This result is due to the interface dipolar charges. At temperatures ranging from  $100$  K to  $200$  K, we have a second regime with much lower variation of  $0.090$  V/K. By studying  $V_G$  dependence of  $\log_{10}(I_D)$  on the temperatures, the maximum value of  $k$  ( $\sim 0.11$  dec/K) could be obtained at  $V_G = 5$  V. Furthermore, the pn heterojunction device could be characterized as a temperature sensor well working at low  $V_D$  and  $V_G$ .

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