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Reconfigurable Digital Circuits Based on Chip Expander with Integrated Temperature Regulation

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Abstract

This article is dealing with a development of custom chip expander platform with the possibility of accurate temperature control and integration of additional silicon-based features. Such platform may serve as a useful tool which facilitates the burdens connected with measurement and analysis tasks of experimental semiconductor structures. The devised solution provides the functionality of carrier substrate (Al_2O_3 compound) with CTE compatibility to the experimental silicon chip and is fully customizable with respect to a particular chip. It also allows achieving an easy fan-out of small-diameter chip terminals into a larger, more convenient area and placement of chip specimens conveniently into space-constrained chamber of the AFM microscopes, probe stations, etc. Real application of the developed chip expander platform is demonstrated in context of digital reconfigurable circuits based on polymorphic electronics. In this case the chip expander with attached polymorphic chip REPOMO is thermally stabilized at an ambient temperature level up to approximately 135˚C and its sensitivity to this phenomenon is demonstrated.

Keywords

Reconfiguration, Digital Circuits, Polymorphic Electronics, Chip Expander, Thick Film, Wirebonding

1. Introduction

Reconfiguration of digital circuits is nowadays considered a widely accepted method which offers numerous feasible ways how to efficiently approach diverse range of existing problems, that are inherently coupled with the domain of contemporary digital electronics. In addition, recent progress within the field of design techniques and low-level building blocks for digital circuits have clearly established yet another direction where the aptly chosen set of components is deployed with the purpose of executing several different (intended) functions. Such type of circuit is often designed as a heterogeneous compact structure comprising both multifunctional, as well

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as their conventional, single-purpose counterparts.

The notion of polymorphic electronics [1] defines, in its own essence, a standalone category of reconfigurable circuits. In this case the intended change of the active function is essentially caused by the occurrence of relevant phenomena having a straightforward impact on the fundamental characteristics of circuit building components, e.g. once these are exposed to the influence of temperature, specific level of power supply voltage, illumination intensity, a special control signal, etc. Most importantly, the change of the polymorphic circuit function comes into effect right away (without any eminent delay perceived) and sensitivity to the environments is naturally embedded to the circuit itself. This is probably the most significant difference between polymorphic electronics and traditional approach to reconfiguration principle.

In order to enable the execution of real experiments with polymorphic electronics, the first reconfigurable chip in the world has been previously designed and physically fabricated. The chip itself is called REPOMO [2] and comes encapsulated in DIL-28 package. In addition to various measurements based on changes of supply voltage as the means of active function selection for the integrated configurable logic elements, its natural sensitivity to temperature variations taking place within the surrounding environment has been identified [3] as well.

However, direct exposure of the REPOMO chip die to the influence of temperature on its behavior was a bit cumbersome just due to the package encapsulation. The proposed chip expander platform simply gets rid of these pitfalls and in the same time provides greater flexibility due to the option to work directly with the bare chip die attached to the expander carrier board. In addition, features like thick-film heating elements and the possibility to integrate other silicon-based circuitry blocks alongside the main chip (REPOMO die in our case) extends its potential exploitation. Moreover, the platform can be customized in order to address the nature of a particular chip and auxiliary elements to be mounted on top of it.

The structure of this paper is organized in the following way: Section 2 provides brief review of basic reconfiguration principles applicable for digital circuits. Then, Section 3 surveys essential aspects behind the concept of polymorphic electronics and circuits design. Novel platform targeted for bare die assembly, which is equipped with temperature regulation features, is introduced in Section 4. Furthermore, experimental results based on the proposed chip expander platform are demonstrated in Section 5. Final conclusion and reflection of further research directions are given in Section 6.

2. Reconfigurable Circuits

Reconfigurable circuit typically consists of a grid-like layout with a certain number of different resources (transistors [4], gates, logic cells or another, e.g. RTL-level components [5]), programmable interconnection matrix and necessary volume of a configuration memory. From a technical point of view, interconnections—responsible for the structural aspects of the circuit—are always programmable, but logic blocks can have either programmable or in most cases fixed function.

The core of each reconfiguration process is based on the capability of changing accordingly the interconnections among individual components of the actual circuit. General purpose fine-grained reconfigurable architectures for digital circuits, such as e.g. FPGAs or FPTAs [4], must obviously have almost complete interconnection network to achieve efficient-enough mapping of a circuit to the available resources. On the contrary, coarse-grained architectures may have the interconnection network more specialized (e.g. data buses among data inputs/outputs of components) [5] [6].

In order to address wide range of different application scenarios of FPGA-like devices, the internal memory for configuration information storage purposes is mostly based on RAM type. In addition, some degree of resistance to a random configuration bit string change is required. It is important namely when the configuration bit string (or its part) is generated (pseudo-) randomly by means of using evolutionary algorithm [7]. Nowadays, many FPGA chips support also partial reconfiguration which is ability to reconfigure a specific part of a particular chip, without simultaneously affecting its remaining portion.

3. Fundamentals of Polymorphic Electronics

In general, polymorphic circuits could be used in situations which involve instantaneous or gradual adaptation of the circuit to variable operating conditions or as a means of smart and fast reconfiguration [1]. Such behavior is useful for circuits that must adapt themselves to unfriendly environment, e.g. by imposing restriction on overall power consumption [8] or heat dissipation [3], and in the same time preservation of necessary basic functionality

is vital. Polymorphic electronics is also very beneficial for applications that are basically mono-functional, but need some additional feature. This is attractive e.g. for embedded diagnostics [9], security applications [10], etc.

3.1. Polymorphic Gates

Polymorphic gate is described as an element which realizes elementary logic (Boolean) function, whereas the function may vary in accordance with the particular state of the environment. Such feature may help to save chip area as well total transistors count and, in the same time, reduce global interconnections significantly. The gate may exhibit e.g. NAND function for some range of the power supply voltage (V_{dd}) and e.g. NOR function for another range of the V_{dd} [11]. It is assumed that polymorphic gate may perform no more than one function with respect to any particular instant during the course of time.

Only two of the polymorphic gates have been physically fabricated so far; remaining polymorphic gates were either simulated or tested in a FPTA [4]. For instance, the 6-transistor NAND/NOR gate controlled by V_{dd} was fabricated in a 0.5-micron HP technology [12]. Another NAND/NOR gate controlled by V_{dd} and introduced in [13] was utilized in the REPOMO chip [2]. Internal electrical interconnections of the designed gate are depicted at a transistor level together with its physical layout in **Figure 1**.

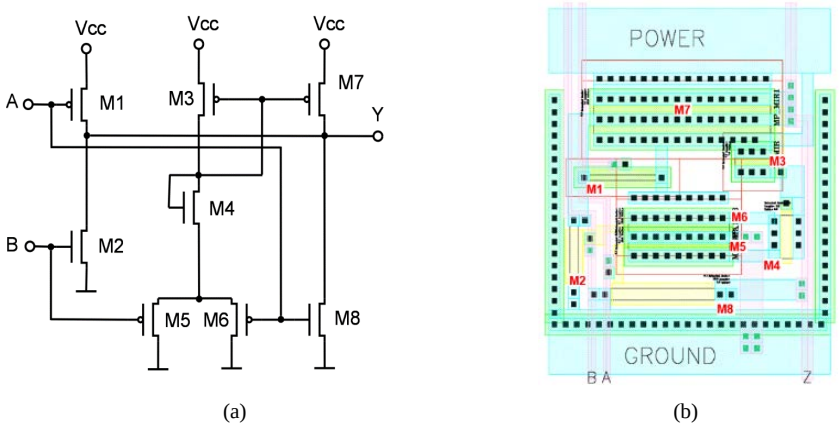
The NAND/NOR polymorphic gate, utilized in the REPOMO chip, is compatible with wide-spread CMOS based circuits (to facilitate its use together with conventional CMOS gates on a single chip). The technology expects the range of V_{dd} supply voltage roughly up to 5.5 V. The gate will accomplish two primary functions f_1 = NAND and f_2 = NOR. Whereas f_1 needs supply voltage around 5 V in order to be executed correctly, function f_2 demands lower supply voltage—around 3.3 V. This is still, however, quite characteristic for digital logic circuits.

3.2. Synthesis of Polymorphic Circuits

Today, the majority of polymorphic circuits are designed almost exclusively at a gate level. Simple circuits could be evidently designed by hand, but the achieved degree of optimization or, in other words, solution optimality would be questionable. Therefore optimization methods established for ordinary digital circuits turns out to be quite unusable. It seems that the evolutionary optimization methods could bring a solution. Almost all complex polymorphic circuits up to the date were designed by means of using Cartesian Genetic Programming (CGP) [14], but also some alternative methods exist [15].

4. Construction of Chip Expander

In order to facilitate all the necessary operations with an experimental semiconductor structure, which is quite often delivered as a bare die slice, it is fundamental to have the appropriate means how to attach the input and output terminals in an easy way to the measuring and testing instrumentation equipment. One of the feasible



(a) (b)

Figure 1. Internal structure of polymorphic NAND/NOR gate on a transistor level (a) and its corresponding physical layout (b) using standard CMOS AMIS 0.7 um technological library. The resulting size of a single gate (b) is approximately 55.8 um × 68.2 um.

methods is to link up the corresponding chip pads by means of using wirebonding process [16]—thin wires (e.g. Au, AlSi) running between designated points on a test structure and suitable carrier board. Since there is a rather small footprint of these on-chip terminals, the interfacing wires are further connected to the layer composed of a suitable conductive motive that makes these signals accessible through easy-to-handle contacts. We literally call these proposed structures as chip expanders.

4.1. Carrier Substrate and Its Layers

As a base layer for the subsequent production of a chip expander, there are used ceramic plates made of Al_2O_3 with a thickness between 0.25 mm and 0.632 mm. These substrates are commonly used as carriers for structures in the domain of thick film hybrid integrated circuits [17]. Before the deposition of the conductive layer it is necessary as a first step to clean the surface of these substrates by isopropyl alcohol in an ultrasonic bath which is then followed by rinsing with deionized water. In either case it's truly vital to get rid through this procedure of any impurities residing on a surface of the substrate, which could ultimately cause defects and seriously influence the conductive motive.

The conductive layer is used for unfolding of the signals across the substrate surface and it is prepared with a silver thick-film pastes ESL 9912-K, which is applied by means of screen printing technology [18]. Before drying procedure the deposited layer has an overall thickness of about 60 microns. After drying in an oven at 125˚C for 15 min, the layer thickness is reduced to approximately 35 microns due to the evaporation of volatile components. The pre-dried structure is further thermally cured in the oven at 850˚C with a peak at time of 10min. and the total processing for 1 h. If necessary, it is also possible to deposit the insulating layer (overglaze composition ESL 4774-BCG), which is used as a solder mask in order to prevent uncontrolled spillage of molten solder during the mounting procedure of expander peripheral pins. This layer is also dried at 125˚C for 15 minutes, but the firing profile is 525˚C with a peak at time 10 to 15 min and total duration of firing cycle reaches 40 minutes.

If the application requires a chip operation at a controlled temperature higher than ambient temperature, it is possible to equip the reverse side of chip expander with a thick film heating element. Thanks to this heating system it is possible to reach temperatures up to 350˚C. In order to measure and stabilize this temperature, miniature semiconductor chip with PN junction is deployed for that purpose. Its placement can be found on the front side in the immediate vicinity of the experimental chip (see bottom-left corner on **Figure 2**). This arrangement can take temperature control feedback over the outer periphery.

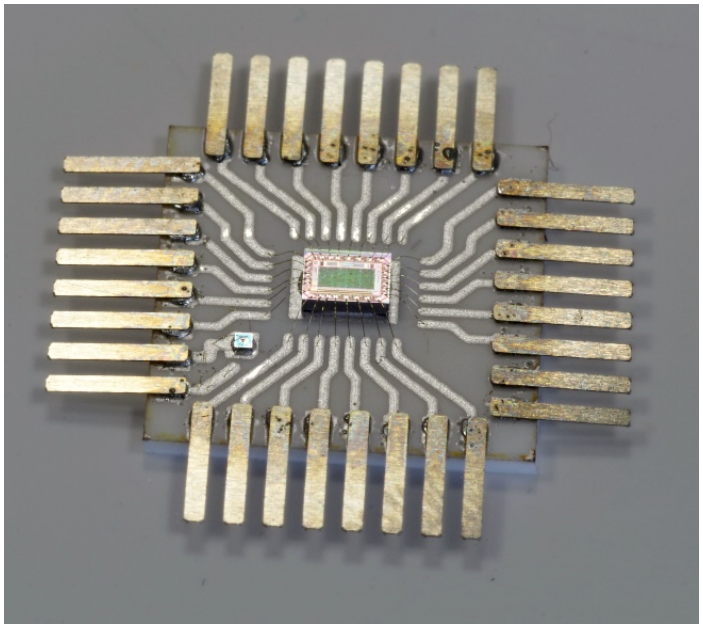


Figure 2. Assembly of REPOMO bare die (precisely in the centre) and P/N junction (close to the bottom left corner) element for direct temperature measurement is mounted on top of the experimental chip expander.

4.2. External Leads and Chip Die Bonding

The leads are made by using etched stencil in 1.27 mm pitch. These leads are dimensionally etched from ALPAKA ($CuNi_{18}Zn_{20}$) material of thickness 150 microns. Its rated current transmission capacity is about 5A. These leads are adjusted and mechanically fixed by soldering or gluing by requirements of application. For low temperature applications is most commonly used eutectic SnPb solder alloy or conductive adhesive EPOTEK H31D. For high temperature applications up to 350˚C is used brazing alloy Cd95Ag5.

Firm attachment of the experimental chip to expander is achieved with the alternative application of conductive or non-conductive adhesive, according to the actual application. If conductive interconnection of chip die with expander is necessary, then one-component epoxy adhesive EPOTEK H31D from Epoxy Technology is used. Minimum bond line cure schedule in this case is 150˚C/1 hour. In case that the conductive connection is not required, it is used one-component epoxy adhesive with high thermal conductivity EPOTEK H61 whose minimum bond line cure schedule is 150˚C/30 minutes. In the case of low temperature resistance of the chip it is possible to use alternative bond line cure schedule 120˚C/60 min. After drying the adhesive operating strength range is from −55˚C to 300˚C.

Glued chip die is contacted to the conductive layer of the expander through the wire bonding technology [16]. It is primarily using Au and $AlSi_1$ wires mostly with a diameter of roughly 25 um. We used ultrasonic bonding technology (both ball and wedge). Besides other aspects the bonding process parameters are dependent primarily on the structure of the contacted layer on the chip and also on their current properties (oxidation, aging, etc.). The resulting platform arrangement after passing through all the technological steps is shown on **Figure 2**.

5. Experimental Results

The polymorphic filter, as it was proposed in [19], consists of N − 1 delay registers, N multiplication units and an N-operand adder which is divided into two sub-adders whose outputs are summed in the third adder. The filter can operate either in the standard mode or backup mode. In standard mode, the filter is operated as any conventionally created N-tap filter with coefficients $b_0 - b_{N-1}$. In the backup mode, the filter approximates the standard mode using restricted resources. In this mode the filter utilizes only M, where M < N coefficients ($b*_0 - b*_{M-1}$) and M − 1 delay registers.

Therefore, original coefficient values $b_0 - b_{M-1}$ are reconfigured and unused parts of the filter are disconnected. In order to reconfigure coefficients, polymorphic constant multipliers could be used. The operation mode was controlled directly through the chip exposure mounted on the proposed platform to the influence of temperature. The measurement presented on **Figure 3** depicts the behaviour of the polymorphic FIR filter circuitry.

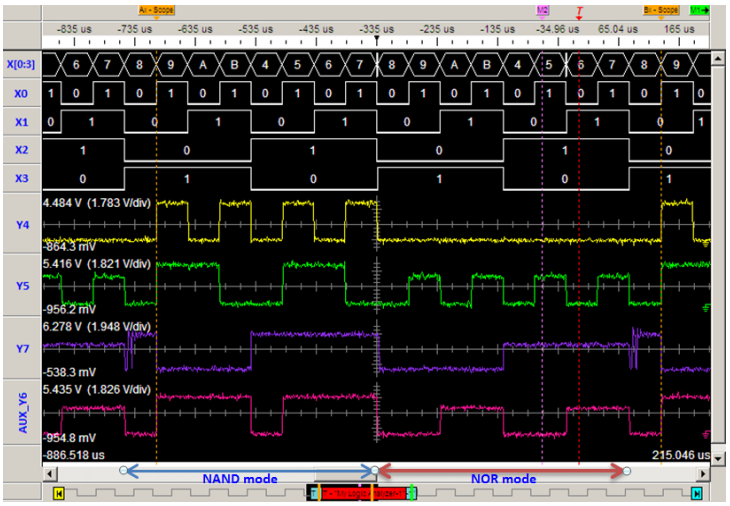


Figure 3. Behaviour of the polymorphic FIR filter section in REPOMO chip on the developed chip expander platform. NAND operation mode is active with the supply voltage of 3.3 V and temperature above 135˚C. Circuit enters NOR operating mode with a temperature of approx. 125˚C and lower.

6. Conclusion

For the purpose of experimental evaluation of the proposed chip expander platform properties, partial section of FIR filter was conceived in polymorphic reconfigurable chip REPOMO. Then, the proposed chip expander platform was heated up using the integrated thick film element. Obtained results are depicted on **Figure 3** and thereby confirm that the proposed chip expander is suitable for experiments with bare chip dies.

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