

State Variable Model for Considering the Parasitic Inductor Resistance on the Open Loop Performance of DC to DC Converters

Carlos Alberto Lozano Espinosa

Pontificia Universidad Javeriana, Santiago de Cali, Colombia Email: <u>carlosal@javerianacali.edu.co</u>

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Abstract

This paper shows DC and small-signal circuit models for the PWM DC to DC buck, boost and back/ boost converters with the equivalent series resistance of the inductor. The DC voltage transfer function and the efficiency of the converter are derived from the DC model. Small-signal open-loop characteristics are derived from the small-signal model based on a state variable model. A design example proves the performance of the circuit and verification of the model.

Keywords

DC to DC Converter, Parasitic Resistance of Inductor, Small Signal Analysis, Buck Converter, Boost Converter, Buck-Boost Converter

1. Introduction

Many papers about small signal analysis of a DC to DC buck-boost converter can be found in literature that include parasitic resistances in inductor and capacitors and voltage drop in power switch and diode [1]-[5]. Usually, the signal model representation is obtained from an equivalent circuit [4], or in other cases, using a state variable model [3]. Any model can be calculated based on the continuous conduction mode or a non-continuous conduction mode but have different results because the former has control over the duty cycle and the latter has control over the frequency.

The objectives of this paper are: to obtain a DC and small-signal linear circuit models of PWM buck, boost and buck/boost DC-DC converter, taking into account parasitic resistance of the inductor; to derive the DC voltage transfer function and efficiency; to derive small-signal open-loop input-to-output transfer function using a state variable model; and to demonstrate, by a design consideration, the performance of a real circuit.

2. Work Description

In anon ideal DC to DC converter, it is necessary to consider power losses from parasitic resistance of the inductor, parasitic resistance of capacitors and power losses in semiconductor switch and diode. **Figure 1** shows some real DC to DC converters with parasitic resistance in inductor.

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Figure 1. DC to DC Converters: (a) Boost; (b) Buck; (c) Buck-boost.

Voltage drop in switch and diode can be neglected in the analysis of the circuit if the voltage input V_{in} is much greater than the drop voltage in switch, and voltage drop in diode. Also, the parasitic resistance in series with capacitor can be reduced by some parallel capacitors. Neglecting voltage drop in switch and diode and parasitic resistance in capacitor, when switch is ON, the following equations represent the behavior of the circuit buckboost in **Figure 1(c)**.

$$-V_{in} + i_L R_L + L \frac{di_L}{dt} = 0 \tag{1}$$

$$-\frac{V_o}{R} = C \frac{dV_o}{dt}$$
(2)

And, when switch is OFF,

$$V_o + i_L R_L + L \frac{di_L}{dt} = 0 \tag{3}$$

$$i_L - \frac{V_o}{R} = C \frac{dV_o}{dt} \tag{4}$$

The state matrixes of these equations are: When switch is ON,

$$\frac{d}{dt}\begin{bmatrix} i_L\\ V_o \end{bmatrix} = \begin{bmatrix} -R_L/L & 0\\ 0 & -1/RC \end{bmatrix} \begin{bmatrix} i_L\\ V_o \end{bmatrix} + \begin{bmatrix} 1/L\\ 0 \end{bmatrix} V_{in}$$
(5)

And when switch is OFF

$$\frac{d}{dt}\begin{bmatrix} i_L\\ V_o \end{bmatrix} = \begin{bmatrix} -R_L/L & -1/L\\ 1/C & -1/RC \end{bmatrix} \begin{bmatrix} i_L\\ V_o \end{bmatrix} + \begin{bmatrix} 0\\ 0 \end{bmatrix} V_{in}$$
(6)

Adding both states, for $t_{ON} = DT$ and $t_{OFF} = (1-D)T$

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$$\frac{d}{dt}\begin{bmatrix} i_L\\ V_o \end{bmatrix} = \begin{bmatrix} -R_L/L & -(1-D)/L\\ (1-D)/C & -1/RC \end{bmatrix}\begin{bmatrix} i_L\\ V_o \end{bmatrix} + \begin{bmatrix} D/L\\ 0 \end{bmatrix} V_{in}$$
(7)

Using Laplace to solve this first order equation, the voltage input-to-output transfer function is,

$$G_{v}(s) = \frac{V_{o}}{V_{in}} = \left(\frac{(1-D)D}{LC}\right) \left(\frac{1}{s^{2} + \left(\frac{1}{RC} + \frac{R \, \infty}{L}\right)s + \frac{1}{LC}\left((1-D)^{2} + \infty\right)}\right)$$
(8)

where $\propto = \frac{R_L}{R}$. The corner frequency is

$$f_o = \frac{1}{2\pi} \sqrt{\frac{\left(1 - D\right)^2 + \alpha}{LC}} \tag{9}$$

In steady state, the transfer function is,

$$M_{VDC} = \frac{V_o}{V_{in}} = \frac{D}{(1-D) + \frac{\alpha}{(1-D)}}$$
(10)

Maximum gain occurs when,

$$\frac{\partial}{\partial D} \left(\frac{V_o}{V_{in}} \right) = \frac{\left(1 - D\right)^2 - 2 \propto D + \infty}{\left(\left(1 - D\right)^2 + \infty \right)^2} = 0$$
(11)

That is,

$$D = (1+\infty) - \sqrt{\infty (1+\infty)} \tag{12}$$

Figure 2 shows the maximum gain of the circuit for values of α between 0.01 and 0.2. As seen, lower values of α give bigger values of gain and the circuit gets closer to an ideal circuit.

Considering this, buck-boost DC to DC converter operates in continuous conduction mode it is necessary to make sure the lowest inductor current is above cero:



Figure 2. Voltage gain vs. R_L/R of a buck-boost converter.

$$I_{\min} = I_L - \frac{\Delta i_L}{2} > 0 \tag{13}$$

If this condition is not considered, the inductor current will have times with zero current and the circuit will work in non continuous mode. Here $\Delta i_L = I_{max} - I_{min}$, the peak currents of the inductor, and I_L is the average inductor current. The average inductor current is,

$$I_{L} = \frac{I_{o}}{(1-D)} = \frac{V_{o}}{R(1-D)}$$
(14)

When switch is open,

$$\Delta i_L = \frac{V_o(1 - D + \infty)}{Lf} \tag{15}$$

Then,

$$L > \frac{R(1-D)^2 + R_L(1-D)}{2f}$$
(16)

The input current is,

$$I_{in} = I_L D \tag{17}$$

From this equation, the DC current transfer function is,

$$M_{IDC} = \frac{I_o}{I_{in}} = \frac{(1-D)}{D}$$
(18)

Efficiency is calculated from the equation:

$$\eta = \frac{V_o I_o}{V_{in} I_{in}} = M_{VDC} M_{IDC} = \frac{1}{1 + \frac{\alpha}{(1 - D)^2}}$$
(19)

For validating these equations a circuit with some practical characteristics is designed and simulated. This circuit is a 1000 watts buck-boost DC to DC converter with an input voltage $V_{in} = 170$ volts, output voltage $V_o = 230$ volts, frequency f = 50 kHz and 5% of voltage ripple. α can go up to 0.09, as seen on **Figure 2**. Working with $\alpha = 0.05$,

$$2.35D^2 - 3.7D + 1.42 = 0 \tag{20}$$

With this equation duty cycle could be 0.6594 or 0.9156. As the **Figure 3** shows, small parasitic resistance in inductance produces more voltage gain, but a maximum voltage gain does not mean a maximum efficiency. So, in order to have a good efficiency-gain relationship, it is better to work in values of D before the maximum peak of gain, that is, in the left side of the curve. Also, as seen on Vo/Vin, the voltage gain curve has less slope with D between zero and D on the maximum gain than in the rest of the curve, which means that a significant change in voltage gain occurs with D varying between D at the maximum gain and one, where the system becomes unstable or more difficult to control.

In the same **Figure 3**, it is shown the efficiency of the circuit which achieves around 70% for D = 0.6594 and close to 10% with D = 0.9156. The values of resistances are R = 52.9 for the load and $R_L = 2.645$ of the permitted parasitic resistance of the inductor, so that,

$$L > 70.4 \ uH \approx 80 \ uH \tag{21}$$

To calculate the capacitor, an equation derived from an ideal circuit analysis, most seen on any power electronics books, can be used, since parasitic resistance of the inductor does not interfere with the ripple voltage at the output of the circuit.

$$C = \frac{D}{Rf(\frac{\Delta V_o}{V_o})} = 5uf$$
(22)



Figure 3. Efficiency and voltage gain of a non-ideal buck-boost converter with $\alpha = 0.05$.

Simulation of the circuit, using PSIM, is shown in **Figure 4** (with the ripple output voltage). In the same **Figure 4**, it is shown a simulation in Matlab of the step response of the transfer function of the circuit (continuous line). Both simulations curves are superimposed to demonstrate the same response and the validation of the equations with respect to simulations.

Small values of parasitic resistances for the inductor will have faster responses but with some overshoot, as in the case of an ideal circuit. Also, bigger values of parasitic resistance for the inductor will have more losses so that the efficiency will be lower and the voltage gain will be reduced. Using same procedure, equations for buck and boost converters can be obtained and they are shown in **Table 1** and **Table 2**. For the boost converter the curve of voltage gain vs. α is shown in **Figure 5**. The efficiency for maximum gain voltage for each value of α is 50%.

Efficiency is inversely proportional to α , so that in order to have a better efficiency with a reasonable voltage gain, it is necessary to reduce α by increasing the switching frequency or construct the inductance with a thicker wire. **Figure 6** shows voltage gain and efficiency of a boost converter for $\alpha = 0.01$. With a lower value of α higher efficiency can be obtained with higher voltage gain. For this example 90% efficiency can be achieved with a voltage gain of 3 and $\alpha = 0.01$. When $\alpha = 0.05$, for a 90% efficiency only it is possible to have a voltage gain of 1.7.

Figure 7 shows voltage gain varying duty cycle for different values of α .

3. Conclusions

This analysis has concentrated on finding the ac model of DC to DC buck, boost and buck-boost converters, only taking into account the parasitic resistance of the inductor. This is because in large voltage conversion, voltage drop in semiconductor switch and diode can be neglected and the parasitic resistance of the capacitor can be easy reduced by many in parallel.

A buck-boost DC to DC converter has been designed for verification of the performance of the circuit and comparison between the model and circuit simulation. As shown, the voltage output of the circuit close follow the equation obtained as a model. Also, the implication of the value of the parasitic resistance of the inductor with respect to the value of the load is shown in a curve for maximum gain, maximizing the gain of the circuit with the duty cycle as the variable to be controlled.



Figure 4. Comparison of circuit simulation and step response of transfer function of a non-ideal buck-boost converter.



Figure 5. Voltage gain vs. R_L/R for boost converters with α between 0.001 and 0.2.



Figure 6. Voltage gain and efficiency for a boost converter with $\alpha = 0.01$.



Figure 7. Voltage gain vs. duty cycle for a buck converter with $\alpha = 0.05, 0.1$ and 0.2.

Table 1.	Small	signal	model	equations	for	boost	converter.
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Boost Converter					
$G_{\nu}(s)$	$\left(\frac{1-D}{LC}\right)\left(\frac{1}{s^2 + \left(\frac{1}{RC} + \frac{R \alpha}{L}\right)s + \frac{1}{LC}\left(\left(1-D\right)^2 + \alpha\right)}\right)$				
f_{o}	$\frac{1}{2\pi}\sqrt{\frac{\left(1-D\right)^2+\alpha}{LC}}$				
$M_{_{VDC}}$	$\frac{1-D}{\left(1-D\right)^2+\infty}$				
$M_{_{IDC}}$	1- <i>D</i>				
η	$\frac{1}{1 + \frac{\alpha}{\left(1 - D\right)^2}}$				
Max Gain at	$D = 1 - \sqrt{\infty}$				

 Table 2. Small signal model equations for buck converter.

	Buck Converter
$G_{\nu}(s)$	$\left(\frac{D}{LC}\right)\left(\frac{1}{s^2 + \left(\frac{1}{RC} + \frac{R \infty}{L}\right)s + \frac{1}{LC}(1 + \infty)}\right)$
f_{o}	$\frac{1}{2\pi}\sqrt{\frac{1+\alpha}{LC}}$
$M_{_{VDC}}$	$\frac{D}{1+\infty}$
$M_{_{IDC}}$	$\frac{1}{D}$
η	$\frac{1}{1+\infty}$

Equations for buck and boost converters are also shown using the same procedure as in buck-boost converter.

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