

A Timing Skew Calibration Scheme in Time-Interleaved ADC

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ABSTRACT

This paper proposes a digital background calibration scheme for timing skew in time-interleaved analog-to-digital converters (TIADCs). It detects the relevant timing error by subtracting the output difference with the sum of the first derivative of the digital output. The least-mean-square (LMS) loop is exploited to compensate the timing skew. Since the calibration scheme depends on the digital output, all timing skew sources can be calibrated and the main ADC is maintained. The proposed scheme is effective within the entire frequency range of $0 - f_s/2$. Compared with traditional calibration schemes, the proposed approach is more feasible and consumes significantly lesser power and smaller area.

Keywords: Timing Skew; Background Calibration; Time-Interleaved; Analog-to-Digital Converters

1. Introduction

Time-interleaved ADCs are widely used in modern communication systems. It is an effective way to realize high resolution and high sampling frequency by paralleling several low-speed but accurate ADCs [1-3]. Time-interleaving can also achieve better power consumption for Giga-Hertz ADCs compared to traditional ADC architectures. However, because of the process, voltage and temperature variations, the ADC channels are not identical and the performance of the TIADC is limited by the offset, gain and timing mismatches among the ADC channels [4]. For the offset and gain mismatches, they are much easier to be compensated based on the equalization technique in the digital domain [5]. However, the timing mismatch is difficult to calibrate since it is relative with the input signal frequency. The front-end sampler is the radical way to eliminate the timing mismatches whereas it is limited by the process imposed maximum speed and charge injection [6]. Zero-crossing technique was adopted to detect and compensate the timing mismatch [7]. Reconstruction technique based on the interpolating filter was also exploited [8,9]. Although the above methods are useful, it sacrifices the design complexity or power consumption to trade for the good performance.

In this paper, we propose a simple background calibration method to compensate the timing mismatch. It is

effective in the whole Nyquist bandwidth and adaptive to any types of channel ADCs. The rest of this paper is organized as follows. In Section 2, the principle of the timing mismatch detection and the compensation loop are presented. Section 3 provides the simulation results. Lastly, Section 4 gives the conclusions.

2. Proposed Timing Mismatch Calibration Scheme

An M-channel TIADC without offset and gain mismatches are shown in **Figure 1**. With interleaving, each channel ADC samples at a rate of f_s/M and the overall sampling rate of the TIADC is f_s . The analog input $V_{in}(t)$ is band limited from DC to the Nyquist frequency with zero mean.

$$V_{in}(t) = A \cdot \cos(w_m \cdot t) \quad (1)$$

The digital output of the i^{th} -channel ADC can be expressed as

$$y_{i,k} = A \cdot \cos(w_m \cdot (kM + i)T_s + \Delta t_i \cdot w_m) \quad (2)$$

where Δt_i is the timing mismatch in the i^{th} -channel ADC.

The derivative of the digital output is as follows

$$y_{i,k}' = A \cdot w_m \cdot \sin(w_m \cdot (kM + i)T_s + \Delta t_i \cdot w_m) \quad (3)$$

2.1. Principle of Timing Mismatch Detection

At the absence of timing mismatch in all channels, the sampling waveform is shown in **Figure 2** and the digital output difference of adjacent channels is calculated

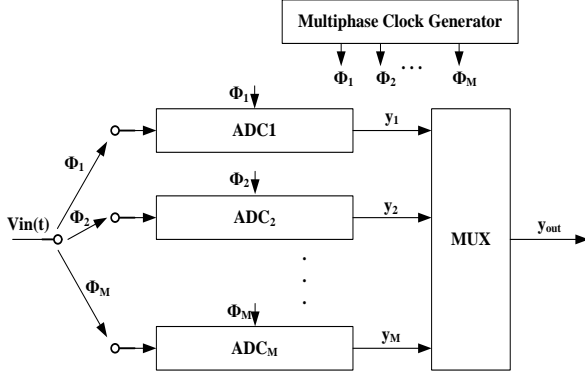


Figure 1. M-channel TIADC.

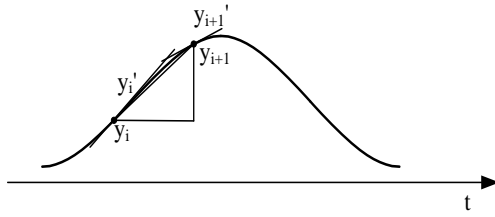


Figure 2. Sampling waveform of TIADC.

$$\begin{aligned} & y_{i+1,k} - y_{i,k} \\ &= A \cdot \cos(w_{in} \cdot (kM + i + 1)T_S) - A \cdot \cos(w_{in} \cdot (kM + i)T_S) \quad (4) \\ &= -2A \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S\right)\right) \cdot \sin\left(\frac{w_{in} \cdot T_S}{2}\right) \end{aligned}$$

The sum of the derivative of adjacent channels is presented.

$$\begin{aligned} & y_{i+1,k}' + y_{i,k}' \\ &= -Aw_{in} \cdot \sin(w_{in} \cdot (kM + i + 1)T_S) - Aw_{in} \cdot \sin(w_{in} \cdot (kM + i)T_S) \quad (5) \\ &= -2Aw_{in} \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S\right)\right) \cdot \cos\left(\frac{w_{in} \cdot T_S}{2}\right) \end{aligned}$$

From (4) and (5), the ratio of the difference and the derivative addition can be expressed as

$$\frac{y_{i+1} - y_i}{y_{i+1}' + y_i'} = \frac{1}{w_{in}} \cdot \tan\left(\frac{w_{in} \cdot T_S}{2}\right) \quad (6)$$

For a specific input signal, the right part of the equation is constant and (6) can be simplified as

$$A_i = D_i - R_i \cdot G = 0 \quad (7)$$

where $D_i = y_{i+1,k} - y_{i,k}$, $R_i = y_{i+1,k}' + y_{i,k}'$ and

$G = \frac{1}{w_{in}} \cdot \tan\left(\frac{w_{in} \cdot T_S}{2}\right)$. Thus, at the absence of timing mismatch, error function A_i equals to zero and the digital

output difference D_i can be calculated by the multiplication of R_i and G .

At the presence of timing mismatch in i^{th} channel Δt_i , the digital output of i^{th} channel will be influenced. Consequently, the output difference D_{i-1} , D_i and the sum of derivative R_{i-1} , R_i are all affected while the others are maintained.

$$\begin{aligned} & D_{i-1} \\ &= -2A \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S + \frac{\Delta t_i}{2}\right)\right) \cdot \sin\left(\frac{w_{in} \cdot (T_S + \Delta t_i)}{2}\right) \quad (8) \end{aligned}$$

$$\begin{aligned} & D_i \\ &= -2A \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S - \frac{\Delta t_i}{2}\right)\right) \cdot \sin\left(\frac{w_{in} \cdot (T_S - \Delta t_i)}{2}\right) \quad (9) \end{aligned}$$

$$\begin{aligned} & R_{i-1} = -2Aw_{in} \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S + \frac{\Delta t_i}{2}\right)\right) \cdot \cos\left(\frac{w_{in} \cdot (T_S + \Delta t_i)}{2}\right) \quad (10) \end{aligned}$$

$$\begin{aligned} & R_i \\ &= -2Aw_{in} \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S - \frac{\Delta t_i}{2}\right)\right) \cdot \cos\left(\frac{w_{in} \cdot (T_S - \Delta t_i)}{2}\right) \quad (11) \end{aligned}$$

Combining (7)-(11), it can be seen that

$$\begin{aligned} & A_{i-1} = -2A \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S + \frac{\Delta t_i}{2}\right)\right) \\ & \cdot \cos\left(\frac{w_{in} \cdot (T_S + \Delta t_i)}{2}\right) \quad (12) \end{aligned}$$

$$\begin{aligned} & \cdot \left(\tan\left(\frac{w_{in} \cdot (T_S + \Delta t_i)}{2}\right) - \tan\left(\frac{w_{in} \cdot T_S}{2}\right)\right) \\ & A_i = -2A \cdot \sin\left(w_{in} \cdot \left((kM + i)T_S + \frac{1}{2}T_S - \frac{\Delta t_i}{2}\right)\right) \\ & \cdot \cos\left(\frac{w_{in} \cdot (T_S - \Delta t_i)}{2}\right) \quad (13) \\ & \cdot \left(\tan\left(\frac{w_{in} \cdot (T_S - \Delta t_i)}{2}\right) - \tan\left(\frac{w_{in} \cdot T_S}{2}\right)\right) \end{aligned}$$

Since the timing mismatch $\Delta t_i \ll T_S$, the first item in (12) and (13) are considered to have the same sign. Under the Nyquist theorem, $w_{in} \cdot T_S < \pi$. The second term in (11) and (12) are both positive. The third term in (12) is positive while that in (13) is negative. Thus, the timing mismatch Δt_i is quantized by the error function A_{i-1} and A_i . According to the signs on A_{i-1} and A_i , Δt_i can be compensated by leading or delaying the sampling clock

of $i-1^{\text{th}}$ channel and i^{th} channel.

The proposed timing skew detector (TSD) is shown in **Figure 3**. The input signal is quantized by each channel

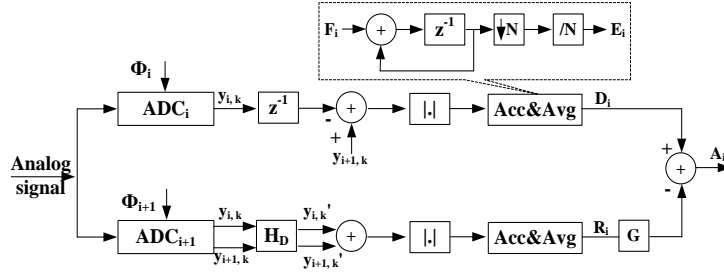


Figure 3. Proposed timing skew detector.

ADC to generate digital output $y_{i,k}$. Referring to [10], the first derivative of the digital output, $y_{i,k}'$, is approximated by the Thiran filter H_D . For any adjacent channels, D_i and R_i are calculated by the accumulation and average (Acc & Avg) block. By multiplying with the constant value G , the product of R_i and G is subtracted from D_i and generates the timing error A_i . Since G is a constant value for a specific input signal, $G = D_i/R_i$ is defined.

2.2. LMS Calibration Loop

A LMS technique is exploited to compensate the timing mismatch. The first channel ADC is set as the reference channel and its sampling clock is not calibrated. Since A_i is the quantization of the timing mismatch of adjacent channels, the sum of A_i represents the total mismatches of all channels. In considering the mean value of the error

$$\bar{A} = \frac{1}{4} \sum_{i=1}^4 A_i \quad (13)$$

\bar{A} is the average timing mismatch of all channels which that would be zero for TIADC. Based on (7) and (14), the relevant timing error can be calculated

$$B_i = A_i - \bar{A} \quad (14)$$

In ideal, B_i can be substituted by zero and (14) will be the same with (6). However, because of the finite approximation, both A_i and B_i exist approximation error. Thus, by subtracting from the average timing mismatch \bar{A} , the relevant timing mismatch in (14) gets rid of the statistical error and represents the real timing error.

The complete LMS timing mismatch calibration loop is shown in **Figure 4**. An accumulation-and-reset (AAR) block is used to filter out the statistical error. The relevant timing error C_i is fed back to the variable delay buffers to compensate the timing error, such that

$$\Delta t_{i,n+1} = \Delta t_{i,n} + \mu_t \times C_i \quad (15)$$

where μ_t is the time step of the delay buffers and it is set to be 0.1ps in this paper. The proposed TSD measures the timing skew between Φ_i and Φ_{i+1} and then adjusts C_i to minimize the timing skew.

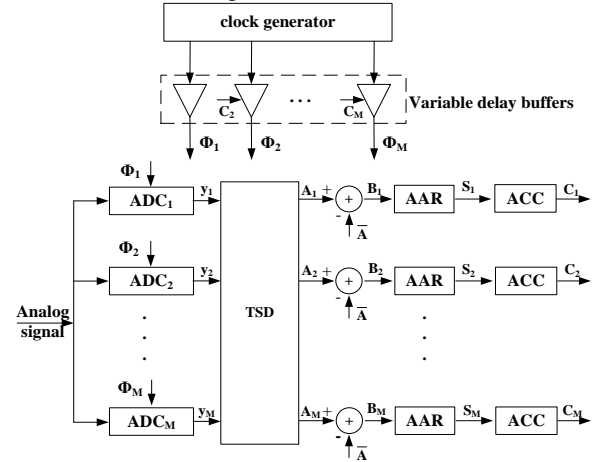


Figure 4. LMS calibration loop.

3. Simulation Results

The proposed timing skew calibration to a 12-bit four-channel TIADC is modeled and simulated with MATLAB. The channel ADC is composed of pipeline ADC with a sample-and-hold (S/H) circuit, four 2.5-bit multiplying-digital-to-analog converter (MDAC) stages, and 3-bit flash ADC. To focus on the timing skew calibration, offset and gain mismatch are assumed to be nonexistent in this paper. Considering the real situation of a chip, the model contains sorts of non-ideality. Firstly, 3‰ random mismatches are added between the capacitors in all multiplying-digital-to-analog converter (MDAC) stages. The parasitic capacitor at the input node of MDACs is set to be a quarter of the sampling capacitor. The DC gain of the amplifier in S/H and in the first MDAC stage is designed to be 80 dB, and other MDAC stages are scaled down in sequence. The rms jitter of the sampling clock is set at 0.2 ps. For all simulations, the timing mismatch

among channels is assumed to satisfy Gauss distribution with a standard deviation of $0.01T_s$.

The timing skew calibration convergence process is shown in **Figure 5**. Since the first channel is set as the reference channel, only other three channels are calibrated. Initially, the timing mismatch of the channels is at the maximum. During calibration, the timing mismatches

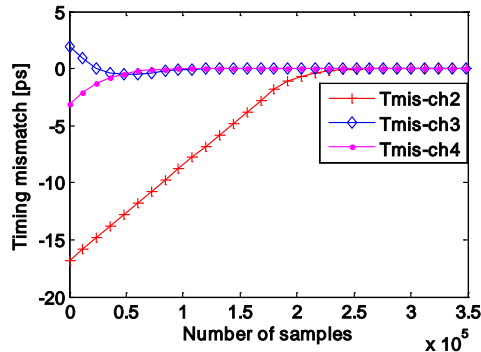


Figure 5. Timing skew convergence time.

are minimized after approximately 3×10^5 samples.

Figure 6 shows the output spectra of the TIADC with and without the proposed timing skew calibration. The normalized input frequency is at $f_{in} = 0.153f_s$. When the calibration is off, the distortions due to the timing skew appear at frequencies $f_s/4 \pm f_{in}$ and $f_s/2 - f_{in}$ with high energy. The signal-to-noise and distortion ratio (SNDR) of the TIADC is 38.3 dB. After calibration, the distortions attributed by the timing mismatch are minimized, and the SNDR is improved to 68.8 dB, which is close to the desired value of 68.9 dB.

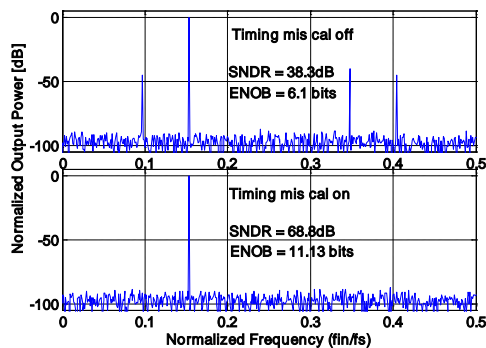


Figure 6. Output spectra of the TIADC.

4. Conclusion

This paper proposes a digital background timing skew calibration scheme for TIADC. It detects the relevant

timing error by the ratio of the output difference and the sum of the first derivative of the channel ADCs. Since the detection depends on the digital output, all timing skew sources can be calibrated and the main ADC is maintained. The proposed scheme is effective within the entire frequency range of $0 - f_s/2$. Compared with traditional calibration schemes, the proposed approach is more feasible and consumes significantly lesser power and smaller area.

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