**Scientific
Research**

A Digital Background Calibration Technique for Successive Approximation Register Analog-to-Digital Converter

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ABSTRACT

A digital background calibration technique that corrects the capacitor mismatches error is proposed for successive approximation register analog-to-digital converter (SAR ADC). The technique is implemented in SAR ADC which is based on tri-level switching. The termination capacitor in the Digital-to-Analog Converter (DAC) is regarded as a reference capacitor and the digital weights of all other unit capacitors are corrected with respect to the reference capacitor. To make a comparison between the size of the unit capacitor and that of the reference capacitor, each input sample is quantized twice. The unit capacitor being calibrated is swapped with the reference capacitor during the second conversion. The difference between the two conversion results is used to correct the digital weight of the unit capacitor under calibration. The calibration technique with two reference capacitors is presented to reduce the number of parameters to be estimated. Behavior simulation is performed to verify the proposed calibration technique by using a 12-bit SAR ADC with 3% random capacitor mismatch. The simulation results show that the Signal-to-Noise and Distortion Ratio (SNDR) is improved from 57.2 dB to 72.2 dB and the Spurious Free Dynamic Range (SFDR) is improved from 60.0 dB to 85.4 dB.

Keywords: Analog-to-Digital Conversion; Capacitor Mismatch; Digital Background Calibration; SAR ADC

1. Introduction

As the dimension of CMOS technology continues to scale down, the advantages of successive approximation register analog-to-digital converter (SAR ADC) become prominent over other ADC architectures due to its simple structure. For charge redistribution SAR ADC, the essential building blocks, including switched-capacitor array, comparator and digital circuits, can be well designed with devices scaling down into the nanoscale domain. In recent years, researches on high speed SAR ADC are extensively reported [1-5]. The unit capacitor is usually brought down to the limit allowed by kT/C noise and the process to decrease the settling time of the Digital-to-Analog Converter (DAC) [1-3,6,7]. However, the mismatch of such small capacitors is severe, and degrades the linearity of the ADC. Calibration of capacitor mismatch error is indispensable for high resolution SAR ADC if small unit capacitors are used. Recently, digital-domain background calibration is more preferred than analog-domain calibration as the design complexity is

transferred to digital circuits which can benefit from the device scaling of CMOS technology. In addition, digital-domain calibration tracks the variations of the fabrication process and environmental factors.

In [8], the "split ADC" architecture is applied to SAR ADC to correct the capacitor mismatch error. Two identical SAR ADCs are used to quantize the input signals. The difference of their output codes is used to estimate the digital weights of the capacitors. The "split ADC" architecture however, inevitably increases the complexity and area of the analog circuits. A perturbation-based background digital calibration is proposed in [9]. The SAR ADC quantizes each analog input signal twice with two analog offsets. The difference between the two quantization results is used to calculate the actual weight of each capacitor. In this calibration algorithm, the input dynamic range is reduced due to the offset injection. A dithering technique is developed in [10] to examine the MSB capacitor weights for the SAR ADC. The dithering signal is injected to the input signal and the capacitor weights are extracted from the dithered signal. The

dithered signal is quantized twice to handle the problem of reduced signal range. However, an extra sample-and-hold amplifier, which holds the input signals for two ADC cycles, is needed for the calibration running in the background.

This work presents a digital background calibration technique to correct the capacitor mismatch errors in SAR ADC with tri-level switching. Tri-level switching, which is widely used in SAR ADC [3,4,11], reduces the switching energy and the total capacitance [4]. In the proposed calibration technique, the termination capacitor in the DAC is regarded as a reference capacitor and the digital weights of all of other unit capacitors are corrected with respect to the reference capacitor.

This paper is organized as follows. Section 2 introduces the tri-level switching method. Section 3 describes the details about the digital calibration technique. Behavior simulation results are presented in Section 4 and the conclusion is given in Section 5.

2. Tri-Level Switching

Figure 1 shows the schematic of a 4-bit differential SAR ADC and its timing diagram. A 3-bit DAC can be used to realize a 4-bit SAR ADC based on the tri-level switching. **Figure 2** shows the waveform of the reference voltage generated by the DAC and two different data formats.

During the sampling phase, all the capacitors are connected to the input voltage and the top plates of the capacitors are connected to V_{CM} which equals to half of V_{REF}. After that, all the capacitors are reset to V_{CM} during the resetting phase. If $V_{DAC,P} > V_{DAC,N}$, $C_{3,P}$ is then switched from V_{CM} to GND and $C_{3,N}$ is switched from V_{CM} to V_{REF}. All of the remaining capacitors are switched in the same manner. If the input voltage is $V_{i,1}$, the output code is "0110" according to each comparison result, as indicated in **Figure 2**. The output data format is offset binary.

The output code can be derived in another way. The weights of the three capacitors in digital domain Wd_i ($i = 1, 2,$ and 3) are 00010, 00100 and 01000, respectively. The first bit of the digital weight is the sign bit. A 5-bit code is used to represent the digital weight of each capacitor, which will be explained in the following paragraphs. If a capacitor is switched from V_{CM} to V_{REF}, the digital weight of the capacitor should be added to the output code; if a capacitor is switched from V_{CM} to GND, the digital weight of the capacitor should be subtracted from the output code. In the above example, C_3 is switched from V_{CM} to GND while C_2 and C_1 are switched from V_{CM} to V_{REF}. Therefore, the output code can be determined by Equation (1). The output data format is two's complement.
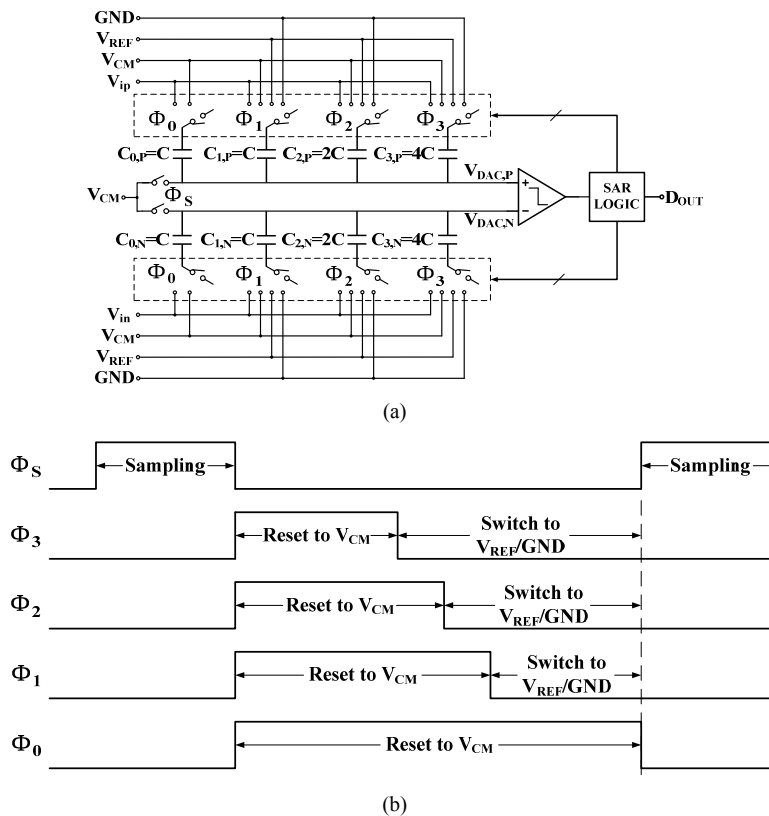
$$D_{OUT} = -Wd_3 + Wd_2 + Wd_1 = 11110 \qquad (1)$$

(a)

(b)

Figure 1. (a) A 4-bit differential SAR ADC and (b) the timing diagram of the SAR ADC.
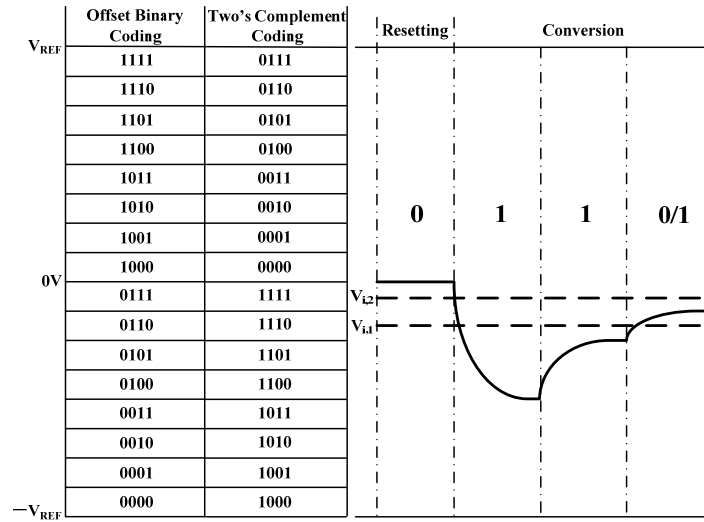
Figure 2. The output data formats and the differential output voltage waveform of the DAC.

The result of the last comparison, which is performed after the switching of C_1, is useful. However, there is no capacitor that is switched after the switching of C_1. The result given in Equation (1) cannot be taken directly as the final output code of the 4-bit SAR ADC. To solve this problem, a virtual capacitor C_V is introduced with digital weight Wd_V = "00001", which is half of the digital weight of the LSB capacitor. If the last comparison indicates that $V_{DACP} > V_{DACN}$, the digital weight of the virtual capacitor should be subtracted from the output code, and vice versa. In the above example, if the input voltage is $V_{i,1}$, D_{OUT} should be modified as

$$D_{OUT} = -Wd_3 + Wd_2 + Wd_1 - Wd_V = 11101 \quad (2)$$

The higher 4-bit code, which is "1110", is reserved as the final output code. If the input voltage is $V_{i,2}$, the last comparison would indicate that $V_{DAC,P} < V_{DAC,N}$, thus $D_{OUT} = -Wd_3 + Wd_2 + Wd_1 + Wd_V = 11111$. The final output code is 1111, which is also correct.

3. Digital Background Calibration

3.1. Basic Principle

The capacitor array of the DAC shown in **Figure 1** includes eight unit capacitors. The single-ended DAC is redrawn in **Figure 3(a)**. The binary weighted capacitors C_3, C_2 and C_1 are composed of $C_{u,j}$ (j = 4, 5, 6, and 7), $C_{u,j}$ (j = 2 and 3) and $C_{u,1}$, respectively. The initial digital weight of $C_{u,j}$ (j = 0, 1, …, 7) are 00010. In this calibration technique, the termination capacitor $C_{u,0}$ is considered as a standard capacitor and it is the reference capacitor during the calibration. The analog weights of other unit capacitors are compared with that of $C_{u,0}$. If $C_{u,j}$ is larger than $C_{u,0}$, the digital weight of $C_{u,j}$ should be increased, and vice versa. The digital weight of $C_{u,0}$ remains unchanged.

To compare the analog weights of $C_{u,j}$ and $C_{u,0}$, each input signal is quantized twice. **Figure 4** presents the timing diagram. In the first conversion, the schematic of the DAC is shown in **Figure 3(a)**. C_3, C_2 and C_1 are switched sequentially. In the second conversion, $C_{u,0}$ replaces $C_{u,j}$ and $C_{u,j}$ acts as the new termination capacitor. The schematic of the DAC during the second conversion is shown in **Figure 3(b)** assuming that $C_{u,3}$ is compared with $C_{u,0}$. As a result, C_2 is composed of $C_{u,0}$ and $C_{u,2}$ rather than $C_{u,3}$ and $C_{u,2}$. As shown in **Figure 4**, during the second conversion, the switching activities of $C_{u,0}$ and $C_{u,2}$ are triggered after the switching of C_3 whereas $C_{u,3}$ keeps connecting to V_{CM}.

The output code D_{OUT} of each conversion is calculated as following:

$$D_{OUT} = \sum_{j=0}^{M} d_{u,j} \cdot Wd_{u,j} + d_V \cdot Wd_V \quad (3)$$

where $Wd_{u,j}$ is the digital weight of $C_{u,j}$; $d_{u,j} = 1$ or -1 if $C_{u,j}$ is switched from V_{CM} to V_{REF} or GND; $d_{u,j} = 0$ if $C_{u,j}$ acts as the termination capacitor; $d_V = \pm1$ according to the last comparison result; and M is the total number of unit capacitors. The difference between the two conversion results, ΔD_{OUT}, can be used to correct the digital weight of $C_{u,j}$. Two cases are considered in the following.

Case 1: $C_{u,j}$ *is switched from* V_{CM} *to* V_{REF} *in the first conversion.*

In this case, if $C_{u,j}$ is larger than $C_{u,0}$, the DAC output voltage during the first conversion would be larger than that during the second conversion after $C_{u,j}$ or $C_{u,0}$ is switched. Therefore, the output code of the first conversion would be smaller than that of the second conversion, or $\Delta D_{OUT} < 0$.

If $C_{u,j}$ is smaller than $C_{u,0}$, the DAC output voltage during the first conversion would be smaller than that
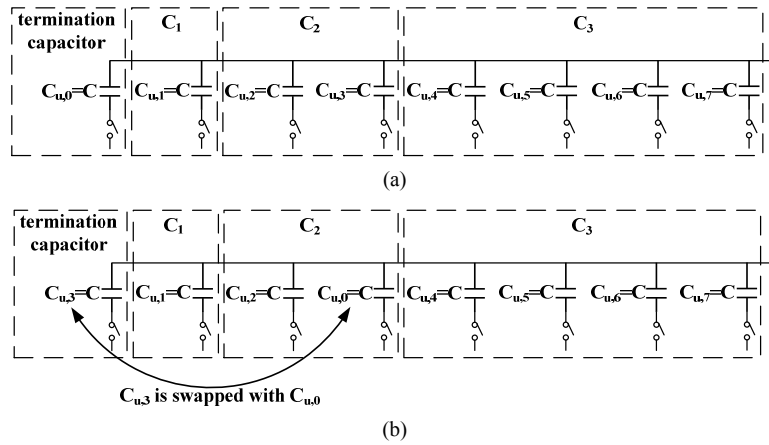
Figure 3. (a) A 4-bit differential SAR ADC and (b) the timing diagram of the SAR ADC.
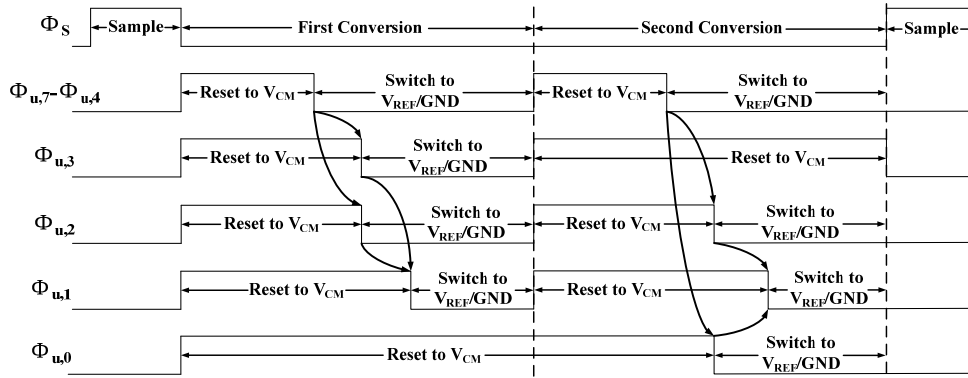

Figure 4. The timing diagram of the DAC shown in Figure 3 when $C_{u,3}$ is under calibration.

during the second conversion after $C_{u,j}$ or $C_{u,0}$ is switched. Therefore, the output code of the first conversion would be larger than that of the second conversion, or $\Delta D_{OUT} > 0$.

In case 1, the LMS (Least Mean Square) update equation that is used to correct the digital weight of $C_{u,j}$ can be written as:

$$Wd_{u,j} [n+1] = Wd_{u,j} [n] - \mu \Delta D_{OUT} \qquad (4)$$

where μ is the convergence coefficient and n denotes the number of corrections. According to Equation (4), if $C_{u,j}$ is larger than $C_{u,0}$, $Wd_{u,j}$ is increased since $\Delta D_{OUT} < 0$; if $C_{u,j}$ is smaller than $C_{u,0}$, $Wd_{u,j}$ is decreased since $\Delta D_{OUT} > 0$. $Wd_{u,j}$ is corrected in the right direction in both situations. When the digital weights of all unit capacitors approach their final values, ΔD_{OUT} is driven towards zero and the calibration process converges.

Case 2: $C_{u,j}$ *is switched from V_{CM} to GND in the first conversion*

In this case, if $C_{u,j}$ is larger than $C_{u,0}$, the DAC output voltage during the first conversion would be smaller than that during the second conversion after $C_{u,j}$ or $C_{u,0}$ is switched. Therefore, the output code of the first conversion would be larger than that of the second conversion, or $\Delta D_{OUT} > 0$.

If $C_{u,j}$ is smaller than $C_{u,0}$, the DAC output voltage during the first conversion would be larger than that during the second conversion after $C_{u,j}$ or $C_{u,0}$ is switched. Therefore, the output code of the first conversion would be smaller than that of the second conversion, or $\Delta D_{OUT} < 0$.

In case 2, the LMS update equation that is used to correct the digital weight of $C_{u,j}$ can be written as:

$$Wd_{u,j} [n+1] = Wd_{u,j} [n] + \mu \Delta D_{OUT} \qquad (5)$$

$Wd_{u,j}$ is also corrected in the right direction according to Equation (5).

To reduce the estimation error of $Wd_{u,j}$, the internal code length of the digital weights must be long enough. The unit capacitors are calibrated from $C_{u,1}$ to $C_{u,M}$ sequentially. The calibration process restarts from $C_{u,1}$ after $C_{u,M}$ has been calibrated. The average value of the two conversion results is the final output.

3.2. Calibration Technique with Two Reference Capacitors

The number of unit capacitor increases exponentially as the resolution of SAR ADC increases. For a 10-bit SAR ADC based on tri-level switching, there are 512 unit ca-

pacitors. If all of the unit capacitors are calibrated in the way described above, the layout of the switches array would be complex and the convergence speed would be slow. This paper introduces two reference capacitors into the calibration process to solve this problem.

An 8-bit DAC with two reference capacitors is shown in **Figure 5**. C_i ($i = 0, 1, \ldots,$ and 4) are composed of unit capacitor C_{uA} with a value of C. C_i ($i = 5, 7, \ldots,$ and 9) are composed of unit capacitor C_{uB} with a value of 8C. The parameters to be estimated are the digital weights of $C_{uA,j}$ ($j = 1, 2, \ldots,$ and 15) and $C_{uB,j}$ ($j = 1, 2, \ldots,$ and 31). $C_{uA,0}$ is the standard capacitor for all other unit capacitors. The initial digital weights of $C_{uA,j}$ and $C_{uB,j}$ are 0000000010 and 0000010000, respectively.

Two reference capacitors are involved in the calibration process. They are defined as $C_{R1} = C_{uA,0}$ and $C_{R2} = C_{uA,8} + C_{uA,9} + \ldots + C_{uA,15}$. C_{R1} and C_{R2} are the reference capacitors for $C_{uA,j}$ and $C_{uB,j}$, respectively. The flow chart of the system is shown in **Figure 6**.

When $C_{uA,j}$ is under calibration ("FLAG" = 1), C_5 acts as the termination capacitor during the two conversions while $C_{uA,j}$ is swapped with C_{R1} ($C_{uA,0}$) in the second conversion, and thus the digital weight of $C_{uA,j}$ is corrected with respect to C_{R1}. When $C_{uB,j}$ is under calibra-

tion ("FLAG" = 2), C_0 acts as the termination capacitor during the two conversions while $C_{uB,j}$ is swapped with C_{R2} ($C_{uA,8}$ - $C_{uA,15}$) in the second conversion, and thus the digital weight of $C_{uB,j}$ is corrected with respect to C_{R2}.

However, C_{R2} is not a standard capacitor as its capacitance is not precisely $8C_{uA,0}$. The digital weight of C_{R2}, which can be expressed as $Wd_{R2} = Wd_{uA,8} + Wd_{uA,9} + \ldots + Wd_{uA,15}$, is constantly updated along with the progress of the calibration. Given that C_{R2} is taken as the reference capacitor for $C_{uB,j}$, $Wd_{uB,j}$ ($j = 1, 2, \ldots,$ and 31) should be updated by the same amount once Wd_{R2} changes. Therefore, each time when $C_{uA,15}$ has been calibrated, the following calculation in the digital domain is conducted:

$$Wd_{uB,j}[n_2+1] = Wd_{uB,j}[n_2] + \Delta Wd_{R2}$$
$$= Wd_{uB,j}[n_2] + \left(\sum_{j=8}^{15} Wd_{uA,j}[n_1] - \sum_{j=8}^{15} Wd_{uA,j}[n_1-1] \right) \quad (6)$$

where n_1 and n_2 denote the number of corrections for $Wd_{uA,j}$ and $Wd_{uB,j}$, respectively. With this method, the number of parameters that need to be estimated is reduced from 255 to 46 for the 8-bit DAC.

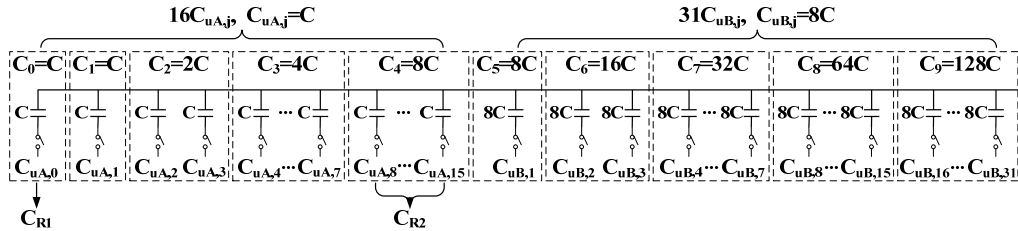With the above calibration technique, Equation (3) is rewritten as:

Figure 5. Schematic of an 8-bit DAC with two reference capacitors.
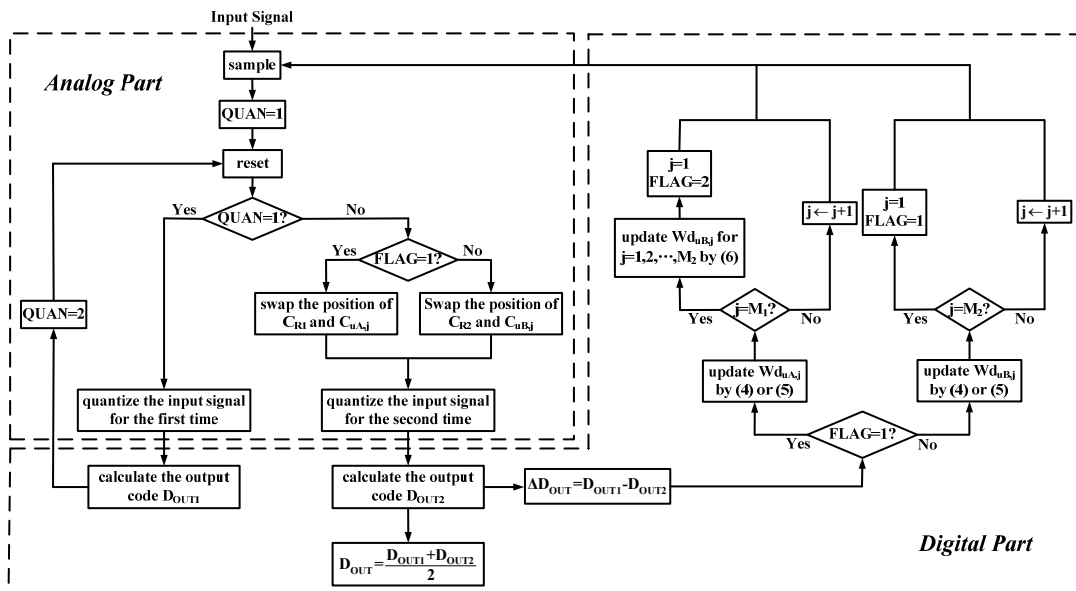

Figure 6. The flow chart of the calibration technique.

$$D_{OUT} = \sum_{j=0}^{M_1} d_{uA,j} \cdot Wd_{uA,j} + \sum_{j=1}^{M_2} d_{uB,j} \cdot Wd_{uB,j} + d_V \cdot Wd_V \quad (7)$$

4. Simulation Results

Behavior modeling and simulation has been performed with a 12-bit SAR ADC to verify the proposed calibration technique. The system structure of a 12-bit SAR ADC is shown in **Figure 7**. The DAC is split into higher 8-bit sub-DAC and lower 3-bit sub-DAC to reduce the total capacitance. The higher 8-bit sub-DAC is the same as that shown in **Figure 5** and the lower 3-bit sub-DAC is a binary weighted capacitor array. $d_{L,j}$ (j = 1, 2, and 3) are the bit decision results of the lower 3-bit. $Wd_{L,j}$ (j = 1, 2, and 3) are the digital weights of the lower 3-bit and they are not updated. Mismatches of C_S and the lower 3-bit capacitors do not deteriorate the ADC performance significantly.

Random capacitor mismatches of 3% were added to all of the capacitors. The internal code length for the digital weights was 26-bit. The convergence coefficient μ was set to 2^{-12}. The learning curve of the Signal-to-Noise and Distortion Ratio (SNDR) is shown in **Figure 8**. With calibration, the SNDR increases from 57.2 dB to 72.2 dB and the Spurious Free Dynamic Range (SFDR) increases from 60.0dB to 85.4dB. After about 700 000 samples, the SNDR converges to a stable value. The variations of $Wd_{uA,1}$ and $Wd_{uB,1}$, which are converted to decimal numbers, are shown in **Figure 9**. The digital weights of all unit capacitors keep stable after they have converged.

5. Conclusion

A digital background calibration technique for SAR ADC is proposed in this paper. Double conversions are carried out for each input sample. As the average value of the two conversion results is used as the final output,
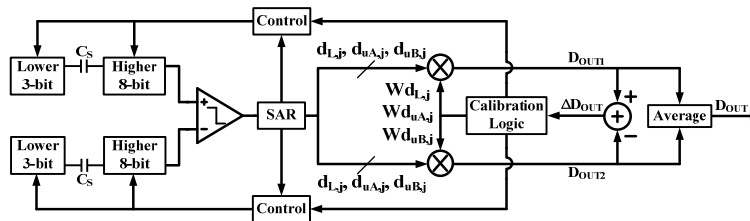

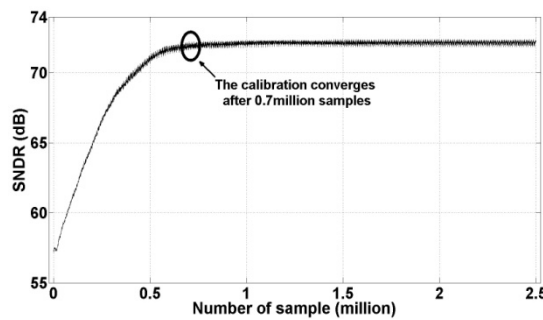Figure 7. The system structure of a 12-bit SAR ADC.
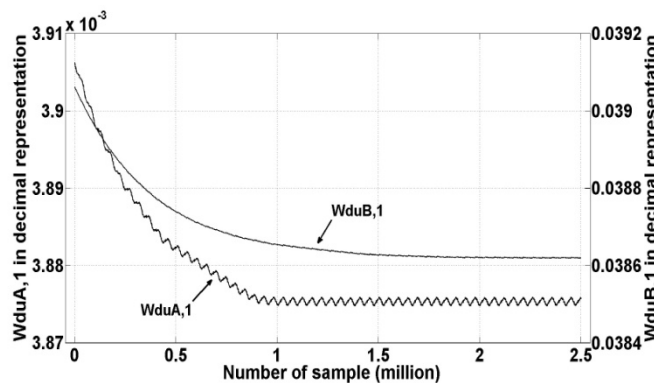

Figure 8. The learning curve of SNDR.

Figure 9. The variations of $Wd_{uA,1}$ and $Wd_{uB,1}$.

the noise power is decreased by 3 dB. With the same principle presented in the paper, the number of reference capacitors can be easily expanded to be more than two to further reduce the number of parameters to be estimated. Behavior simulation results reveal significant improvements in SNDR and SFDR.

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