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Key Issues for Implementing Smart Polishing in Semiconductor Failure Analysis

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Abstract

"Industry 4.0" has become the future direction of manufacturing industry. To prepare for this upgrade, it is important to study the automation of semiconductor failure analysis. In this paper, the sample polishing activity was studied for upgrading to a smart polishing process. Two major issues were identified in implementing the smart polishing process: the optimization of current polishing recipes and the capability of making decisions based on live feedback. With the help of Solver add-in, the current polishing recipes were optimized. To make decisions based on live images captured during polishing, strategies were explored based on finger polishing process study. Our investigation showed that a grey scale line profile analysis on images can be used to build the vision capability of our smart polishing system, on which a decision-making capability can be developed.

Keywords

Semiconductor Process Optimization, Failure Analysis, Image Process, Grey Scale Line Profile Analysis, Smart Polishing System

1. Introduction

Failure analysis (FA) is one of the most important sectors in modern integrated chip (IC) fabrication. Wherever there is a failure limiting production yield or causing chip malfunction, root cause and failure mechanism analysis is needed so as to improve the manufacturing process as well as the product yield. Therefore, FA with high quality is always critical and indispensable for semiconductor industry. Generally, FA on IC chips or wafer pieces can be categorized into physical FA (PFA) and electrical FA (EFA). The former requires layer by layer inspections from top-most layer down to the layer where the defect lies or to the

substrate level, with an optical microscope or scanning electron microscope (SEM). The latter, however, includes a lot of special techniques such as nano-probing, photo emission, thermal analysis by which the suspected failure location will be isolated for further analysis.

IC chips can be considered as films stacked on silicon substrates. As the defect is usually embedded deep inside the film layers, in most of the cases, a few film layers have to be removed before the defect can be revealed or an EFA can be performed, and this is usually achieved by sample polishing. Obviously, FA quality is directly linked to how well the sample is prepared. The most common method for sample preparation is finger polishing, during which the engineer polishes the sample by pressing it against a rotating platen covered by a certain cloth with slurry supplied in between the sample and the cloth. Finger polishing is simple and flexible, however, its quality is heavily dependent on engineer's experience.

Since the term "Industry 4.0" emerged in 2011 [1], it has become more and more widely accepted and the manufacturing industry is gradually transforming into "smart factory". To cope with this trend and get well prepared for the next generation of FA, it is of great urgency to study the automation of all FA techniques. In GlobalFoundries Singapore, a prototype smart polishing system with fully automation is currently being built up. Its major hardware consists of a robotic arm and a polisher. To implement the smart polishing process, some key issues must be solved. Two major issues we have identified are the optimization of current polishing recipes and the capability of making decisions based on live feedback during polishing. In this paper, optimization on the current finger polishing process will be discussed, which will be used for polishing recipe builder programming. Strategies of process and analysis on images obtained from sample polishing will also be discussed, which will lay the foundation for the smart polishing system's decision making capability.

2. Polishing Process Optimization

2.1. Problem Background

Polishing process is to remove unwanted material away with mechanical forces. Usually, a slurry containing abrasive particles is used to enhance the material removal rate. Moreover, the chemistry of slurry may induce reactions with the sample surface which can help in generating a new layer easily to be peeled off. A simple illustration of polishing process is shown in **Figure 1**. Before the sample contacts the cloth, the abrasive particles and slurry solution are spread over the polishing cloth.

As shown in **Figure 1**, when the sample is pressed down to the cloth surface, some abrasive particles will be trapped at the top of the cloth asperities and in contact with the sample surface. These particles are called effective abrasive particles. It can be seen from this figure that the total area in contact with sample surface will determine the total amount of effective abrasive particles, which will

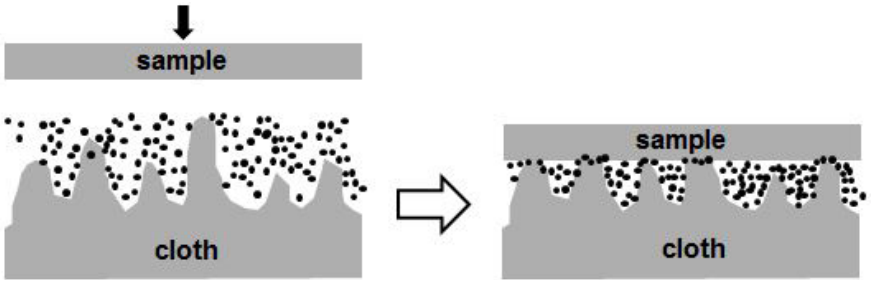

Figure 1. Effective abrasive particles in the polishing interface.

affect the material removal rate (MRR). If the force applied is larger, the contact area will increase; however, the increment is not linear and there will be a maximum value (theoretically will be the sample's surface area).

MRR can be used to gauge the polishing process. There are several parameters affecting MRR such as pressure or force applied, slurry type (average diameter of the abrasive particles), platen rotation speed and time used. Conventionally, the Preston equation is adopted to predict the MRR [2]:

$$MRR = K_p \cdot P \cdot V \,. \tag{1}$$

where P is the force applied, V is the relative velocity and K_p is a general coefficient which represents the combined effects of the remaining parameters and can be determined experimentally. The Preston equation can only provide a linear prediction of the variation in the MRR, however, lots of studies have shown that the real MRR during polishing is nonlinear [3]-[11]. In order to simplify our model, we varied the force applied only with three different levels while kept the other parameters fixed. In other words, we only have three different MRR values in our model.

Table 1 lists the MRR at different force level based on experiments.

It can be seen from **Table 1** that higher force can bring high MRR value, thus shorter time for the polishing process. However, high force usually brings more scratches to the sample surface which is not preferred as the sample needs to be inspected. Based on experience, once a high force applied, a mid force polishing for 60 s is necessary to undo the possible damages induced by high force polishing. The same is true for mid force and in this case, the 60 s low force polishing will be necessary. In order to have the best surface quality, low force polishing for 60s is needed to achieve a smooth surface for inspection.

To avoid unnecessary damages to the target layer, when the high force is applied, it should be stopped when the target layer is 100 nm away. Similarly, for mid force, 50 nm will be the safety distance.

In summary, to achieve high MRR, high force is preferred; however, low force is required for surface quality concern. These two are contradicting with each other and optimization is needed to get the best solution.

2.2. Optimization of Polishing Process by Excel Solver

Optimization on polishing process is performed with Microsoft's Excel Solver

add-in. Based on the background information above, we have listed the critical parameters for modeling in **Table 2**, including the MRR values. A set of constrains based on the requirements are added to the model. Using a global nonlinear search method, the Solver can give us the optimized results.

The equations used to build the model in Solver can be expressed as:

$$\text{Purpose:To find minimum of } (t1+t2+t3). \tag{2}$$

$$t1\cdot 8+\left(t2+t_{add2}\right)\cdot 2+\left(t3+t_{add3}\right)\cdot 0.4\geq \text{target thickness to be removed} \tag{3}$$

$$t_{add2}=0 \text{ if } t1=0, \text{ or } t_{add2}=60 \text{ if } t1\neq 0. \tag{4}$$

$$t_{add3}=0 \text{ if } t2+t_{add2}=0, \text{ or } t_{add3}=60 \text{ if } t2+t_{add2}\neq 0. \tag{5}$$

$$t1,t2,t3 \text{ are integers and } t1,t2,t3\geq 0,\ \ t3+t_{add3}\geq 60. \tag{6}$$

Equation (3) needs to be adjusted according to real case, as we don't want to over-polish the sample too much.

With this model, we can predict the time needed to remove a certain thickness (amount) of material, which is illustrated in **Figure 2**.

It can be seen clearly from **Figure 2** that the relationship between polishing time and removed material thickness is not linear. An exponential fitting was performed by Excel and the fitted equation is shown in **Figure 2**. The fitting is close to data points, but the variation becomes more and more obvious when the thickness is larger and larger.

Now let's use a typical IC device as a real example. The cross-section illustration of a 40nm IC chip with 6 stacking film layers is shown in **Figure 3**.

Before polishing is started, layer 6 with SiO_2 has been removed and only low-k films left. Usually the last two layers (film 1 and 2 in **Figure 3**) are important and we normally start inspection from there. The problem now becomes how to remove three low-k layers efficiently. To include some over-polishing allowance, the total removal thickness is set to be between 580 to 620 nm. Therefore, Equations (2) to (6) can be written as:

$$\text{Purpose:To find minimum of } (t1+t2+t3). \tag{7}$$

$$t1\cdot 8+(t2+t_{add2})\cdot 2+(t3+t_{add3})\cdot 0.4\geq 580. \tag{8}$$

Table 1. Average MRR at different force levels.

Force Level	High	Mid	Low
Average MRR, nm/s	8	2	0.4

Table 2. Parameters for polishing process model.

Parameter Name	Value/Range		
Force Level	F1, High	F2, Mid	F3, Low
Time, s	t1	t2	t3
Additional Time, s	n.a.	t_{add2}	t_{add3}
MRR, nm/s	8	2	0.4

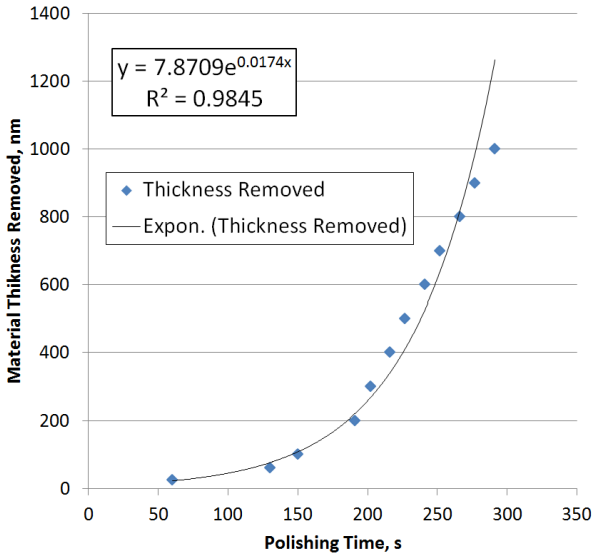

Figure 2. Predicted polishing time for removing a certain amount of material.

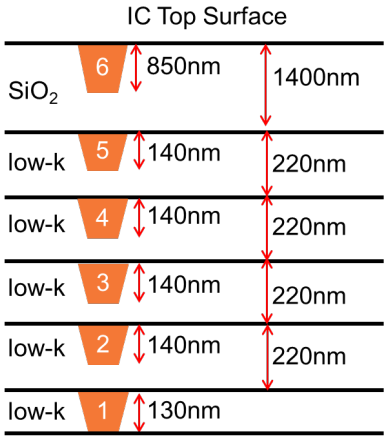

Figure 3. Film stacking structure of a typical 40 nm IC chip.

$$t1\cdot 8+(t2+t_{add2})\cdot 2+(t3+t_{add3})\cdot 0.4\le 620\,. \tag{9}$$

$$t_{add2}=0 \text{ if } t1=0, \text{ or}, t_{add2}=60 \text{ if } t1\neq 0\,. \tag{10}$$

$$t_{add3}=0 \text{ if } t2+t_{add2}=0, \text{ or } t_{add3}=60 \text{ if } t2+t_{add2}\neq 0\,. \tag{11}$$

$$t1,t2,t3 \text{ are integers and } t1,t2,t3\ge 0,\ t3+t_{add3}\ge 60\,. \tag{12}$$

With Equations (7) to (12), we can find solutions with the Solver add-in.

Table 3 shows the solution provided by Solver and **Table 4** is the recipe currently used by engineers. It can be seen from **Table 3** and **Table 4** that the polishing time has been shortened from 410 s to 237 s, about 42% in reduction. Verification experiments show very good consistence with the prediction.

This example shows that we can optimize the polishing recipes with a proper modelling and the optimized solutions can be gathered as a recipe library for our smart sample polishing system.

Table 3. Solution for polishing three low-k layers found by Solver.

Parameter Name	Value/Range		
Force Level	F1, High	F2, Mid	F3, Low
Time, s	51	1	60
Additional Time, s	0	60	60
Materials Removed, nm	408	122	50
			Total Time: 237 s

Table 4. Recipe for polishing three low-k layers based on experience.

Parameter Name	Value/Range		
Force Level	F1, High	F2, Mid	F3, Low
Time, s	30	60	200
Additional Time, s	0	60	60
Materials Removed, nm	240	240	104
			Total Time: 410 s

3. Smart Polishing System and Real-Time Decision Making Strategy

One of the important designed features for the smart polishing system is that it can adjust the polishing parameters based on real-time sample situation. That means, during the polishing process, the system will check the sample's status and adjust the polishing recipe accordingly.

Figure 4 shows the planned configuration of our smart polishing system. The main concept is to use a robotic arm to simulate the finger polishing process. A CCD camera will capture the sample surface status during polishing. Images taken by the camera will be processed and analyzed by our software specially programmed for the system. Based on the live feedback images, the software will evaluate the situation and make decisions for what to do next, so as to ensure the outcome of the polishing process is as expected.

Since the robotic arm is used to simulate finger polishing process, we would like to study how the FA engineer controls the polishing process first and then transfer the learnings to the smart system action designing. One important action during finger polishing is status check after polishing for a while. Based on the sample surface morphology evolution and pattern recognition, the FA engineer can tell if the polishing goal has been achieved. **Figure 5** shows the sample surface pattern evolution during finger polishing process. It can be seen from this figure that the pattern is getting irregular with several new features formed after polishing. Our study here is trying to generate useful information from these newly generated features.

There is one important feature in **Figure 5** worth highlighting that there are several ripples formed near the left edge of the graph after polishing for a while.

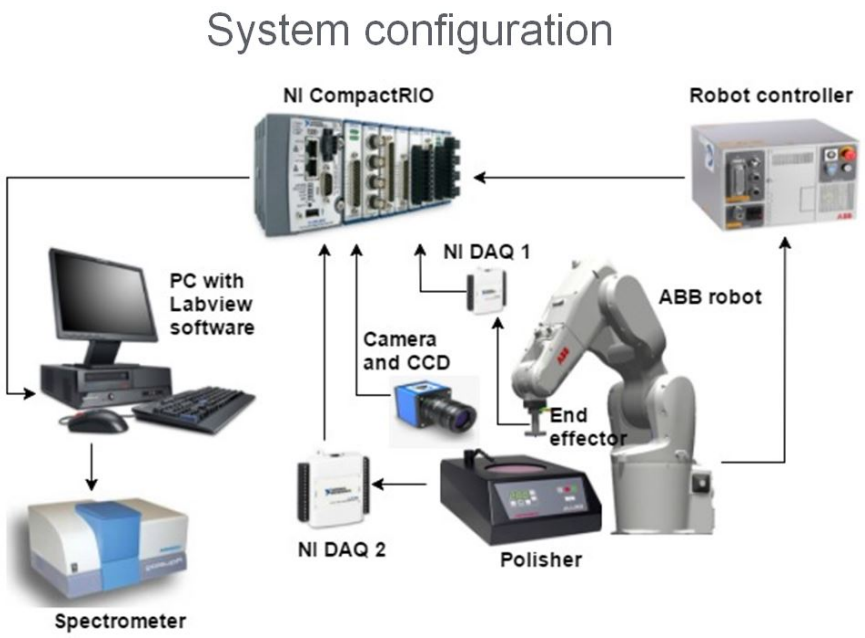

Figure 4. Smart polishing system configuration.

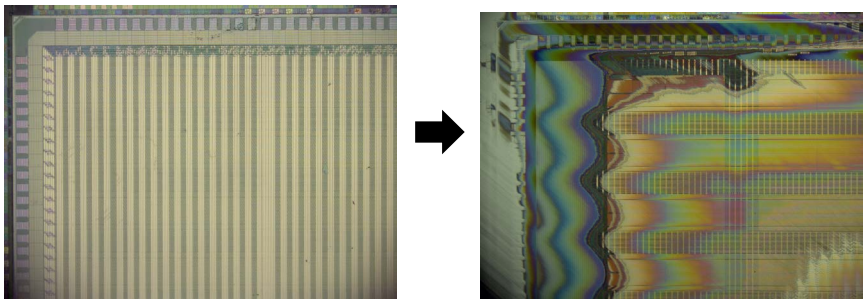

Figure 5. Surface pattern evolution during polishing process.

This phenomenon is not unusual during polishing process and the ripples are related to the IC's stacking film structure. In fact, we can identify which film the ripple stands for by counting its sequence from the left-most edge (bare silicon surface). To make this clear, we can use the stacking structure in **Figure 3** as an example, as illustrated in **Figure 6**. Please be noted that **Figure 3** and **Figure 5** are not the same IC chip and only layer 1 and 2 match with the ripples in the current case.

The ripple counting approach stated above is exactly how our FA engineers evaluate the polishing progress. We would like to adopt this ripple identification method to the smart polishing system so the system can evaluate the sample overall situation and find out what to do next, in order to achieve the polishing goal. Obviously this requires lots of image processing and information extraction work, as well as decision-making network to conclude from the information obtained. Here, we will explore the image process and the decision-making strategies based on the information extracted.

As colors in images will vary when the light intensity or bulb type in micro-

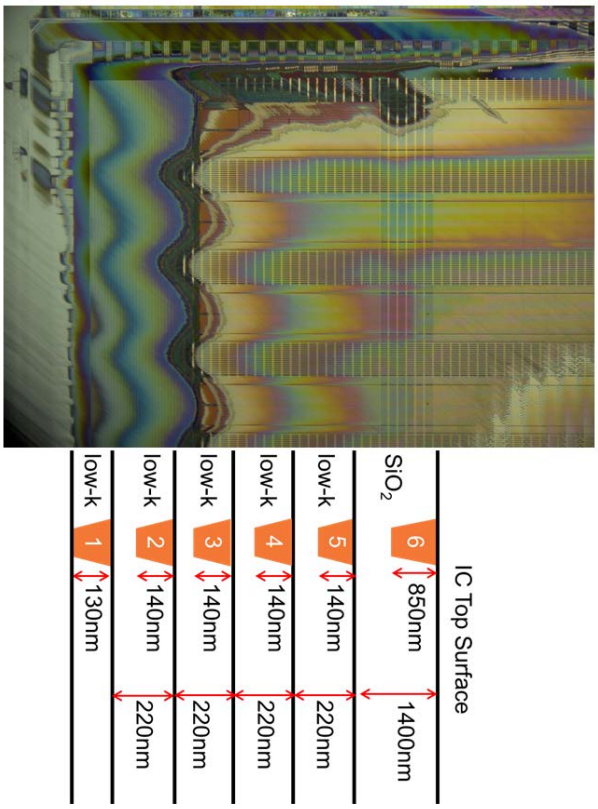

Figure 6. Relationship between ripples and film stacks.

scope changes, we will firstly convert the colored images into grey scale graphs by extracting the color plane information. After that, we will check the grey scale values along a line across the ripples, *i.e.*, line profile check.

Figure 7 illustrates the line profile analysis using NI Vision Assistant. The grey scaled image is under analysis and a sampling line across the ripples is drawn to do the profile check on grey scale values. The small graph at the left bottom corner shows the gray scale value along the sampling line.

If we take a closer look of the line profile graph in **Figure 7**, several deep valleys can be seen, which stand for the ripple to ripple interfaces. To make this clearer, the profile graph is aligned with the grey scale image in **Figure 8**. It can be seen from this figure that the grey scale profile can be used to extract the ripple pattern information and each ripple can be correlated to a specific peak on the line profile curve.

As stated in previous analysis, the ripples on sample surface actually stand for the different film stacking structures left on the sample after polishing. In other words, ripples are corresponding to different sample thickness. Therefore, if we have identified which peak stands for the target thickness (as indicated in **Figure 8**), we can check whether or not the polishing speed or MRR is within designed specifications by monitoring the movements of the identified grey scale peak. This information can help the smart polishing system to decide what adjustment should be made to control the final polishing outcome.

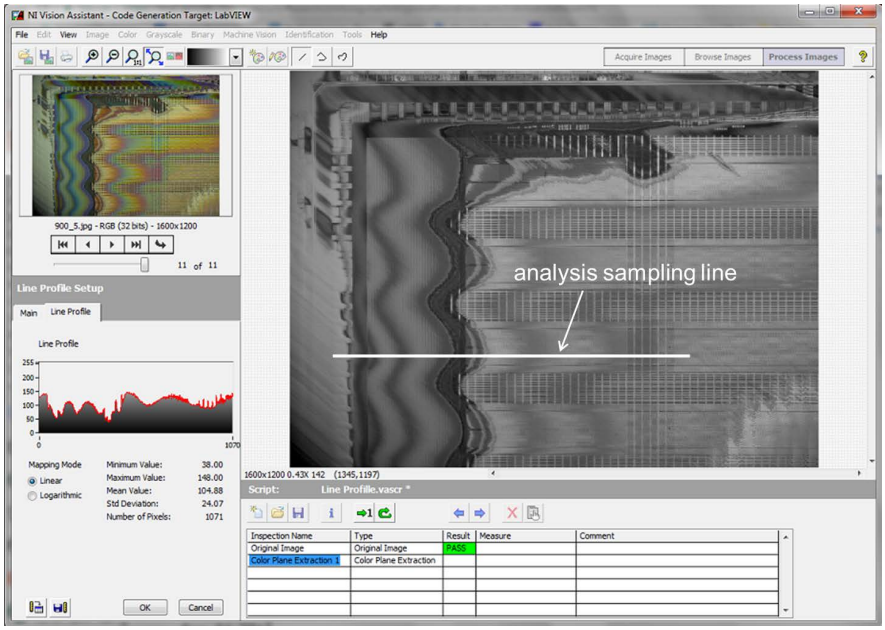

Figure 7. Image processing software interface.

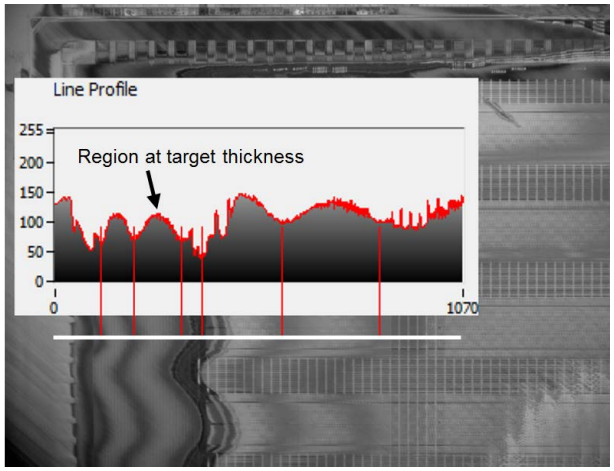

Figure 8. Grey scale line profile and ripple pattern comparison.

If the sampling line on **Figure 7** is drawn at an already known starting point on the chip, the physical coordinates of the IC chip surface will be mapped to the sampling line. Thus the region of interest (ROI) on the sample can be located in the sampling line and the smart polishing system can use this information to judge whether or not the polishing goal (ROI reaches target thickness) has been achieved. Software subroutine based on this strategy is currently being programmed and tested.

The example above clearly shows that grey scale line profile analysis can be used in extracting useful information from images obtained during sample polishing. More case studies are needed to validating the image processing and strategies on different samples.

4. Conclusions

The implementation of smart polishing requires the integration of a lot of hardware parts as well as software modules to make it intelligent. There are a lot of important issues which determine the performance of the whole system. We discussed two major issues here for the fundamental study in building up the core functions. The optimization of polishing process demonstrated here can help us to improve the efficiency. Image process and analysis strategy based on grey scale line profile analysis is very promising in realizing the smart system's vision capability, on which the decision-making capability based on live feedback can be developed.

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