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Real-Time Video Transmission of Visible Light Communication Based on LED

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Abstract

In order to realize the video image transmission and the excellent lighting function of the visible light communication system, a LED-based visible light communication method and system is proposed. Based on the field programmable gate array (FPGA) hardware, the RS channel coding is applied to the visible light communication system. A pulse position decision algorithm is proposed, which is applied to the receiver of the visible light communication system to meet the error-free decision of the signal. The design of the system is based on the analog-to-digital conversion circuit, which provides a large signal dynamic range for the pulse position decision algorithm, and designs the LED driver based on the bias circuit to realize the fast broadband modulation of the signal. The test results show that the combined application of pulse position decision algorithm and Reed-Solomon codec can reduce the error of system signal and meet the real-time and reliable transmission of signal. The system can display the received video in real time from the receiver, and the whole system communication distance up to 5 m.

Keywords

Visible Light Communication, LED, Reed-Solomon, Pulse Position Decision, Video Transmission

1. Introduction

This template, created in MS Word 2007, provides authors with most of the formatting With the LED equipment and craft work updating, visible light communication based on LED technology is becoming a key research direction of wireless optical communication [1]. The previous studies focus on the simulation of modulation and coding, as well as the conceptual experimental demonstration, the purposes are to achieve fast and strong anti-interference ability of VLC system [2] [3]. Based on the previous research, this treatise proposes a

pulse position decision algorithm and combines the RS coding method to improve the reliability and effectiveness of VLC system, which both based on FPGA to realize. At the same time, the driver circuit of LED and amplifying circuit are designed, the real-time video is processed in this paper, finally at the receiving end can display the monitors information from the transmitting end. The dual functions of visible light communication system about lighting and communication both realized in this paper.

2. Transmitter Design

Through the real-time video acquisition, the analog video signal is converted into digital signal, the signal processing is mainly completed on the FPGA platform, STM32 as the main control device. The camera collects real-time video information, and converts it into digital component by analog-digital composite video decoder (TW2867). The decoder integrates anti aliasing filter and COMS analog to digital converter, as well as the PLL can output 108 MHz clock, programmable tone, saturation, sharpness and other parameters. The transmitter achieves the function of video acquisition and conversion. Principle diagram of the transmitting terminal is as shown in **Figure 1**.

2.1. Signal Processing of Transmitter

RS encoding method has excellent characteristics, strong correction ability and higher efficiency in the linear block code, the group code length is short with good performance [4]. RS (15, 9) encoding can be used to deal with burst errors in visible light communication. Based on the finite field GF (24), the block length n is 15 ($2^4 - 1$), the message length k is 9, the parity length e is n-k therefore is 6, the maximum error correction capability t is 3, the minimum code distance d is 7.

The generate polynomial expression is:

$$\boldsymbol{g}(x) = x^6 + 7x^5 + 9x^4 + 3x^3 + 12x^2 + 10x + 12 \tag{1}$$

The native original polynomial expression is:

$$\boldsymbol{p}(x) = x^4 + x + 1 \tag{2}$$

Therefore, the resulting matrix is:

$$G = [I_k\, p] = \begin{Bmatrix} 1 & 0 & \ldots & 0 & 0 & x^{n-1} (\mathrm{mod}\, g(x)) \\ 0 & 1 & \ldots & 0 & 0 & x^{n-2} (\mathrm{mod}\, g(x)) \\ \vdots & \vdots & \ldots & \vdots & \vdots & \vdots \\ 0 & 0 & \ldots & 0 & 1 & x^{n-k} (\mathrm{mod}\, g(x)) \end{Bmatrix} \tag{3}$$

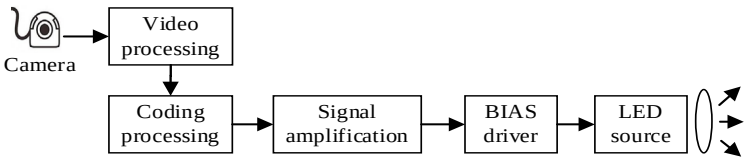

Figure 1. Principle diagram of the transmitting terminal.

According to the above formula, the formula after encoding is:

$$C(x) = x^r u(x) \bmod g(x) + x^r u(x) \tag{4}$$

where x is the original element, and t is the error tolerance, $x^r u(x) \bmod g(x)$ represents the remainder of $x^r u(x)$ divided by $g(x)$.

The native original polynomial expression can be calculated by the regenpoly instructions in Matlab. In the FPGA encoding circuit is designed based on $g(x)$ multiplication or division method. The structure is realized by the current shift register structure, in which the adder is exclusive OR and not-carry, multiplier into the form of modulo two sums. The algorithm is constructed by the function [5]. The coding structure is shown in **Figure 2**.

2.2. Driving Circuit Design

Designed with Bias-T driver circuit, with ultra-high bandwidth, and can achieve analog digital dual-signal modulation. Light source drive circuit shown in **Figure 3**, the FB pin of constant current bias chip is the voltage loop feedback pin, combine with its peripheral circuit for constant voltage regulation, protecting LED and so on [6] [7]. ISP pin is the current feedback resistor of the positive connection terminal, can protect short circuit. ISN is the current feedback resistor negative connection terminal, the Bias-T drive circuit make light source work in the linear work area, the electrical signal superimposed on the DC bias.

According to the AC frequency of capacitor and inductance, fC = 1/(2πRC)

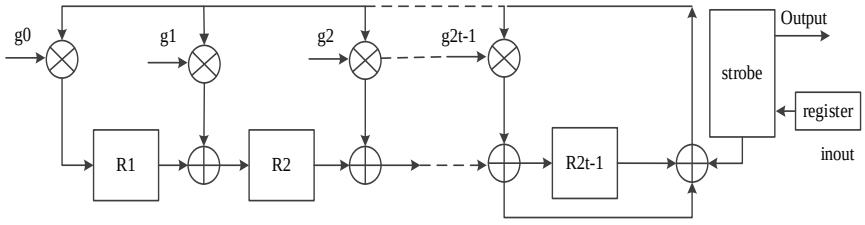

Figure 2. RS coding assumption diagram.

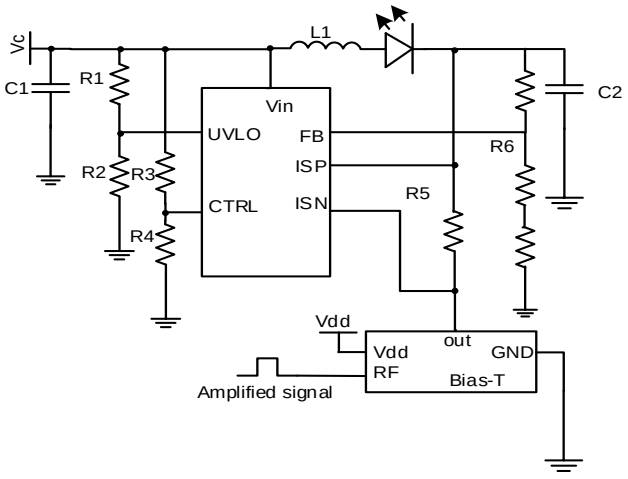

Figure 3. LED driver circuit.

and fL = R/(2πL), the light source and load in series. Capacitance, assembling capacitor and inductance and series 50 Ω matched microstrip lines, to reduce the return loss to expand the bandwidth to ensure the signal fidelity.

3. Receiver Design

The main function of the photoelectric detector is achieving the received optical signal to the electrical signal conversion, recover the video signal and display the real-time video at the end of receiver. The structure of receiver is shown in **Figure 4**.

3.1. Receiving Circuit Design

The characteristics of the amplifier circuit shows that the first level of amplification is particularly important, while the noise is also amplified, so the circuit requires a low noise amplifier chip. The chip selection should take into account the characteristics of high bandwidth and in-band gain stability. So the circuit uses a high gain bandwidth, low noise voltage feedback amplifier (OPA2846), receiver amplifier circuit shown in **Figure 5**. The amplified signal still has the form of an analog signal, so the signal is sampled by the modulo sampling circuit module to provide a larger signal dynamic range for the signal decision. The AD9280 chip has the characteristics of high speed processing ability and low power consumption. The sampling circuit is composed of AD9280 and the attenuation circuit.

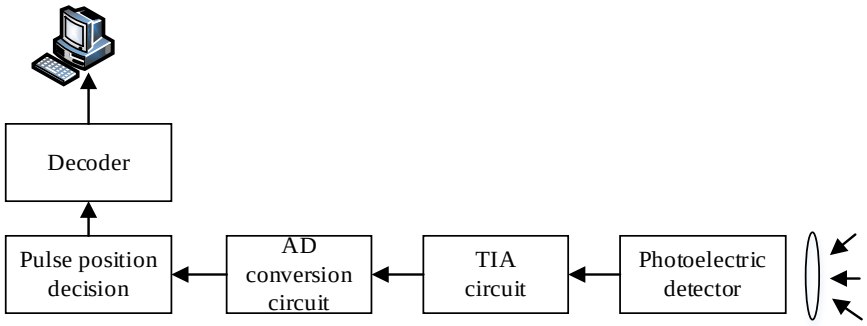

Figure 4. Principle diagram of the receiving terminal.

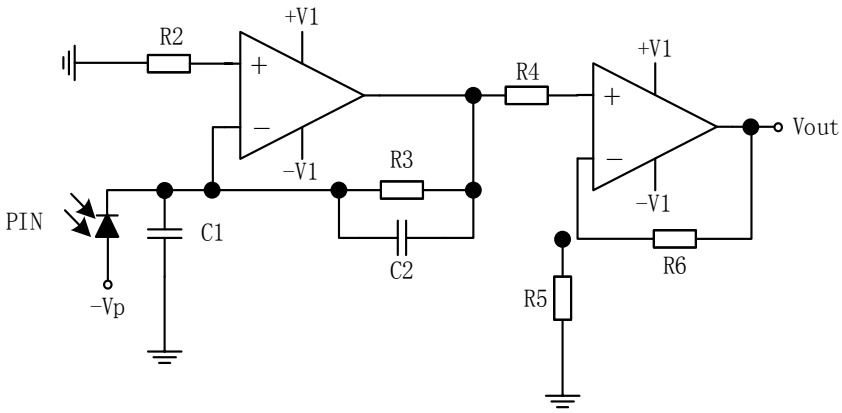

Figure 5. Amplifier circuit of the receiving terminal.

3.2. Signal Processing of Receiver

The signal received by the experiment still has the form of an analog signal, so the data is processed according to the sampling data provided in the previous chapter. In order to provide a larger dynamic range for the signal, and to ensure the correctness of the subsequent signal processing, the sum of the adjacent sampling pulses is summed in the FPGA to prevent two or more miscarriage of justice in one frame of data. Improve the reliability of communication systems. The implementation process is shown in **Figure 6**.

The design of the RS decoder consists of a syndrome calculating circuit, a key equation solving circuit, a Chien search circuit and a Forney algorithm circuit and so on [8], the logic circuit is shown in **Figure 7**. First, for the solution of syndrome calculating circuit, and the value of the syndrome S is actually calculated by the receiver symbol polynomial $R(x)$, each value of the generator polynomial $g(x)$ is substituted into $R(x)$ to find the polynomial. The circuit is parallel to the 6-way solution to syndrome. On the error value detection, if the value of syndrome calculating circui is 0, there is no error, otherwise there is error. The finite

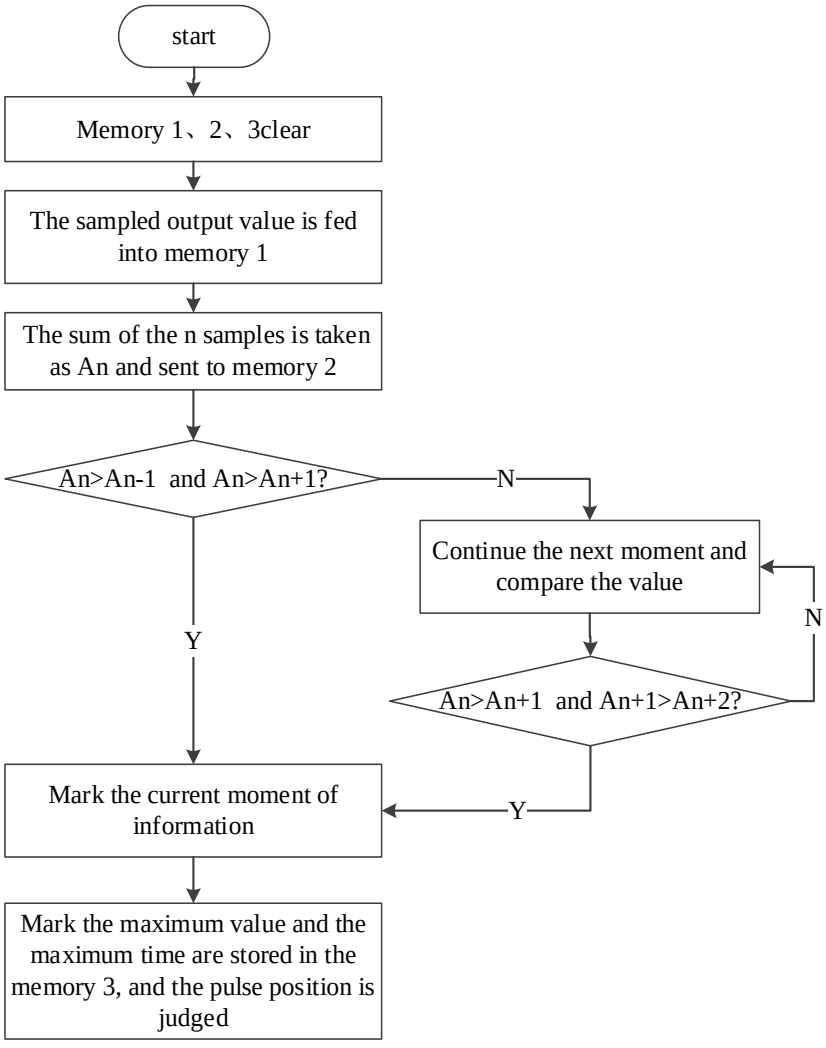

Figure 6. Pulse position decision realization process.

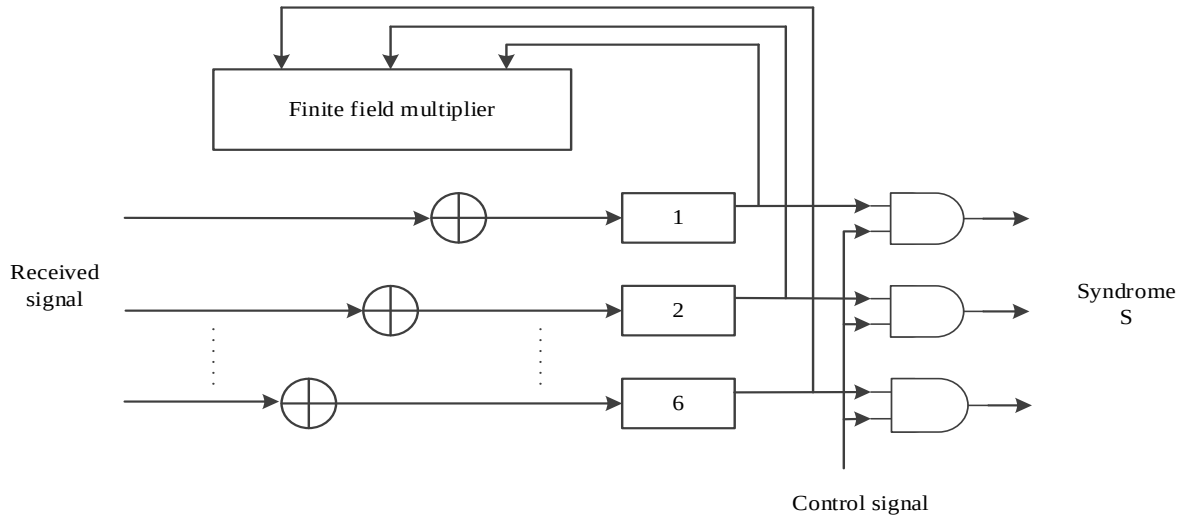

Figure 7. Syndrome calculating circuit.

field multiplier in **Figure 7** uses MATLAB to calculate the constant coefficient multiplier, which is efficient and can improve accuracy, and the result can be saved as a.v format.

If the symbol is wrong, then the error from this step to find. For the solution of key equations, the key equation is $S(x)\sigma(x) = \omega(x)\bmod x^{2t}$, $\sigma(x)$ is the error position polynomial, and $\omega(x)$ is the error value polynomial. In the operation, the data is initialized and the current syndrome is updated by the internal memory of the calculation unit [9]. One iteration for each clock cycle, and the result can be outputted until the iteration ends. Inversion of the results yields the coefficients of $\omega(x)$ and $\sigma(x)$.

After the above calculation, the error position and the error value are required. The error position is actually the value of $\sigma(x)$. As shown in **Figure 8**, the Chien search method verifies whether $\sigma(x^l)$ (l = 0, 1, ···, n) is 0, that is, find the value by verifying each r_{n-1} to determine the location.

$$\sigma'(x) = \frac{d[\prod_{l=1}^{v}(1-\beta_l x)]}{dx} = -\sum_{k=1}^{v}\beta_k \prod_{l=1,l\neq k}^{v}(1-\beta_l x) \tag{5}$$

$$\sigma'(\beta_k^{-1}) = -\beta_k \prod_{l=1,l\neq k}^{v}(1-\beta_l\beta_k^{-1}) \tag{6}$$

The final output is the correct source code, the input data and error data through the XOR logic operation, the correct source data can be got. Debugging delay circuit and XOR operation circuit, it is necessary to delay the error data, only the correct delay period makes the data not aligned, the final decoding data can be obtained.

4. Experimental Testing and Analysis

4.1. Data Information Test

Based on FPGA of EP4C515F17C8N to achieve the pulse of the hardware mod-

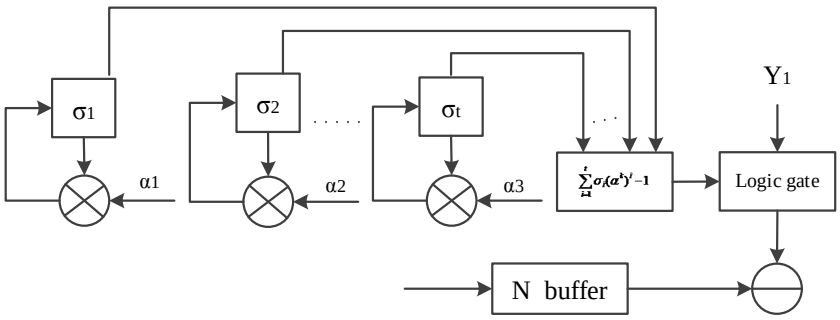

Figure 8. Chien search circuit.

ulation, the original signal is first sent to the register cache, driven by the drive circuit to the light source to send out; receiver sampling circuit using AD9280 chip of AD, the maximum sampling frequency of 32 Msps, using logic analyzer to simulate to meet the signal dynamic range of the pulse decision algorithm. The test results are shown in **Figure 9**.

When the driving circuit module is tested, the square wave signal is generated by a signal generator (SUIN TFG6060). The voltage is 5 Vpp, the signal waveforms are kept good at 20 KHz to 12 MHz, but the square wave signal from 6 MHz starts to narrow at the bottom and the top fluctuation starts to slowly increase. The top and bottom distortion is more serious from 12 MHz, so the test shows that the drive circuit can transmit the OOK signal within 12 Mbit/s and achieve the desired requirements in this article. The oscilloscope (RIGOL DS2202) test results are shown in **Figure 10**.

The amplified circuit is the secondary amplifier circuit at the receiving end. Since the signal measured by the photodetector still has the form of the analog signal, and the signal is almost unchanged through the transimpedance module, the function signal generator is used to generate a sine wave signal for testing; the signal have a gain effect from 6 KHz gradually when changing the frequency during the test, but the waveform is poor; the gain is reduced when the frequency reaches 50 MHz, the effect relatively is best at 35 KHz - 22 MHz. As shown in **Figure 11**, the signal gain waveforms with 5 v and 20 MHz respectively is given, and the gain with 4 V respectively at 20 MHz. From the test results, the linear stability and gain effect are good.

4.2. System Performance Test

Test the performance of the system by testing the eye. In this test method, use the FPGA to generate a way of 300 Kbit/s pseudo-random signal, the modulation method use the key switch modulation. The pseudo-random signal generated by FPGA is loaded into the LED drive circuit, and the oscilloscope is connected directly to the end of the waveform test point and the clock output point. The measured eye diagram of system as shown in **Figure 12**, it can be seen that the eye pattern of receiving end is significantly more open and no overlap between signals, which fully illustrates that the system has good communication ability.

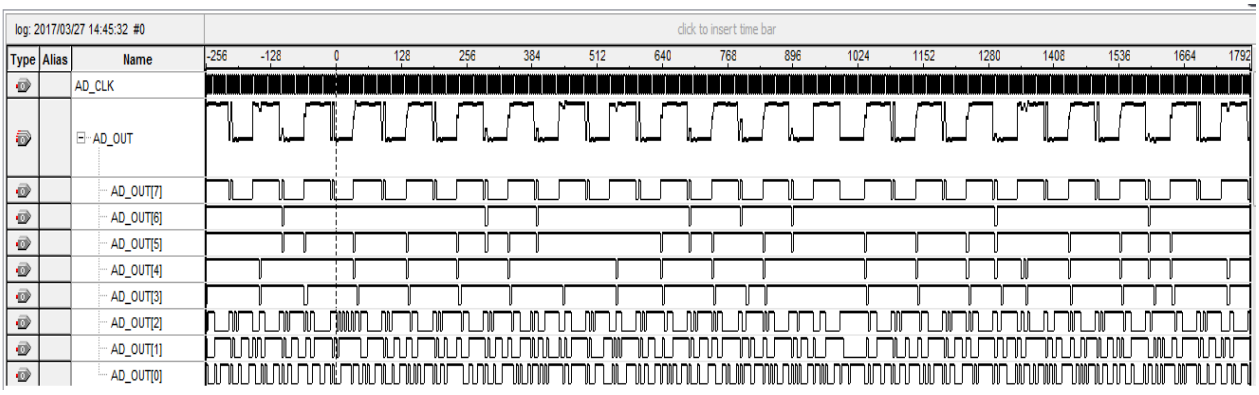

Figure 9. Pulse position signal sampling diagram.

Figure 10. Schematic diagram of drive circuit.

Figure 11. Test results of amplifier circuit.

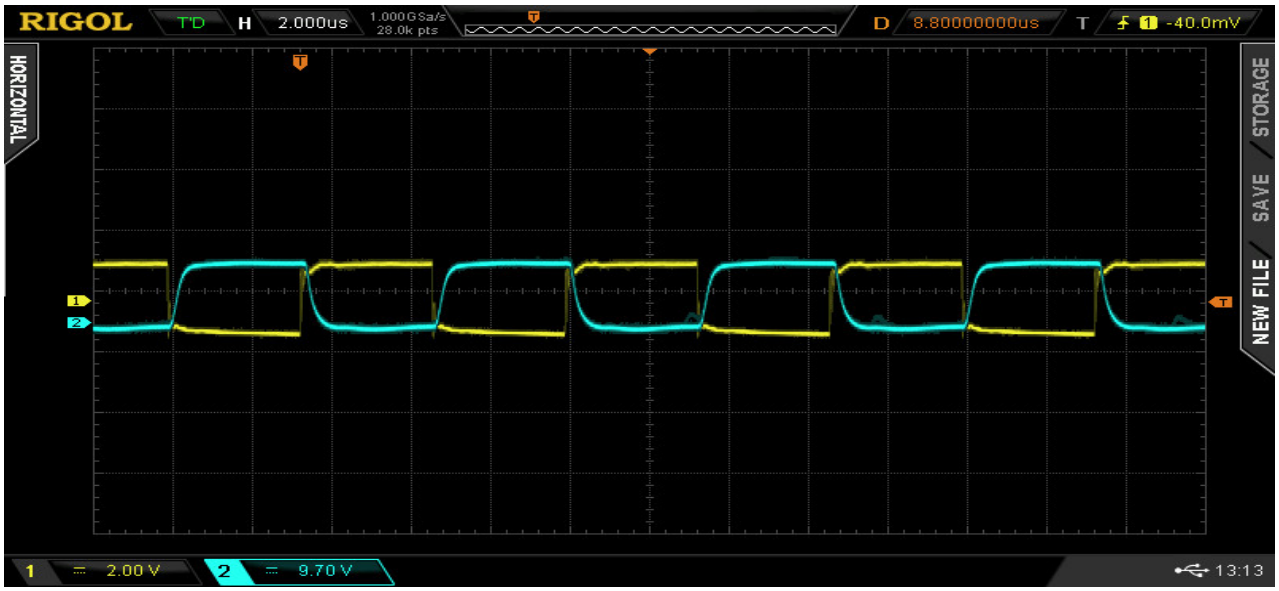

Figure 12. The eye test results of receiving terminal.

Finally, the BER performance of the system is analyzed and the measurement is carried out by using the illuminance meter and the AV5233C error detector. In the test, the angle of the lens is adjusted to match the light intensity of the table, then the intensity of the optical signal is moderate by adjusting the position of the PIN, and the receiving terminal can synchronize signals. The illumination and BER of VLC system is shown in **Table 1**.

From the measurement, when the distance is less than 0.5 meters, the illumination is 42 KLux, photodetector to saturation; at a distance of about 15 meters, the illumination reached 55 Lux, began to appear error, reaching 10 - 8 W. When the distance is more than 25 meters, the error rate is the number of 10 - 6, so we can see that the reliability of the system is good.

4.3. Overall Test

Test chart of video image transmission system is shown in **Figure 13**. 1) shows the test results with background light close-range, using small condensing lens whose focal length is 110 mm and the diameter is 40 mm, it can be seen from the chart display, can display the clear video image in real-time; 2) shows the test results without background illumination, it can be seen that the white LED can provide good lighting for monitoring, but also can realize the video image monitored transmission; 3) shows remote testing, using the lens whose diameter is 102 mm and focal length of 240 mm, the farthest distance can reach 4 meter, and the video can also display at more than 4 m, but the display is not stable at the same time, the video display is not color but gray.

5. Conclusion

Pulse position decision algorithm combined with RS codec using can accurately recover the modulated signal, to overcome the signal misjudgment of the situation

Table 1. The illumination and BER of VLC system.

Performance	Distance/m					
	0.5	1	5	10	15	25
Illumination/lx	42,000	5300	234	102	55	28
BER	-	0	0	0	3.75×10^{-8}	6.30×10^{-6}

(a) (b) (c)

Figure 13. The overall system test.

and improve the reliability of the system. The design of LED driving circuit can drive high power LED with high modulation bandwidth. The sampling circuit can provide a more flexible signal dynamic range for pulse position decision algorithm. On this basis, processing real-time video image, finally the system can transmit real-time video and transmission distance reach 5 meters. Next step can try the three link network model and select APD as the photodetector to improve the transmission distance of the system, at the same time taking into account the effects of temperature and bias.

Acknowledgements

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