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# Ultra-Low Power Designing for CMOS Sequential Circuits

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## Abstract

**Power consumption is the bottleneck of system performance. Power reduction has become an important issue in digital circuit design, especially for high performance portable devices (such as cell phones, PDAs, etc.). Many power reduction techniques have also been proposed from the system level down to the circuit level. High-speed computation has thus become the expected norm from the average user, instead of being the province of the few with access to a powerful mainframe. Power must be added to the portable unit, even when power is available in non-portable applications, the issue of low-power design is becoming critical. Thus, it is evident that methodologies for the design of high-throughput, low-power digital systems are needed. Techniques for low-power operation are shown in this paper, which use the lowest possible supply voltage coupled with architectural, logic style, circuit, and technology optimizations. The threshold voltages of the MTCMOS devices for both low and high $V_{th}$ are constructed as the low threshold $V_{th}$ is approximately 150 - 200 mv whereas the high threshold $V_{th}$ is managed by varying the thickness of the oxide $T_{ox}$. Hence we are using different threshold voltages with minimum voltages and hence considered this project as ultra-low power designing.**

## Keywords

**Ultra-Low Power Design, Dynamic Power, Static Power, Switching Activities, Leakage Power, Power Optimization**

## 1. Introduction

Low power design can be exploited at various levels, e.g., system level, architecture level, circuit level, and

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device level [1]. This paper first gives a brief overview for low power optimization techniques at system and architecture level, reducing power consumption has become an important issue in digital circuit design [1], especially for high performance portable devices. Many power reduction techniques have also been proposed from the system level down to the circuit level. In this section, some of these techniques, which are related to the design for parallel multiplier, will be presented. MTCMOS sleep transistor sizing issues are addressed, and a hierarchical sizing methodology based on mutual exclusive discharge patterns is presented. The multi-threshold CMOS (MT-CMOS) circuit is an effective powering-down scheme in the low supply voltage range, but it needs extra circuits for the data holding in the sleep mode [2], such as the Balloon Circuits or the intermittent power supply scheme.

## 2. Low Power Techniques

### A) Supply Voltage Scaling

To reduce the power consumption, the scaling power supply voltage is most effective method [2]. Reducing the supply voltage can significantly reduce the power dissipation that is a quadratic function of the operating voltage. This is illustrated in **Figure 1**, it represents the power consumption as a function of $V_{dd}$ for a 4-bit carry look-ahead adder in 0.18 μm process technology [3] [4]. The supply voltage for various logic functions and logic styles are dependence on the power consumption.

However, the supply reducing voltage also the delay is increases. The relationship between $V_{dd}$ and the delay, $T_d$, can be expressed as

$$Td = \frac{C_L \times V_{dd}}{l} = \frac{C_L \times V_{dd}}{\frac{\mu C_{ax}}{2}(W/L)(V_{dd} - V_t)^2} \tag{1}$$

From the Equation (1), when $V_{dd}$ approaches the threshold voltage, $V_t$, the delay increases drastically [4], as shown in **Figure 2**. Obviously, using this method causes the performance loss on the speed. In order to compensate for the loss in throughput at low supply voltages, the parallel and pipelined architectures as well as modifying the threshold voltage of the devices can be applied for several techniques.

### B) Reducing Effective Capacitance

When the performance loss in throughput due to lowering the supply voltage is not acceptable. The low power consumption in CMOS circuits can also effective the reducing capacitance. The effective capacitance is defined by the product of the physical capacitance and the switching activity [5], which is shown as

$$C_{\text{effective}} = \alpha_{0\text{-}1} C_L$$

where $\alpha_{0\text{-}1}$ is the node transition activity factor and $C_L$ is the load capacitance which refers to physical capacitance. The switching power consumption can be rewritten as
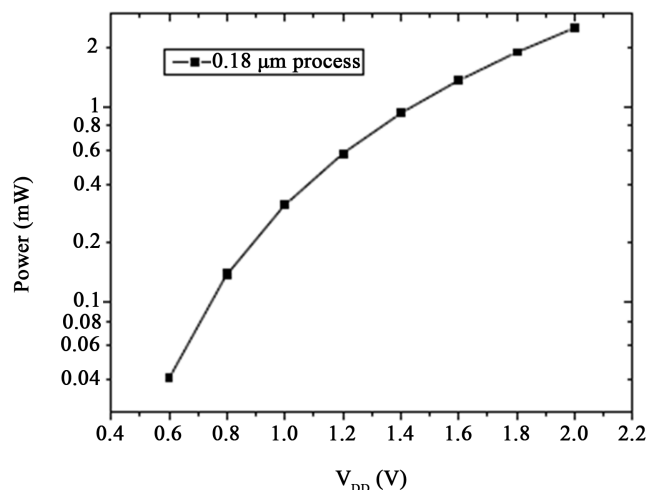


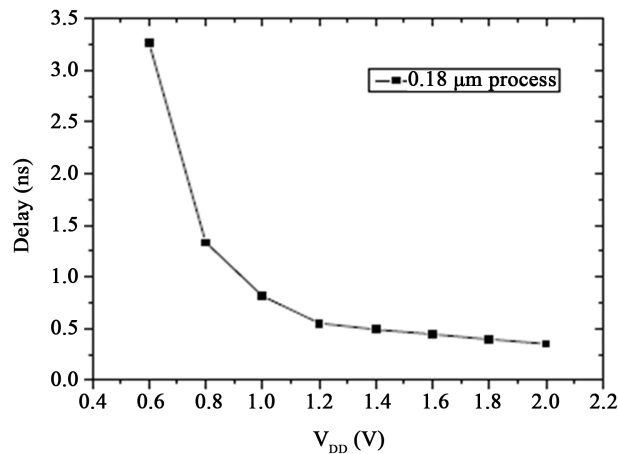**Figure 1.** Power consumption for a 4-bit CLA as a function of $V_{dd}$ [1].

**Figure 2.** Propagation delay versus $V_{dd}$ for a 4-bit CLA adder [3].

$$P_{\text{switching}} = C_{\text{effective}} V_{dd}^2 f_{clk}$$

From the above equation, reducing the switching power consumption can be achieved by minimizing both of the physical capacitance and the switching activity [6].

Physical Capacitance Reduction:

The physical capacitance can be reduced through selecting the appropriate circuit style and optimizing the transistor sizes.

## 2.1. Effects of Circuit Styles

The different circuit and logic styles result in different gate and diffusion capacitance of the transistors in a combinational logic circuit [6]. Some of the circuit styles can substantially reduced the physical capacitance and is good for low-power operation. **Figure 3** represents the power-delay products of an 8-bit adder relationship between that was implemented in 2 μm CMOS technology with different circuit styles and the corresponding propagation delays.

As shown in **Figure 2**, the adder that was implemented by using complementary pass transistor logic (CPL) is about twice as fast as the conventional static CMOS. This is due to that CPL improves the performance of the circuit with a lower input capacitance and reduced voltage swing. Moreover, a CPL logic circuit consumes less power than a static CMOS one, for instance, the power saving for a CPL adder is about 30% compared to a conventional static CMOS adder [7]. This improvement is mainly due to the reduction in capacitance. The performance of a full adder implemented with different circuit styles, such as conventional CMOS, transmission gate CMOS. Power dissipation of the circuit dramatically on the delay circuit styles to reveals this comparison. The compared results indicate that the CPL-TG provides the lowest power delay product, and the LCPL2 has the second lowest power delay product. Both of them are the best suited for low-power high-performance applications such as adders and multipliers.

## 2.2. Transistor Sizing

The capacitive load that originates from transistor capacitance and interconnect wiring can be reduced by optimizing transistor sizes whenever possible and reasonable. In general, increasing the transistor sizes results in a large (dis)charging current and simultaneously increases the parasitic capacitance. On the other hand, reducing the transistor sizes will result in decreasing input capacitance that may be the load capacitance for other gates and lowering the speed of the circuit. Thus, the objective of transistor sizing is to obtain the minimum power dissipation under given performance requirements. In order to explain how to make transistor sizing, let us consider a static inverter driving a load capacitance being composed of an intrinsic (diffusion) and an extrinsic (wiring and fan out) capacitances. When the total load capacitance to the gate output is dominated by the diffusion capacitance, the smallest possible sizes of the transistors should be used for obtaining the lowest power consumption. Otherwise, if the load capacitance is dominated by the extrinsic component [8].

### C) Switching Activity Reduction

The dynamic power consumption of a circuit is strongly related to the switching activity of the circuit [8]. At the circuit level, one main consideration for low-power designs is the choice of the static or dynamic logic styles. The dynamic logic gates are clocked, and undergo the pre-charge and evaluation phases, which are suitable for high-speed applications for the expense of high power dissipation. Whereas the static CMOS is the best choice for low-power high-speed implementation of dedicated circuit applications like multipliers .The switching activity can be reduced by many means such as reordering input signals, no bus-sharing technique, and minimizing the glitching activity of the static circuits etc.

## 2.3. Minimizing Glitching Activity

Glitches, or dynamic hazards, are unwanted signal transitions which occur before the signal settles to its intended value. Glitches can be generated and propagated in both data path and control parts of the circuits. The simulation result from the circuit simulator (Specter) was obtained under the different conditions. The spurious transitions consume extra power compared to the glitch-free scenarios. The number of spurious transitions in a circuit depends on the logic depth, input patterns, and intermediate carry signal states etc.

The glitching activity in static circuit designs can be minimized by selecting structures with balanced signal paths and reduced logic depth. The tree structures can be applied to implement a circuit with both of the balanced signal paths and less logic depth, while the chain structures are quite the contrary. A good example in **Figure 4** illustrates the choice of the tree or chain structures [5]. The second adder computes twice and the third adder computes three times per cycle due to the finite propagation delay through the previous adders. By contrast, the logic depth in the tree case has been reduced from three to two and the signal paths are more balanced. Thus, the switched capacitance (effective capacitance) for the chained case is a factor of 1.5 larger than in the tree [8] [9].

Another possible approach to eliminate the spurious transitions is to use dynamic logic circuits instead of static logic, since any node in dynamic logic circuits can only undergo at most one transition per clock cycle.

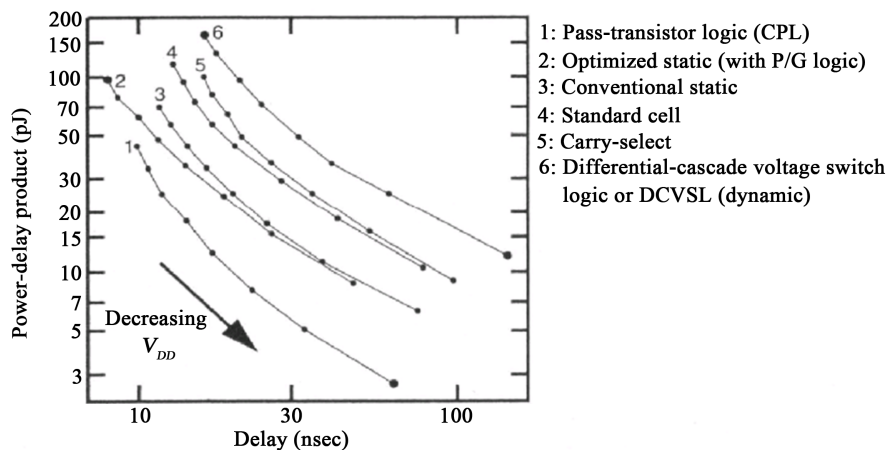### D) Reduction Technique for Leakage Power



1: Pass-transistor logic (CPL)
2: Optimized static (with P/G logic)
3: Conventional static
4: Standard cell
5: Carry-select
6: Differential-cascade voltage switch logic or DCVSL (dynamic)

**Figure 3.** Power-delay products versus delay for an 8-bit adder [4].
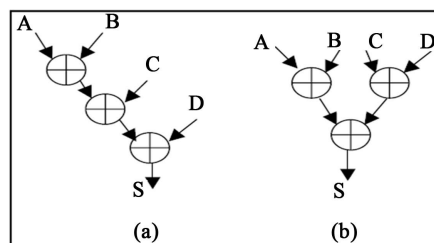


**Figure 4.** Tree versus chain structures [6].

The number of typical reduction for leakage techniques fall in two categories, either leveraging the stack effect or increasing the transistor threshold voltage. Forcing transistors into stacks is not a scalable solution and its implementation becomes very complicated for large designs. There are three main reasons for minimizing leakage current. They are (i) source/drain junction leakage current which is due the junction acts as an diode in reverse bias when the transistor is in sleep mode. *i.e.* in OFF. (ii) Is gate tunneling leakage current which flows through the oxide to substrate? If the gate oxide is thin, then the current increases exponentially. And the third one is (iii) sub threshold leakage current, which is a current from source to drain. It is diffusion current built by minority carriers in the channel in the MOS devices [9].

As technology scales into the deep-submicron (DSM) regime, standby sub threshold leakage power increases exponentially with the reduction of the supply voltage vdd and the threshold voltage vth. For many event driven applications, such as mobile devices where circuits spend most of their time in an idle state with no computation, stand by leakage power is especially detrimental on overall power dissipation [10]. Multi-Threshold CMOS (MTCMOS) is an effective circuit-level methodology that provides high performance in the active mode and saves leakage power during the standby mode. The basic principle of the MTCMOS technique is to use low vth transistors to design the logic gates where the switching speed is essential [11], while the high vth transistors (also called sleep transistors) (**Figure 5**) are used to effectively isolate the logic gates in standby state and limit the leakage dissipation. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

## 3. Leakage Feedback Static Flip Flop

Another use of the leakage feedback gate is to modify the static MTCMOS flip flop to eliminate the need for the parallel inverter to re circulate data. The leakage feedback structure can be used instead, which does not slow down the critical path because no extra capacitances are introduced on internal nodes [12]. The addition of the helper sleep devices only add load to the outputs of I4 and I5 which are not part of the critical path, so the speed of the MTCMOS flip flop is not compromised. When transitioning from the sleep state to the active mode state, one cannot immediately turn on the master latch high Vt sleep transistors because that might accidentally cause the data to flip state.

## 4. Simulation Results (Figure 6 and Figure 7)

Simulations were performed on the various MTCMOS flip flop architectures in a 0.16 u technology with high Vt approximately 0.15 V and low $V_t$ approximately 0.05 V (defined the 10 nA @ 10 um point). **Figure 8** illustrates how the leakage feedback gate of **Figure 9** can hold data during the standby state even when the input varies during the sleep state [12].

## 5. Conclusion

In this paper, several existing power reduction techniques are discussed and a novel circuit design technique to minimize sleep mode power consumption due to leakage power in CMOS technology is discussed. This circuit technique provides significant energy savings in sleep mode without any speed degradation or die area overhead. Moreover, it is almost independent of technology scaling and has no circuit design complexity. This paper presented several dual-threshold voltage circuit techniques that can help reduce sub threshold leakage currents during standby modes for combinational logic blocks [13]. MTCMOS was shown to be an effective standby leakage control technique for static logic, but difficult to implement since sleep transistor sizing is highly dependent on discharge patterns within the circuit block. We have developed a multi-sleep transistor synthesis
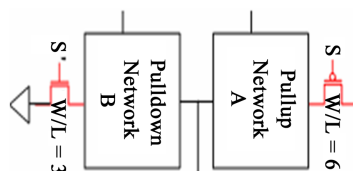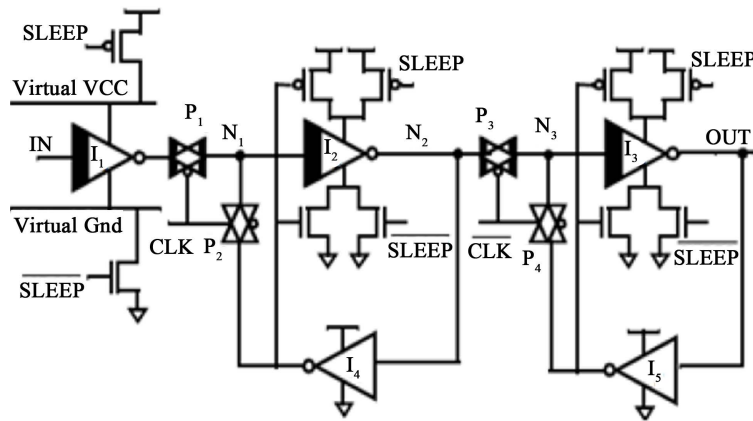


**Figure 5.** Sleepy transistor [8].
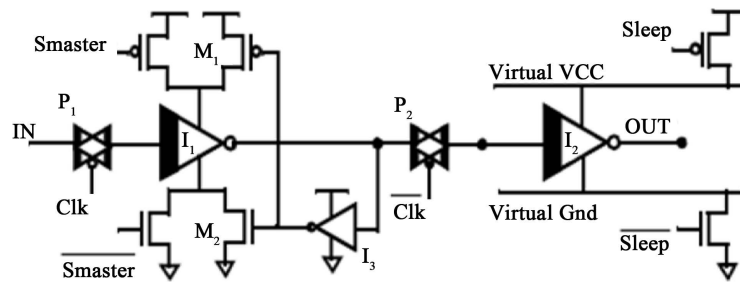
**Figure 6.** Leakage feedback MTCMOS flip-flop [8].



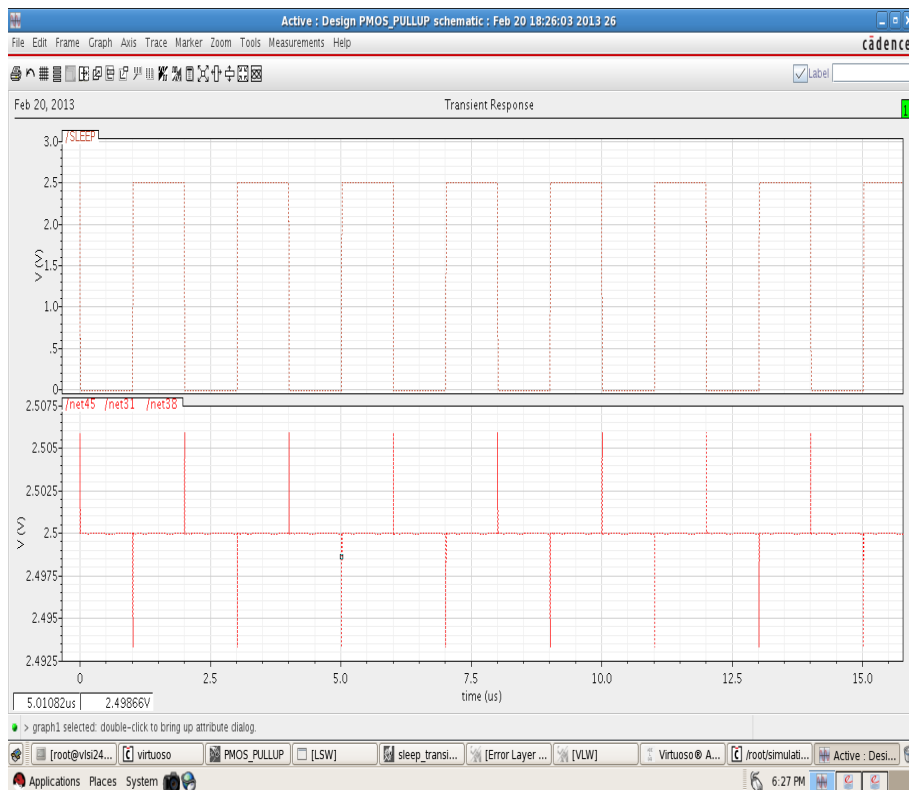**Figure 7.** Dynamic flip-flop leakage feedback [9].



**Figure 8.** Simulation of leakage feedback MTCMOS flip-flop [13].

**Figure 9.** Simulation of leakage feedback dynamic flip-flop [13].

technique which enables to further reduce the total leakage w.r.t. the case of high-sleep transistors [14].

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