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Fast Switching Fractional-N Frequency Synthesizer Architecture Using TDTL

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ABSTRACT

This paper presents an efficient indirect fractional frequency synthesizer architecture based on the time delay digital tanlock loop. The indirect type frequency synthesis systems incorporate a low complexity high performance adaptation mechanism that enables them to remain in a locked state following the division process. The performance of the proposed fractional-N synthesizer under various input conditions is demonstrated. This includes sudden changes in the system input frequency as well as the injection of noise. The results of the extensive set of tests indicate that the fractional-N synthesizer, proposed in this work, performs well and is capable of achieving frequency divisions with fine resolution. The indirect frequency synthesizer also has a wide locking range and fast switching response. This is reflected by the system ability to regain its lock in response to relatively large variations in the input frequency within a few samples. The overall system performance shows high resilience to noise as reflected by the mean square error results.

Keywords: Fractional, Synthesizer, Time Delay Tanlock Loop, Register Adaptation

1. Introduction

Frequency synthesizers, particularly the fractional type, are a fundamental component of the many types of modern wireless communication systems in use now a day. These complex wireless systems, be it for the ever growing mobile communications market or other applications, need to support a multitude of different wireless standards for disparate applications with their own data transfer requirements. However, irrespective of the wireless standard in use, the data to be transferred will somehow need to be modulated on a radio frequency (RF) carrier, and the modulated signal is then transmitted over the air, and received and demodulated at the receiving end. At both the transmitting and the receiving end, an accurate RF carrier signal must be generated. Therefore, a radio frequency synthesizer is always required in order to perform frequency translation and channel selection [1–5].

The design of frequency synthesizers continues to present major challenges due to the stringent RF requirements as well as the demands for high speed in digital transceivers supporting the drive for convergence. Conventional frequency synthesis techniques [1,2] in use today may be broadly classified into the following types:

- Phase-locked loop (PLL) based, or 'indirect'
- Mixer / filter / divide, or 'direct analog'
- Direct digital synthesis (DDS)

Each of these methodologies has its merits and limitations. Direct analog synthesis uses the functional elements of multiplication, division and other mathematical manipulation to produce the desired frequency, but this method is a very expensive one. DDS uses logic and memory elements to digitally construct the desired output signal. On the output side, a digital-to-analog (D/A) converter is used to convert the digital signal to analog domain. The main limitations of DDS are the limited bandwidth and spurious harmonic generation. PLL-based frequency synthesis has been widely used in industry. However, one of the major difficulties associated with the PLL-based technique is that a PLL with a wide frequency range cannot be achieved easily. In addition, fast switching is difficult to achieve. Typically, the output frequency step size of this method is the reference frequency. With fractional-N synthesis technique, finer frequency control can be achieved; however, these systems typically have very narrow bandwidth [7–10].

Today's advanced communication systems demand frequency synthesizers of high resolution, wide bandwidth and fast switching speed. The fractional frequency synthesizer proposed in this paper is designed to achieve the above mentioned requirements. It is of the indirect

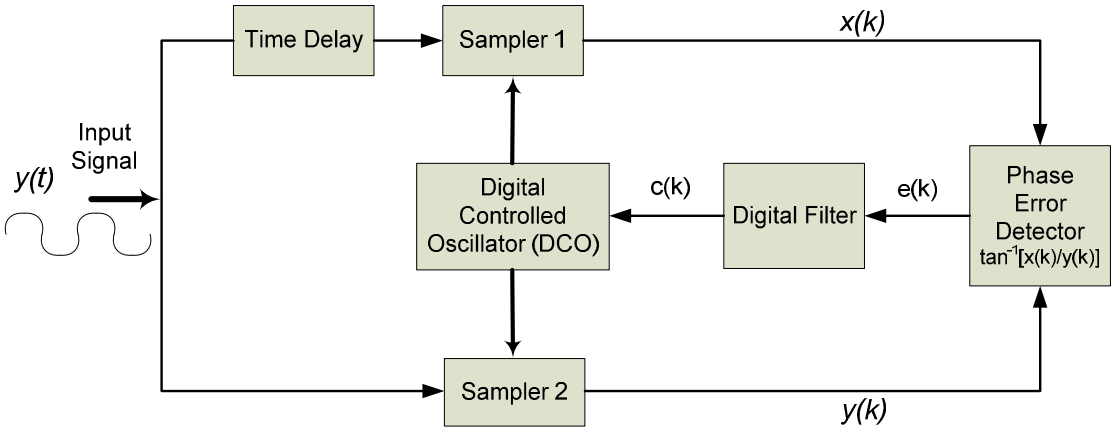


Figure 1. Architecture of time-delay digital tanlock loop.

type that uses time delay digital tanlock loop (TDTL) as the phase locking element, a divider, and an efficient adaptive control structure.

The paper is organized as follows. Section 2 presents the architecture and system equations of the time-delay digital tanlock loop. This also includes the locking range of the TDTL which is a major aspect of a phase lock loop. Section 3 discusses the process and the challenges of using the TDTL as a frequency synthesizer. The adaptation process introduced to enable the TDTL based frequency synthesizer to achieve locking for the fractional frequency division is detailed in Section 4. The results of the new TDTL based fractional frequency synthesizer (TDTL-FFS) for various division factors and under different input conditions are detailed in Section 5. An assessment of the performance of the TDTL-FFS is presented in Section 6. The conclusions of this work are presented in Section 7.

2. TDTL Architecture and System Equations

The architecture of the TDTL is shown in Figure 1. It consists mainly of two samples and hold blocks, a phase detector, a low pass filter, a digitally controlled oscillator, and a time-delay block [11]. Being comprised of these components, the TDTL lends itself for implementation in various digital systems technologies. The TDTL offers an inexpensive implementation and improved performance compared with other synchronization techniques. Compared with the conventional digital tanlock loop in [12], the TDTL in Figure 1 does not preserve the linearity of the phase characteristics due to the existence of input dependant phase shift caused by the time delay. However, this disadvantage is considered relatively minor due to the significant advantages offered by the TDTL, which include wider locking range and fast acquisition behavior. An in depth comparison of the conventional digital tanlock loop and TDTL with extensive results and discussion is given in [13]. The mathematical analysis of the TDTL under noise free conditions is detailed below. All of the signal notations are chosen in reference to the block diagram shown in Figure 1. The analysis follows a similar line to that given in [13,14].

The TDTL receives a continuous time sinusoid *y(t)* which is given by (1).

$$y(t) = A\sin\left[w_o t + q(t)\right] + n(t) \tag{1}$$

where A is the amplitude of the signal, ω_0 is the free running frequency of the DCO, $\theta(t)=(\omega-\omega_0)t+\theta_0$ is the information-bearing phase and $n(t)$ is the additive white Gaussian noise (AWGN). The signal is assumed not to have a DC component. Usually the phase process $\theta(t)$ is a translation of frequency or phase steps. w is the radian frequency of the input signal and θ_0 is a constant. A phase lag $\psi=\omega\tau$ is induced to the input signal after it passes through the time delay block. Therefore, $x(t)$ is generated, which is a phase shifted version of the input signal $y(t)$, this signal is given by (2).

$$x\ (t) = A\sin\left[w_o t + q(t) - \Psi\right] + n'(t) \tag{2}$$

where $n'(t)$ is the time-delayed AWGN due to τ. The aforementioned continuous time signals pass to the sample and hold blocks, and thereby get transformed to the discrete time signals in (3) and (4).

$$y(k) = A\sin\left[w_o t(k) + q(k)\right] + n(k) \tag{3}$$

$$x(k) = A\sin\left[w_o t(k) + q(k) - \Psi\right] + n'(k) \tag{4}$$

where $q(k) = q[t(k)]$.

The sampling interval between the sampling instants $t(k)$ and $t(k\text{-}1)$ is given by (5).

$$\mathrm{T}(k) = T_0 - c(k-1) \tag{5}$$

where $T_0=2\pi/\omega_0$ is the nominal period of the DCO and $c(i)$ is the output of the digital filter at the i^{th} sampling instant. Assuming $t(0)=0$, the total time $t(k)$ elapsed up to the k^{th} sampling instant is given by (6).

$$t(k)=\sum_{i=1}^{k}T(i)=kT_o-\sum_{i=0}^{k-1}c(i) \tag{6}$$

$$y(k)=A\sin\left[q(k)-w_o\sum_{i=0}^{k-1}c(i)\right]+n(k) \tag{7}$$

$$x(k)=A\sin\left[q(k)-w_o\sum_{i=0}^{k-1}c(i)-\Psi\right]+n'(k) \tag{8}$$

and therefore, the phase error between the input signal and the DCO can be also defined as:

$$j(k)=q(k)-w_o\sum_{i=0}^{k-1}c(i)-\Psi \tag{9}$$

Having defined the phase error, Equations (7) and (8) can be rewritten as

$$y(k)=A\sin[f(k)+\Psi]+n'(k) \tag{10}$$

$$x(k)=A\sin[f(k)]+n'(k) \tag{11}$$

These signals are applied to the phase detector producing the error signal *e*(*k*) given in (12).

$$e(k)=f\left[\tan^{-1}\left(\frac{\sin[f(k)]}{\sin[f(k)+\Psi]}\right)\right]+z(k) \tag{12}$$

where $f(g)=-p+[(g+p)\bmod 2p]$, $z(k)$ is a random phase disturbance due to AWGN. The error signal *e*(*k*) represents a nonlinearly mapped version of the phase error. However, the effect of the nonlinearity is minimum and *e(k)* can be approximately linear if ψ is equal to, or in the vicinity of $\pi/2$. The digital filter, which has a transfer function given by *D*(*z*) receives the error signal *e(k)* and produces the signal *c*(*k*) that drives the DCO. Therefore, the system difference equation can be derived from (6) and (9) as

$$f(k+1)=f(k)-wc(k)+\Lambda_o \tag{13}$$

where $\Lambda_0=2p(w-w_0)/w_0$, and the AWGN terms are neglected since noise-free analysis is assumed. In the case of the conventional digital tanlock loop, the linear characteristic function of the phase detector enables the description of the loop as a linear difference equation, and hence finding the lock range using the stability criterions of its Z-transformed transfer function [12]. However, the nonlinear characteristic function of the TDTL phase detector results in a nonlinear difference equation, which can only be solved by numerical analysis. The lock range of the TDTL was analyzed in [11], using fixed-point theorems [15]. The digital filter of the first order loop is simply a gain block G_1, and the system equation is given by

$$f(k+1)=f(k)-K_1'h[f(k)]+\Lambda_o \tag{14}$$

where $K_1'=wG_1$. Defining $K1$ as $\omega_o G_1$ will result in $K_1'=K_1/W$, where $W=w_o/w$. The nominal phase lag Ψ_o induced by the time delay units on the input can be initially arranged by manipulating the parameters ωo and τ in the manner given by $\Psi_o=\omega\tau_o$. Therefore, the locking range can be acquired by numerically solving the inequality

$$2|1-W|<K_1<2W\frac{\sin^2(a)+\sin^2(a+\Psi_o)}{\sin(\Psi_o)} \tag{15}$$

where $a=\tan^{-1}(b)$, $b=\dfrac{\sin(\Psi)\tan(h)}{1-\cos(\Psi)\tan(h)}=\dfrac{\sin(\Psi)}{\cot(h)-\cos(\Psi)}$

and $h=\dfrac{\Lambda_o}{K_1'}$

One of the properties of the first order TDTL is that it converges to a nonzero steady state phase error, which is translated with a phase offset between the pulses of the DCO and the zero crossings of the input signal. The steady-state value of the phase error is given by $f_{ss}=s+jp$ where $j\in\{1,0,-1\}$. Figure 2 shows the locking range of the first-order TDTL for different values of Ψ_o as well as the conventional digital tanlock loop locking region [11]. Note that the region enclosed by (1), (2) and (3) is for the conventional digital tanlock loop; the region enclosed by (1), (2) and (4) is for the TDTL when $\Psi_0=\pi/2$; and the region enclosed by (1) and (5) is for the TDTL when $\Psi_0=\pi$.

The range of independent locking of the TDTL and the effect of initial phase error are studied in depth in [11, 13]. Since the TDTL has non-linear characteristic function numerical analysis were used to determine the range of independent locking. The analysis shows that the TDTL offers an advantage on the conventional digital tanlock loop in this regard.

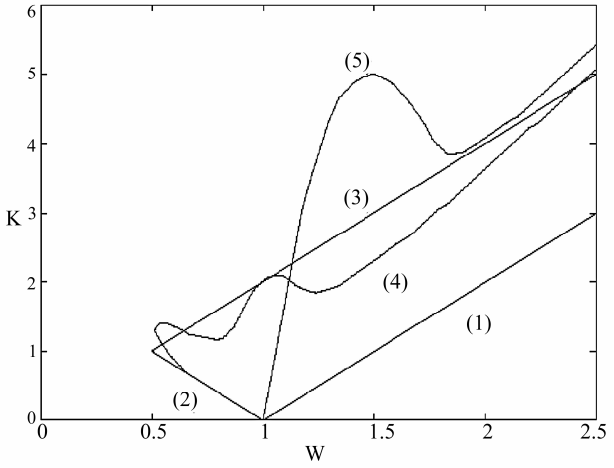


Figure 2. Major locking range of the first-order TDTL for different values of $Y_0=w_0t$.

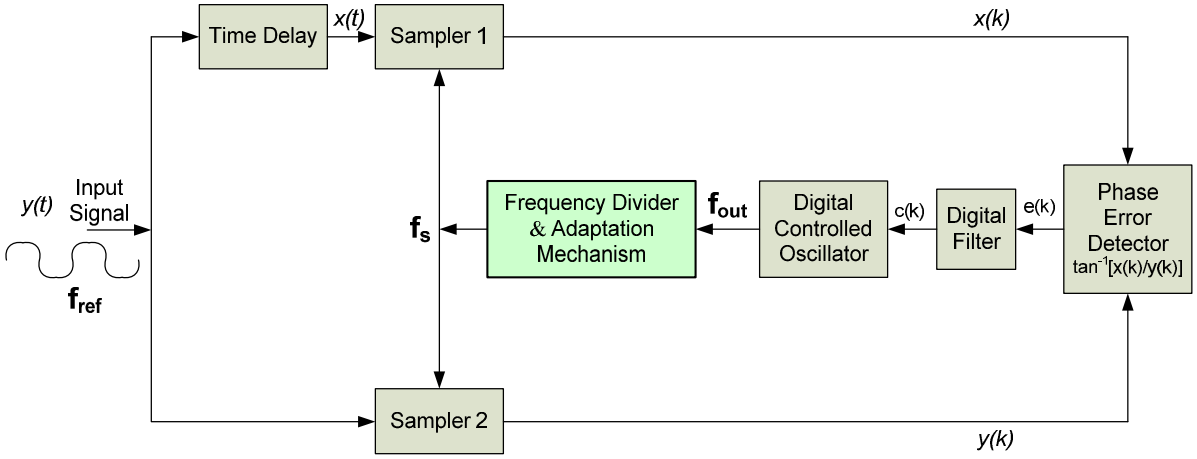


Figure 3. Basic architecture of TDTL-based frequency synthesizer.

3. TDTL-Based Frequency Synthesizer Architecture

In order to utilize the TDTL system, described in the previous section, for indirect frequency synthesis the original system architecture needs to be modified as shown in Figure 3. The additional block in Figure 3 is a composite frequency divider with adaptation control mechanism. This is slightly more involved than a conventional indirect phase lock loop based synthesizer, which would normally only include a divider in its basic form. However, in the TDTL-based frequency synthesizer (TDTL-FS) structure in Figure 3 the adaptation mechanism is essential for the proper operation and stability of the system, as explained below. Once the system operates correctly it results in dividing the DCO output frequency by the desired factor specified by the composite divider block.

The necessity to incorporate an adaptation mechanism is dictated by the direct bearing that a divider block, after the DCO, has on the overall locking state of the TDTL-FS. If the system parameters of the original TDTL in Figure 1, without the divider, are selected such that it operates at optimum point "A" within the first-order loop locking range depicted in Figure 4, then such a system will have a stable behavior, within bounds, as demonstrated by the results in Section 4 as well as in [14]. However, it was observed that the moment a division of the TDTL DCO output frequency is attempted the complete system gets driven out to a point outside the lock range, such as point "B", of Figure 4. Once the system moves to such points outside the lock range, it will be in an unstable state and hence cannot be used. The reason for this is that the divider block affects both the DCO free running frequency and the error signal at the input of the digital filter block. Both of these parameters have direct effect on the system locking.

Therefore, incorporating an adaptation mechanism with the divider in Figure 3 is necessary to overcome the critical locking problem outlined above. It is to be noted that point "A" in Figure 4, at which W=1and K_1=1, is considered an optimum point within the lock range of the first-order TDTL with $\pi/2$ delay, because it allows for maximum symmetrical variation in both the input frequency and the loop gain while maintaining the system locked state. In this study it is always assumed that the loop is operating at this point prior to switching the divider for frequency synthesis.

4. TDTL Fractional-N Frequency Synthesizer

The complete block diagram of the TDTL-FFS is depicted in Figure 5. In addition to the TDTL, the system includes a fractional divider block that uses the pre- scaler technique, and an efficient adaptation mechanism that utilizes registers in order to maintain coherence between the input signal frequency (f_{ref}) and the divider output frequency (fs). As the TDTL-FFS involves multiple divisions, fast system response that counteracts the effect of the division and keeps the complete system in lock is highly desirable.

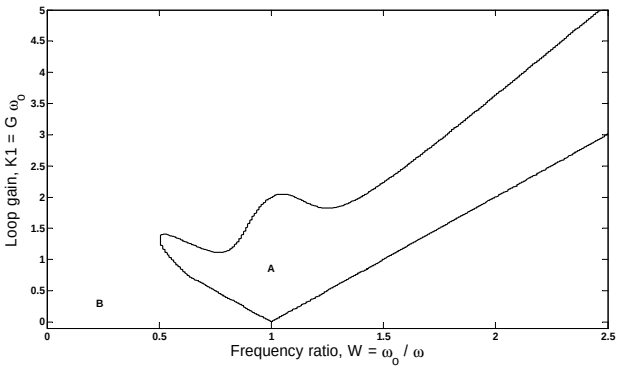


Figure 4. Lock range of 1st order TDTL with $\pi/2$ delay.

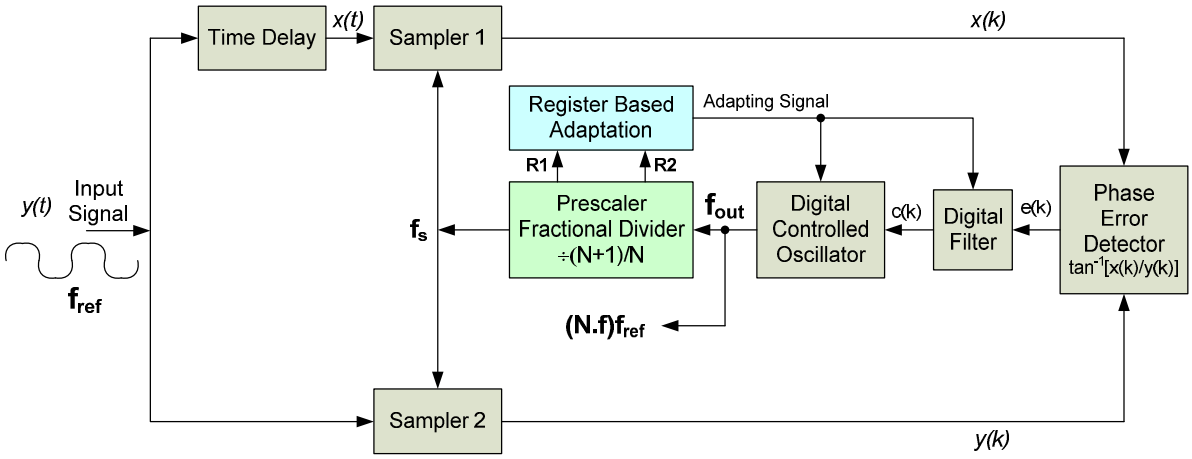


Figure 5. TDTL-FFS with register adaptation.

In the TDTL-FFS in Figure 5, the output frequency (f_{out}) varies by a fraction of the input reference frequency (f_{ref}). This is achieved by realizing an equivalent fractional division ratio, such as N.f, where N and f are the integer and fractional parts of the division respectively. Figure 6 shows the combined structure of the prescaler fractional divider (PFD), that achieves N.f, and the register-based adaptation (RBA). The shaded blocks in Figure 6 make up the RBA while the rest form the PFD module. The PFD divides by N or N+1 according to the control unit. If the PFD divides by N for P output pulses of the DCO and N+1 for Q output pulses, then the equivalent division ratio will be as given in (16).

$$\frac{P+Q}{P/N+Q/(N+1)} \tag{16}$$

The RBA part of Figure 6 uses two registers and a multiplexer. Registers 1 and 2 store the division outputs of dividers N and N+1 respectively. The storage process is controlled by pulses R1 and R2. The outputs of the registers are fed back to the DCO and the digital filter to compensate for the effect of the division and hence keep the overall system in lock.

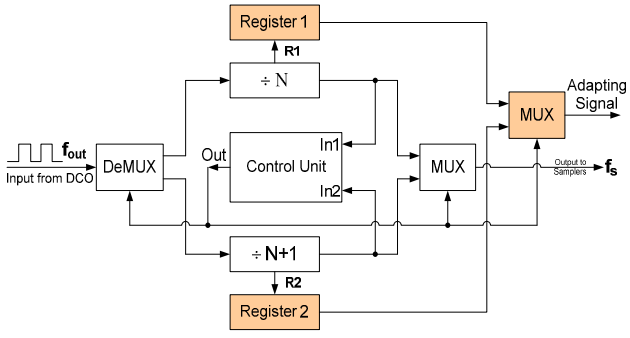


Figure 6. Adaptation mechanism for fractional divider using register approach.

5. Simulation Results of TDTL-FFS

The TDTL-FFS architecture described in the previous section was modelled and simulated using MATLAB/ Simulink. The performance of the complete system was evaluated for two criterions at this stage. The first is the ability of the synthesiser to stay locked or regain locked state should it lose that due to the division process. The second is achieving the correct frequency division ratio with respect to the system input signal frequency. The testing process involved subjecting the system to sudden changes in the input signal frequency by applying positive and negative frequency steps to the input, and changing the division factor. It is assumed that the system is stable prior to the application of step inputs and the division. The subsections below show the results of the first-order TDTL without the presence of a divider, and the TDTL-FFS.

5.1. First-Order TDTL

The first-order TDTL was simulated and its operation verified by applying both positive and negative frequency steps to the input. The steps represent the sudden change in the input signal frequency. The reason behind testing the TDTL by itself is to form a kind of a reference or a signature that can be used for further assessment of the performance of the TDTL synthesizers. This necessity is dictated by the fact that, as discussed in the previous section, utilizing the TDTL as a synthesizer affects the architecture as well as the stability of the loop. A loop that is unstable obviously will not be useful.

The loop was set to operate at optimum point "A" in Figure 4, where $W=\omega_o/\omega_{in}=1$, $K_1=G\omega_o=1$, and $\psi_o=\omega_o\tau = \pi/2$. An input was applied to the TDTL with a positive frequency step of 0.4, this means that the operating point will shift to the point where W=0.71. Although the input shifted the loop to another operating point, the new point

is still within the locking range of the loop. Hence, the loop did not go out of lock and stabilized indicating that the loop has locked onto the new frequency. However, the TDTL response does not converge to zero error in the steady state due to the limitations of the first order loop. The limitation is an inherent feature of the first-order TDTL because the filter block in Figure 1 is only a gain block of G. The response of the system to a positive frequency step is shown in Figure 7. The error signal or the system response is taken from the output of the phase error detector. The result of applying a negative frequency step is shown in Figure 8. In this case W=1.42, but the system manages to stabilize and converge to none-zero steady state error.

5.2. Fractional-N TDTL Frequency Synthesizer

The performance of the fractional-N TDTL frequency synthesizer architecture with register based adaptation mechanism, as described in Section 3, was evaluated through an extensive set of tests. The tests were primarily concerned with assessing the ability of the TDTL-FFS, which includes the composite divider block, to remain in lock following the division of the DCO output frequency and achieve various frequency division ratios.

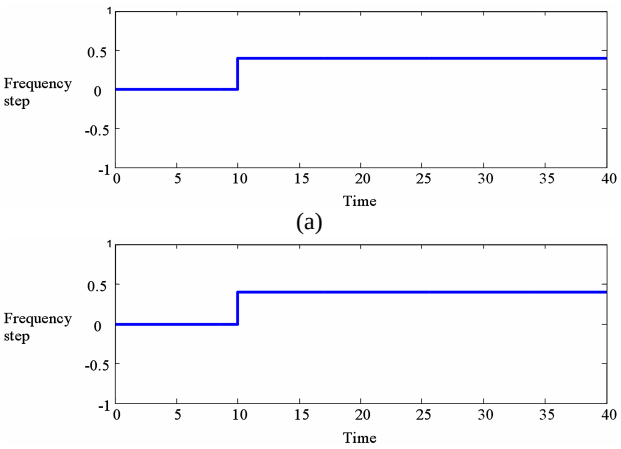


Figure 7. TDTL response to a positive frequency step of 0.4. (a) Frequency step input; (b) Output of the phase error detector.

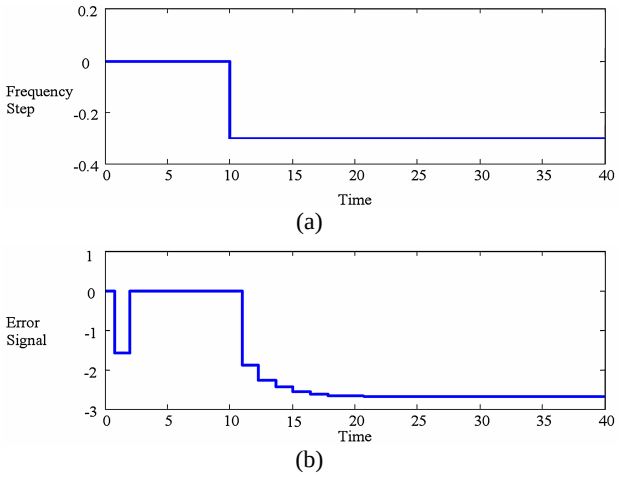


Figure 8. TDTL response to a negative frequency step. (a) Frequency step input; (b) Output of the phase error detector.

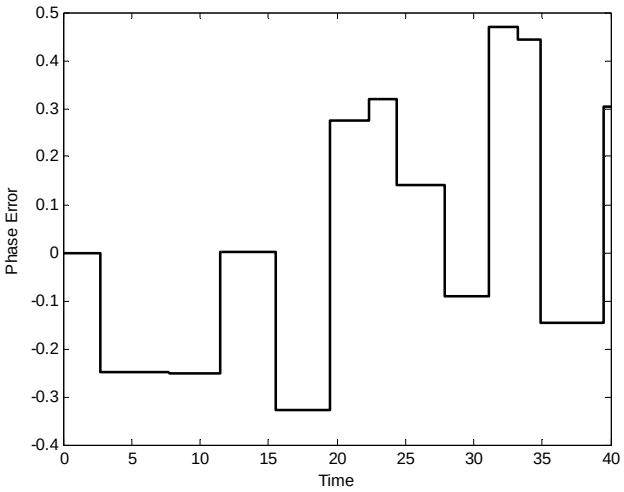
The extensive tests conducted on the TDTL-FFS indicate that it performs very well with respect to the evaluation criterions stated above. This section details some of the results that were achieved. In all the test cases it is assumed that the basic TDTL parameters were selected so that it operates at the optimum point within the locking range of Figure 4 prior to the activation of the composite divider block that converter the system to a TDTL-FFS. It is also assumed that sudden changes in the input signal frequency are not severe so as to drive the system out of lock. These assumptions are applied in order to focus on proving that the new architecture is capable of performing fractional frequency synthesis. TDTL system architectures that deal with wide variations in the input signal frequency through extended locking range are discussed in [13,14].

The importance and effectiveness of the register based adaptation mechanism of the composite divider block of the TDTL-FFS is illustrated in Figure 9. In this case the TDTL-FFS was subjected to the positive frequency step in Figure 7(a) and a pre-scaler divider block with a division ration of 4 and no adaptation was included at the DCO output. Figure 9(a) shows that the system lost its locked state. This is further illustrated by the phase plane plot depicted in Figure 9(b). Replacing the divider block with one that also includes the register adaptation elements enabled the TDTL-FFS system to regain its locked for the same positive step frequency input as shown in Figure 9(c).

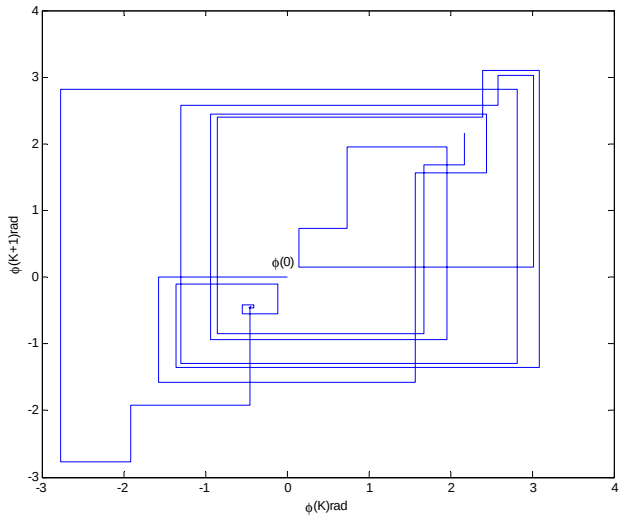
The effect of a division ration of 3.5 and a positive step input, the same one in Figure 7(a), is illustrated in Figure 10. The figure shows the DCO output as well as the divider output which clearly indicates the impact of the division.

The response of the TDTL-FFS to a negative frequency step and a division ratio of 3.8 are illustrated in Figure 11 and Figure 12 respectively. The output of the phase error detector in Figure 11 indicates that the system regain locking following the application of the negative step within a relatively small number of samples. The fractional divider output in Figure 12 indicates a frequency that is 3.8 with respect to that of the DCO output.

In many applications, such as adjacent cells of a wireless network, fine divisions are required. The ability of the TDTL-FFS to achieve such fine fractional division ratios is demonstrated in Figure 13. The division ratio at output of the divider block with respect to the DCO output is 2.0714285. The TDTL-FFS was also tested for other division factors and input frequency steps. The system behaved consistently by achieving the required divisions provided that the assumptions stated earlier are maintained.



(a)



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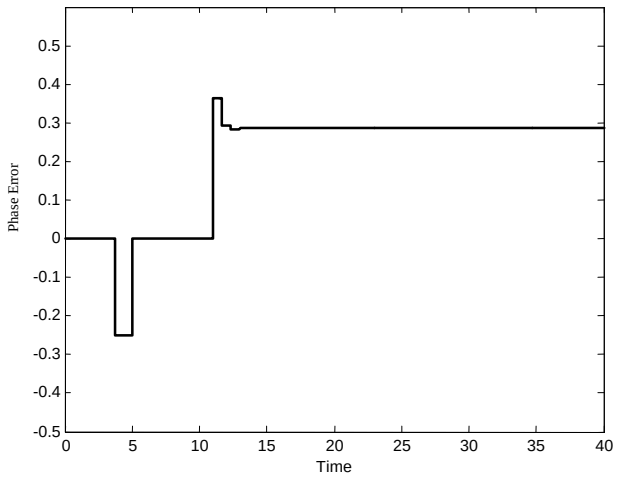
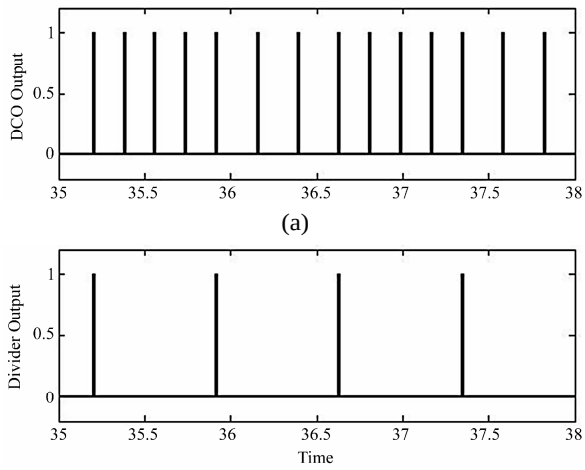


(c)

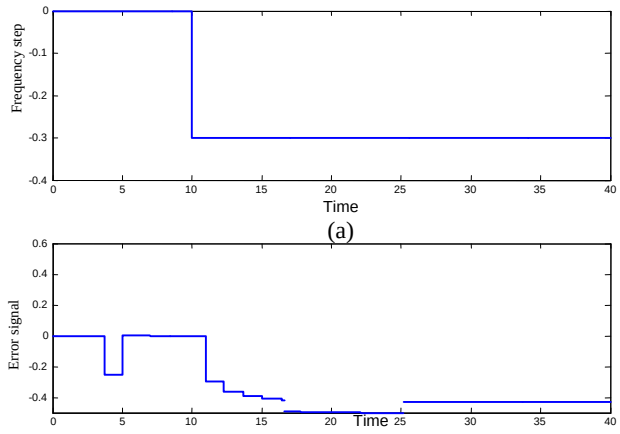
Figure 9. TDTL-FFS response to a positive step. (a) Without adaptation; (b) Phase plane without adaptation; (c) Response with adaptation.



(a)

(b)

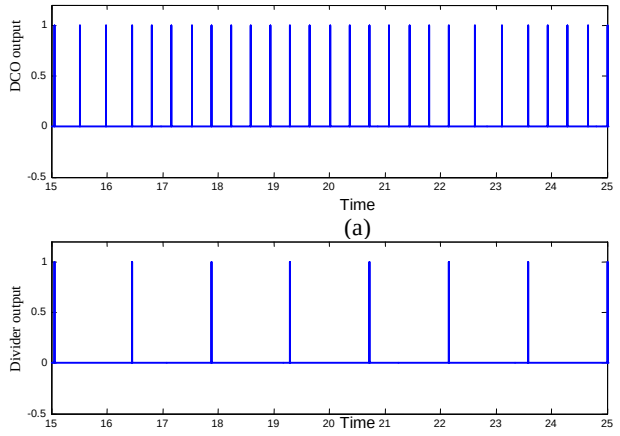
Figure 10. TDTL-FFS outputs for 3.5 division factor. (a) DCO output; (b) Frequency divider output.



(a)

(b)

Figure 11. TDTL-FFS system response to a negative frequency step with RBA. (a) Frequency step input; (b) Phase error detector output.



(a)

(b)

Figure 12. TDTL-FFS outputs for 3.8 division factor. (a) DCO output; (b) Frequency divider output.

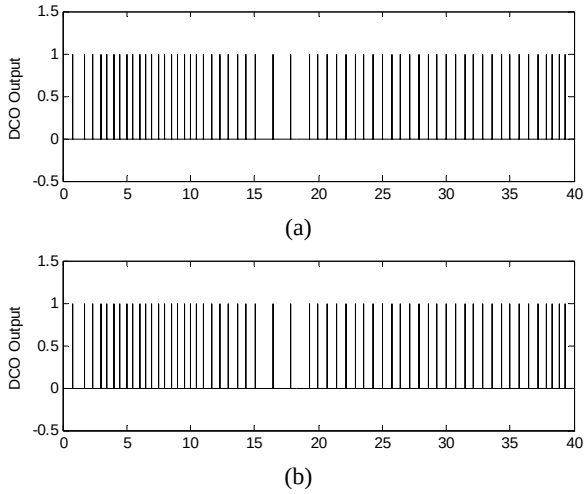


Figure 13. TDTL-FFS outputs for 2.0714285 division factor. (a) DCO output; (b) Frequency divider output.

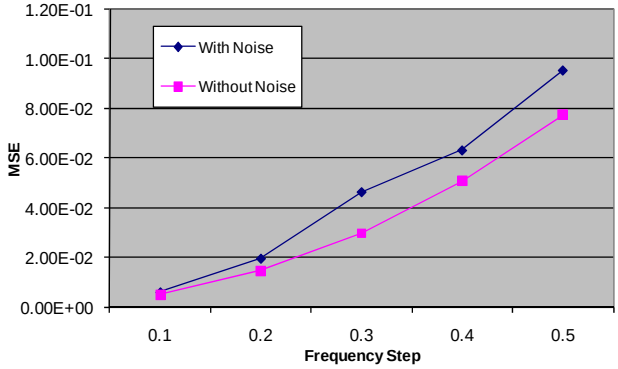


Figure 14. Relationship between frequency step and MSE.

6. TDTL-FFS Speed and Noise Performance

Section 5 above demonstrated the ability of the TDTL-FFS to perform fractional division while maintain the state of locking. Extensive set of test showed that the TDTL-FFS is able to stay in lock when the input frequency varies over a wide range. This is a highly desirable feature of frequency synthesizers as it gives the device the ability to support a variety of wireless communication standards that will invariably operate at different frequencies.

The simulation results of the TDTL-FFS also show clearly that the device support fast switching. The various plots of the synthesizer response, for positive as well as negative input frequency steps, show that the system settles to steady state within a few samples. This was achieved for a variety of division factors including very fine ones. This characteristic of the TDTL-FFS makes it useful in wireless networks with frequency hopping requirements. The performance of the TDTL-FFS under noise conditions was also evaluated. This was done by measuring the mean square error (MSE) for various frequency steps under both noise free and noisy conditions. The plots in Figure 14 illustrate the resilience of the TDTL-FFS to noise. The system kept its locked state and the increase in MSE as a result of the injection of noise is acceptable. A similar study was also conducted to evaluate the effect of noise at different division ratios. The results also indicated that the TDTL-FFS performs very well under noisy conditions.

7. Conclusions

This paper presented a novel fractional frequency synthesizer architecture based on the TDTL. A major challenged faced in utilizing the TDTL for frequency synthesis is keeping the system in locked state following the division process. This problem was overcome by including an adaptation block that compensated for the effects the division had on the loop. The compensation mechanism is an efficient one as it has low complexity and enables fast locking.

The composite adaptor divider block in the TDTL-FFS consisted of a pre-scaler divider and a register based adaptation mechanism. The registers utilize the division information to force the complete system to operate within the locking region by controlling the loop filter gain and the DCO.

The results showed that the TDTL-FFS is capable of performing fractional-N divisions with fine resolution. It can also deal with both positive and negative frequency steps over a wide range of frequencies. The TDTL-FFS has fast switching capabilities and high resilience to noise.

8. References

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