Scientific Research Publishing

Green and Sustainable Chemistry, 2017, 7, 217-233
http://www.scirp.org/journal/gsc
ISSN Online: 2160-696X
ISSN Print: 2160-6951

Silicon and III-V Solar Cells: From Modus Vivendi to Modus Operandi

Alexander Buzynin[1], Yury Buzynin[2], Vladimir Shengurov[3], Vladimir Voronkov[4], Ansgar Menke[5], Albert Luk'yanov[6], Vitaly Panov[1], Nickolay Baidus[3]

[1]Prokhorov General Physics Institute, Russian Academy of Sciences, Moscow, Russia
[2]Institute for Physics of Microstructures, Russian Academy of Sciences, Nizhny Novgorod, Russia
[3]Lobachevski State University, Nizhny Novgorod, Russia
[4]SunEdison, Milano, Italy
[5]Academy of Science and Education Maico-Mannesmann, Hannover, Germany
[6]Lomonosov Moscow State University, Moscow, Russia
Email: abuzynin@yandex.ru

How to cite this paper: Buzynin, A., Buzynin, Yu., Shengurov, V., Voronkov, V., Menke, A., Luk'yanov, A., Panov, V. and Baidus, N. (2017) Silicon and III-V Solar Cells: From Modus Vivendi to Modus Operandi. *Green and Sustainable Chemistry*, **7**, 217-233.
https://doi.org/10.4236/gsc.2017.73017

Received: May 16, 2017
Accepted: August 14, 2017
Published: August 17, 2017

Abstract

In the present paper, some novel opportunities for the development of high-efficient Si and III-V-based solar cells are considered: energy-saving environment friendly low-temperature technology of forming *p-n* junctions in Si (1), elaboration of structurally perfect GaAs/Ge/Si epitaxial substrates (2) and application of protective antireflecting coatings based on cubic zirconia (3). As a result: 1) New technique of forming *p-n* junctions in silicon has been elaborated. The technique provided easy and comparatively cheap process of production of semiconductor devices such as solar cells. The essence of the technique under the study is comprised in formation *p-n* junctions in silicon by a change of conductivity in the bulk of the sample occurring as a result of redistribution of the impurities, which already exists in the sample before its processing by ions. It differs from the techniques of diffusion and ion doping where change of conductivity and formation of *p-n* junction in the sample occur as a result of introduction of atoms of the other dopants from the outside; 2) The conditions for synthesis of GaAs/Ge/Si epitaxial substrates with a thin (200 nm) Ge buffer layer featured with $(1-2)\times 10^5$ cm^{-2} density of the threading dislocation in the GaAs layer. Ge buffer was obtained by chemical vapor deposition with a hot wire and GaAs layer of 1 μm thick was grown by the metal organic chemical vapor deposition. Root mean square surface roughness of GaAs layers of the less than 1 nm and good photoluminescence properties along with their high uniformity were obtained; 3) The conditions ensuring the synthesis of uniform functional (buffer, insulating and protective) fianite layers on Si and GaAs substrates by means of magnetron and electron-beam sputtering have been determined. Fianite films have been

shown to be suitable for the use as an ideal antireflecting material with high protective and anticorrosive properties.

Keywords

Solar Cells, Green Technologies, *p-n* Junctions, Ar Ion-Irradiation, Inversion of Conductivity, Silicon, III-V, GaAs on Si, Ge Buffer, YSZ, Antireflection Coatings

1. Introduction

The development of competitive solar cells (SCs) based on Si and III-V compounds require an improvement of its operational characteristics at simultaneous decrease of the net cost. Currently, average efficiency of SCs based on single crystal silicon approaches to 16%. Novel low-temperature technique of *p-n* junctions formation discussed in the present study allows to reduce the net cost of Si-based SCs and to apply an environment-friendly route of its production. The technique is based on new effect of low-temperature redistribution of admixtures in the semiconductor at irradiation by non-doping low-energy ions.

The highest efficiency (up to 44%) has been achieved in 3-cascade SCs based on InGaP/GaAs/Ge heterostructures matched by the crystal lattice constant at solar radiation intensities of several hundred suns. Because of higher absorption of solar radiation due to direct optical transitions such high efficiencies can be gained at significantly lower thickness of the active region as compared to silicon. In principal, it is enough to have 5 - 6 μm the layer thickness to gain not less than 20% efficiency, whereas in silicon SCs the thickness not lower than 50 - 100 μm is necessary to maintain such efficiency range. This peculiarity opens prospects for the development of light-in-weight film-based SCs. Production of the SCs will require comparatively less initial material, especially, if instead of GaAs or Ge, silicon will be used as a substrate material. At the same time, silicon is an order of magnitude cheaper. In particular, such a replacement will allow actual decreasing the net cost of III-V-based SCs to the level of silicon ones at significant improvement of its operational characteristics. However, in order to ensure high operational parameters of the III-V SCs, it is necessary to obtain high-quality GaAs layers with the threading dislocation density (TDD) on Si substrates not exceeding 10^6 cm^{-2} that, in turn, requires production of perfect buffer layers. Ge buffer layers are considered the most convenient for such application. Usually, at a direct growth of Ge on Si, dislocation density in the epitaxial Ge layer approaches to 10^9 - 10^{10} cm^{-2}.

The use of GeSi gradient buffer layer of 10 μm thickness, in which the gradient increase of Ge ratio is 10% to 1 μm, has been shown to allow TDD decreasing in the Ge layer to 2×10^6 cm^{-2} values. At the same time, the problem of high roughness of the Ge layer still existed. With the purpose to decrease the roughness chemical polishing of Ge_xSi_{1-x} layer at the intermediate stage of the

growth (at x = 0.5) with subsequent up-growing the layer to pure Ge (x = 1) was used. It is worth to note that the mere process of growth of thick GeSi gradient buffer layers is technologically complicated, takes a lot of time and wastes a lot of materials. Therefore, the use of a thin Ge layer (<1 μm) seems to be more promising. However, until recently, it was impossible to solve this problem. In the present study chemical vapor deposition with a hot wire (HW-CVD) technique was successfully applied to obtain a thin perfect Ge buffer layer.

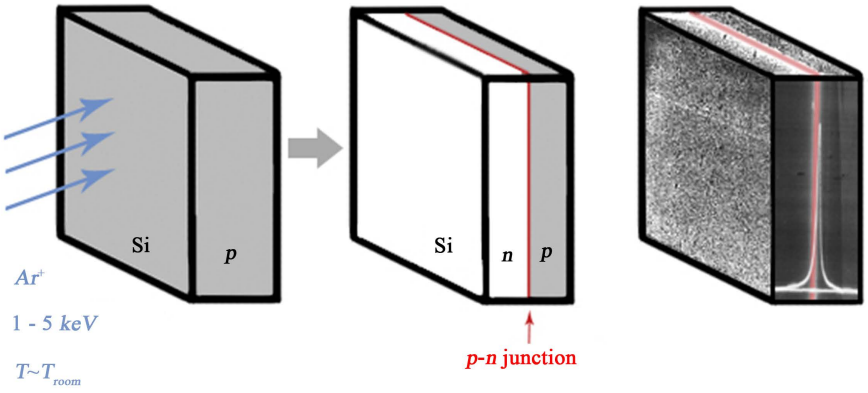
The development of new antireflecting coatings is also an important issue associated with the improvement of the efficiency of SCs. For SCs, in the absence of antireflective coatings, the reflection loss is very significant. For example, for silicon SCs, these can reach 43%, and for SCs based on GaAs—35%. This requires the development of antireflective coatings. In our studies the conditions providing the synthesis of uniform functional (buffer, protective and insulating) fianite layers on Si and GaAs substrates by means of magnetron and electron-beam sputtering have been established. It has been demonstrated that fianite films meet the conditions of an ideal antireflection and feature with high protective and anticorrosive properties. The application of such coating seems to be useful to improve the efficiency and operational life of Si and III-V SCs.

2. Environment-Friendly Low-Temperature Technique of Formation of *p-n* Junctions in Silicon

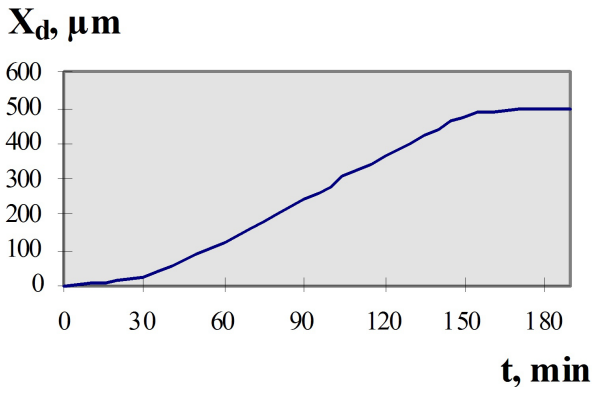
A lot of modern technologies of semiconductor devices are based on formation of *n*- and *p*-regions in a semiconductor crystal and *p-n* junction at their border. For this purpose semiconductors are subjected to doping. Conventional doping techniques (diffusion, ion implantation, and irradiation) have their own common drawbacks: 1) high temperatures, usually more than 1100˚C for the diffusion doping and about 1000˚C for annealing of the radiation defects following ion and irradiation doping; 2) contamination of the crystal by undesirable impurities frequently occurs; 3) almost all dopants are poisonous and pollute the environment [1] [2].

There is also an alternative route of *p-n* junction formation. The route employs a redistribution of donor and acceptor admixtures in a semiconductor (these admixtures always co-exist in real crystals) to form the areas of different conductivity. However, the problem associated with implementation of such an approach is so far under consideration. Herewith, this problem was for the first time solved in our studies [3] [4]. In these studies such redistribution in Si crystal has been observed at irradiation by ions (for example Ar^+) of low energy (1 ÷ 50 keV) at low temperatures (<60˚C) to form an inverted *p-n* junction (**Figure 1(a)** and **Figure 1(b)**), those, which by its characteristics is similar to a conventional diffusion *p-n* junction (**Figure 1(c)**) [3] [4].

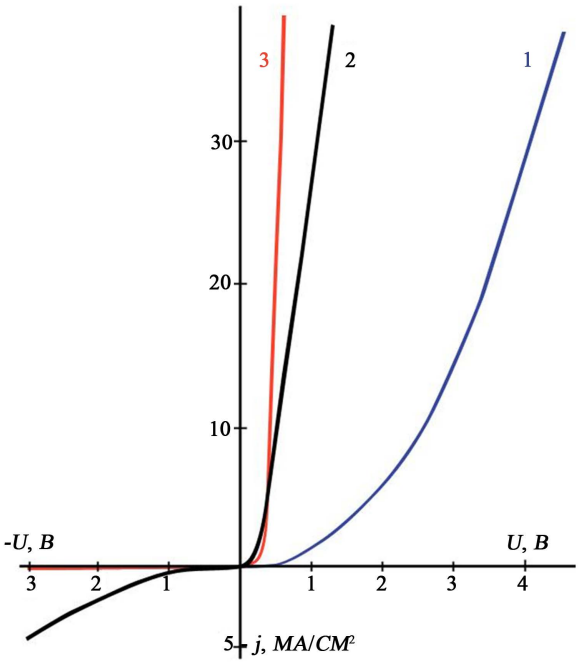
In our studies [5] a model of this phenomenon has been suggested. The observed effect of both formation and propagation of *n*-type regions in the irradiated boron-doped *p*-Si provided an evidence of domination of a powerful self-interstitial flux, which is directed from the very thin defected layer into the



(a)



(b)



(c)

Figure 1. Draft-scheme of the experiment: sketch of SEM image (a, right) comprising a combination of the secondary emission and EBIC), the *p-n* depth (X_d) depending on Ar ions exposition time (b) and BAX characteristics (c) of inverse *p-n* junctions (1, 2) and diffusion one (3) in Si samples with B-Ga contacts (1), Ti contacts (2) and for conventional diode (3).

sample bulk and causes the displacement of boron into an interstitial position. Generation of thermal donors also influences this process. According to the model [5] the formation of *n*-type region in Ar-irradiated samples of *p*-Si is caused by the boron acceptor loss due to self-interstitials produced at the front the surface of Si sample by Ar flux. The mechanism of acceptor loss probably involves reaction of boron atoms with self-interstitials (a kick-out reaction). Model profiles of the Si interstitials (Si_I), boron (B_S) and phosphorus (P_S) substitution atoms at the successive stages of the process of Ar ions irradiation are shown in **Figure 2(a)**. The suggested model and kick-out mechanism of the process [5] were found to be in agreement with the experimental data obtained (**Figure 2(b)**).

Later, the opportunity of formation of *p-n* junctions in Si by means of low-energy irradiation by Ar+ ions at low temperatures has been also investigated and considered in the other studies [6] [7] [8] [9]. Recently such approach to form *p-n* junctions using argon ions treatment has been also demonstrated for GaAs [10].

In [7] an attempt of analysis of the mechanisms of inverse *p-n* junctions has been made. In particularly, the kick-out mechanism was considered as an explanation of the acceptor loss only but cannot account for the occurrence of a donor ("can only explain the loss of an acceptor but cannot demonstrate the occurrence of a donor" [7]). However, such statement seems to be erroneous. This erroneous assertion has been verbatim *et* literatim repeated in a number of further studies, including treatises [8] [9]. As a matter of fact, the loss of acceptors in a local area of a system, those which have donors and acceptors in equal quantity implies the occurrence of additional donors in the system. In fact, for the occurrence of *p-n* junctions (*i.e.*, a boundary between the *p*- and *n*- areas) it is merely enough to decrease the concentration of acceptors in a local area to a value lower than that of donors one. In accordance with the kick-out mechanism this occurs at the relocation of acceptors from the irradiated surface of a sample to its reverse surface. Therefore, there is no necessity for the additional donors occur. The same situation occurs when one wants to withdraw a balance from the equilibrium; he not only decreases the weight of one scale pan but also increases the weight of another.

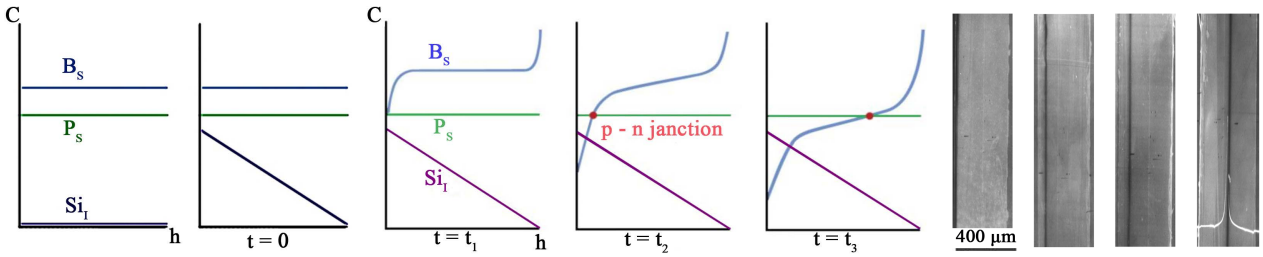


Figure 2. The scheme of self-shifting of the Si interstitials (Si_I) of boron (B_S) and phosphorus (P_S) substitution at successive stages of formation and propagation of the *p-n* junction (a); SEM images (presented as superposition of secondary emission and EBIC modes) of the *p-n* junctions on a chip of Si plate (the plates were irradiated from left side), the dark striae is an image of the *p-n* junction after 20, 45, 60 and 90 minute of the Ar ion irradiation (b).

Basing on this new phenomenon of fast, low-temperature redistribution of impurities in a semiconductor, novel technique of forming *p-n* junctions in silicon has been elaborated. The technique provides easy, cheap, low-temperature, environmental friendly process of production of solar cells and other semiconductor devices , for example X-ray detectors, in which deep *p-n* junctions (>> 1 μm) are used [11] [12]. This makes it possible to replace the widely used practice of maintaining *p-n* junctions by technologies based on elevated temperature, those which involve energy-expansive and toxic processes [2]. Due to physical nature and characteristics of generation of an inverse *p-n* junction, easier and more efficient techniques in the production of semiconductor devices are applicable thus achieving fabrication technology, which involves the formation of two-dimensional (flat) *p-n* junctions over a large area that is necessary for solar cells and similar devices.

3. GaAs/Ge/Si Substrates for III-V Solar Cells

The development of **solar cells (SCs)** based on III-V on Si substrates will provide:

1) A change of expensive germanium and GaAs substrates over convenient Si ones, those which are readily available due to high-scale production;

2) Production III-V/Si SCs of up to 300 mm (and even more) in diameter that will allow to get rid of concentrators;

3) A significant increase of the SCs efficiency as compared to silicon SC at minor increase of the net cost;

4) A considerable decrease of the SCs weight (specific weigh of Si—2.3; Ge—5.5; GaAs—5.9 g/cm^3) that is especially important in aerospace applications.

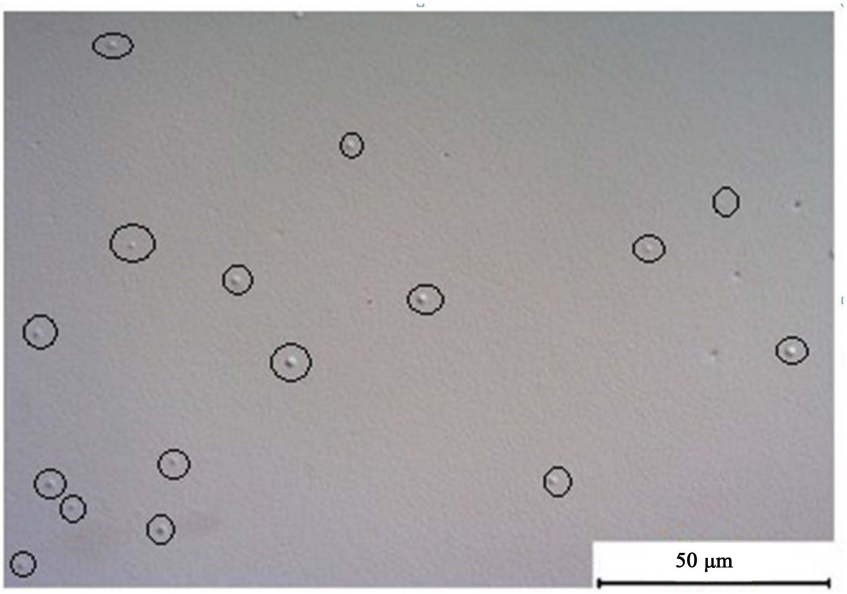
Herewith, in order to ensure the improved characteristics of SCs based on III-V heterostructures on Si substrates, high-quality III-V layers with density of intergrowth dislocations not exceeding 10^6 cm^{-2} are required [13] [14] [15]. Because of a large difference in the lattice parameters (−4%) the TDD in the GaAs layer obtained by a direct growth of GaAs on Si reaches the values of 10^9 - 10^{10} cm^{-2}. To improve the structural quality of GaAs/Si layers the best results formerly were obtained with the use of the thick graded GeSi buffer layers of 10 μm thickness. The TDD in Ge layers grown by this technique is 2×10^6 cm^{-2} [16]. The suggested technique employs ultimately thick gradient buffer. Therefore, due to application of this tool heteroepitaxial process maximally approaches to homoepitaxial one. *i.e.*, it becomes possible to carry out the growth of the same substance with a minor difference of admixture composition by maintaining those conditions of the layer growth, under which a minimum difference of the composition takes place and, consequently, lattice parameters of each sequentially grown layer differ minimally as well.

Herewith, an opposite approach is also known: graphoepitaxy or oriented upgrowing of a layer on amorphous substrate with graphically settled symmetric micro-patterns at complete mismatching between lattice parameters of the epi-

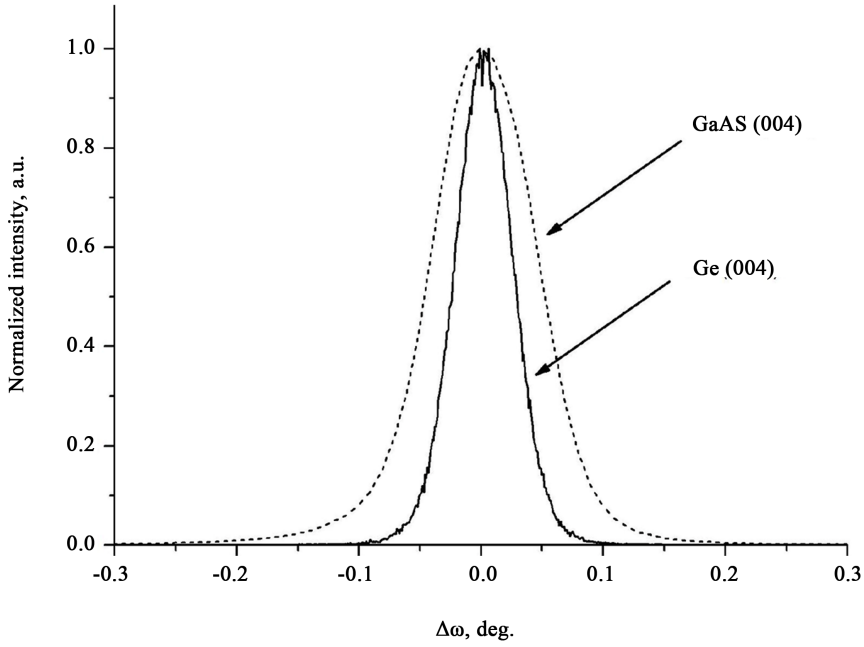
taxy partners. Graphoepitaxy can be considered as a marginal example of this approach. In graphoepitaxy the epitaxially oriented layer is growing at completely structureless (amorphous) substrate with graphically settled symmetric pattern. Graphoepitaxy as a phenomenon, as well as a technique of synthesis of an oriented layer on any substrate has been discovered in Russia by N.N. Sheftal together with one of the authors of the present paper [17] [18]. Six years later, this phenomenon became an object of a considerable interest in the other countries [19] [20] [21] [22]. With the purpose to improve quality of the graphoepitaxial layers a variety of tools were usually used: application of surfactants, growth at high supersaturation (overcooling) of the crystallization media, etc. For example, the use of surfactants in graphoepitaxy of NH_4J from aqueous solution on structureless substrates has shown to be an effective tool to improve quality of the epitaxial film: a simple addition of a diluted soap solution to NH_4J aqueous solution resulted in the change of width to height ratio for the graphoepitaxial islands more than 100 times [17]. Such tools were used also in our studies to solve the problem stated above, *i.e.* to ensure high perfection of the heteroepitaxial Ge layer at its minimal thickness when grown by the HW-CVD on Si substrates.

In the beginning, Ge layers of 200 nm were grown on two-inch epi-ready (100) as well as on Si substrates misoriented from the (100) singular plane to (110) by 5˚ with an epi-ready surface. After degreasing, the substrate was annealed at a high temperature (1200˚C) in the growth chamber for 10 min to remove oxides. The substrate was then cooled to 1000˚C, and Si buffer layer was deposited from the sublimation source. Then, to grow Ge layers, the substrate was cooled to 350˚C, the tantalum strip was heated to 1400˚C, and the growth chamber was filled with germane (GeH_4) to 4×10^{-4} Torr pressure, which was maintained constant during the layer growth using a gas-leaking system. GeH_4 was decomposed on the "hot wire" and Ge layer was deposited on Si substrate. Apparently, atomic hydrogen played a role of the surfactant. Such conditions ensured sufficiently high growth rate of the Ge layer (0.5 - 0.7 μm/hour) and also contributed to the high crystalline perfection and surface smoothness of the layer. The surface of the Ge-on-Si (100) layers showed a stepped morphology that provides an evidence of a laminar mechanism of the growth. The root-mean-square surface roughness (RMS) surface roughness was found to be <0.5 nm that is competitive to the best one achieved so far. Surface of Ge-on-Si (100) layers showed a stepped morphology that provides an evidence of a laminar mechanism of the growth. The root-mean-square surface roughness (RMS) was found to be <0.5 nm that is competitive to the best one achieved so far. The density of etch pits, which was identified with the density of TDD (**Figure 3(a)**) was found to be $1 \cdot 10^5$ cm^{-2} being two orders of magnitude lower than that in Ge layers grown in the other studies [23] [24].

During the second stage, the grown 2-inch Ge/Si structures were placed into the chamber of AIX 200RF Aixtron system. Prior to epitaxial growth of GaAs layer, the Ge/Si substrate was subjected to annealing in hydrogen at T = 750˚C for 10 minutes in order to remove the oxide from Ge surface. Then, mirror-



(a)



(b)

Figure 3. The etching pits of TDD at Ge layer on Si (a) and XRD 2θ/ω scan of GaAs/Ge/Si epitaxial substrate (b).

smooth undoped GaAs single-crystal layer was grown by metal organic chemical vapor deposition (MOCVD) technique in stream of hydrogen, purified with palladium filter at T = 650˚C and under lower pressure (76 Torr) using $Ga(CH_3)_3$ and AsH_3 as precursors.

With the purpose to study GaAs/Ge/Si heterostructures optical, atomic-force (AFM), scanning (SEM) and transmitting (TEM) microscopy techniques, as well as secondary-ion mass spectroscopy (SIMS), XRD and photoluminescence (PL)

were used. The FWHM value of the rocking curve for the (004) X-ray reflections of Ge layers was found to be 190" (**Figure 3(b)**). The Ge layers have a structure of epitaxial mosaic single crystals with almost complete relaxation of the elastic stresses.

TEM images of GaAs/Ge/Si (100) cross-sections have shown somewhat discrepancies to <110> in edge-dislocation network of Ge buffer layer predominantly situated in (100) growth plane and dislocation half-loops were concentrated in vicinity of the interface between Ge layer and Si(100) substrate, whereas a bulk of the Ge layer was actually dislocation-free. Propagation of the dislocations into the bulk of the Ge layer, generations of new dislocations on Ge-GaAs heteroboundary, as well as in the Ge layer have not been observed. Thus, it is possible to conclude that dislocation density in the GaAs layer is of about the same value as in the Ge layer. The TDD decreased by the increase of Ge layer thickness, in particular, due to its "healing", bending with forming dislocation half-loops, annihilation of the opposite sign dislocations at rendezvous contact, etc. (**Figure 4(a)**).

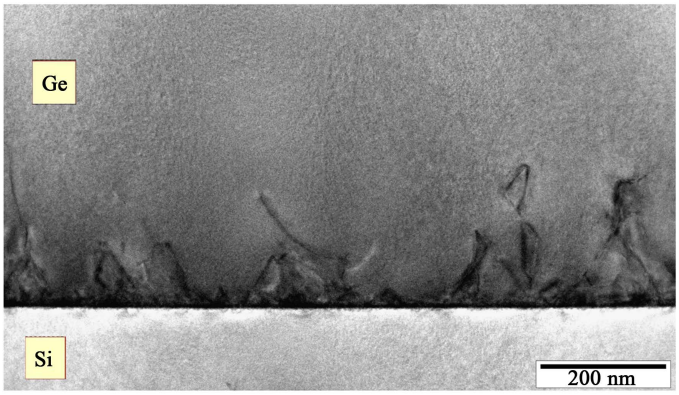
Multiplication of dislocations at further growth of the Ge layer and generation of new dislocations on Ge-GaAs heteroboundary and in GaAs layer were not observed (**Figure 4(b)** and **Figure 4(c)**). That is an evidence for TDD value in GaAs layer is of about of the same quantity as in Ge layer, *i.e.*, about $(1 - 2) \times 10^5$ cm^{-2}. This is significantly lower than the values for GaAs layers obtained by other methods using GeSi [24], InAlAs [25] and InGaAs [26] buffer layers on Si substrates.

The RMS value of surface roughness GaAs layers was less than 1 nm (**Figure 5(b)**) that is also competitive to the best achievements worldwide, in particular to GaAs layers on Si (100) substrate with Ge buffer layer described in [24].

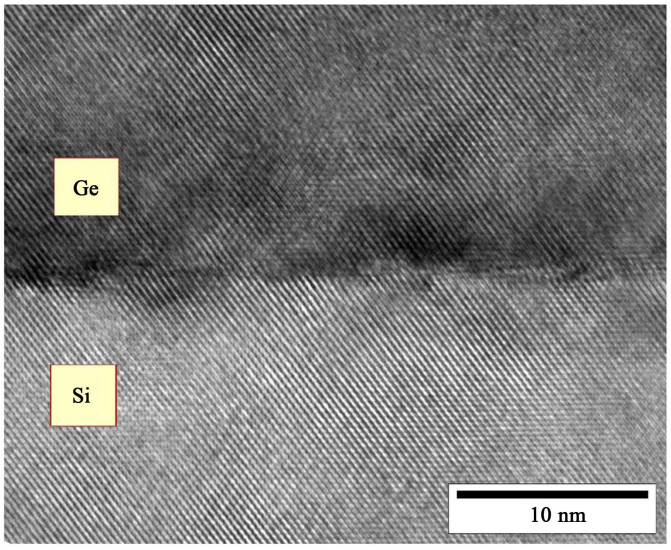
Interdiffusion of Ge and As on Ge-GaAs heteroboundary seems to be an important problem hindering the device application of GaAs/Ge/Si heterostructures. This phenomenon leads to formation of uncontrollable *p-n* junctions disturbing operation of various electronic devices. Thin AlAs layers situated in the area of GaAs/Ge heteroboundary can be used as a diffusion barrier for the interdiffusion. In present study the effect of such AlAs layers of 10 - 500 nm thickness on Ge and as interdiffusion has been studied. Photoluminescence properties of the upper GaAs layer of GaAs/AlAs/Ge/Si (100) substrate were also investigated. Layer-by-layer SIMS analysis of the substrates has shown that the AlAs layer prevented Ge diffusion to GaAs layer that was in agreement with the other studies. Photoluminescence spectra of GaAs/Ge/Si (1) substrates with single (2) and double AlAs (3) insertions are shown in **Figure 5(c)**.

The spectra illustrate that insertion of thin AlAs interlayers into GaAs led to the increase of photoluminescence intensity of the upper GaAs layer that is an evidence of improvement of its structural perfection. PL maps for the epitaxial GaAs/Ge/Si substrates (**Figure 5(d)**) provide an evidence for high uniformity of developed GaAs/Ge/Si epitaxial substrate.

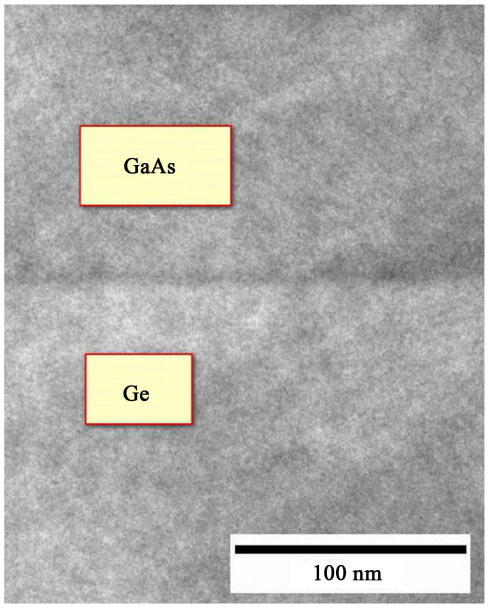
Therefore, the developed GaAs/Ge/Si epitaxial substrates with a thin (200 nm)



(a)



(b)



(c)

Figure 4. TEM images of the cross-sections of GaAs/Ge/Si (100) heterostructure in the area of Ge-Si ((a), (b)) and GaAs-Ge (c) heteroboundaries.

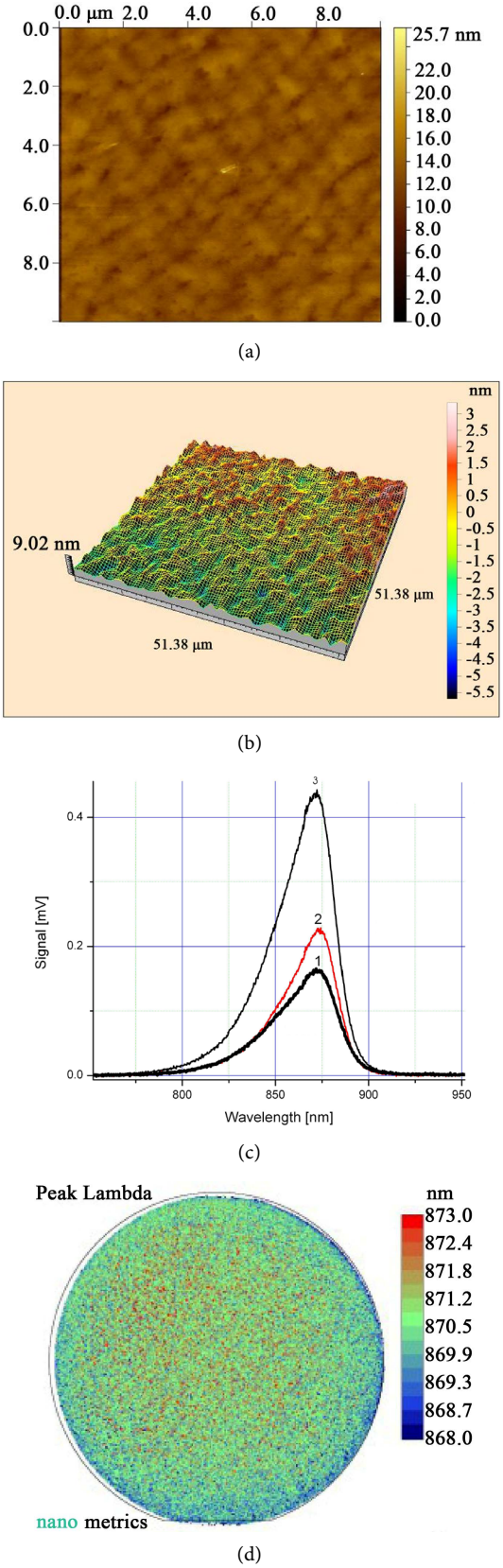


Figure 5. AFM images of Ge/Si and GaAs/Ge/Si layers (Talysurf) and photoluminescence spectra (T = 300˚K) of GaAs/AlAs/Ge/Si (100) heterostructure and 2D map of PL peak wavelength of GaAs/Ge/Si epitaxial substrate.

Ge buffer layer featured with $(1 - 2) \times 10^5$ cm^{-2} TDD in GaAs layer. Such low RMS value of the surface roughness (less than 1 nm), high uniformity and good photoluminescence properties allow to expect its successful application in the field of construction of high-effective III-V/Si SCs.

4. Antireflective and Protective Coatings Based on YSZ and ZrO_2 for Si and III-V Solar Cells

Fianite, or yttria-stabilized zirconia (YSZ) is an extremely promising multifunctional material for new electronic technologies due to its unique combination of physical and chemical properties. It can be used in practically all the main technological stages of the production of devices for optoelectronics: as a monolithic dielectric substrate and a buffer layer for Si and III-V epitaxy, as a material for isolating, antireflection and protective layers, and as the gate dielectric [27] [28] [29] [30]. High transparency of fianite over a wide spectral range (260 - 7500 nm) allows its use in optoelectronic devices, which operate in a wide spectral range: from UV to middle IR, including visual one. The high efficiency of using fianite films as electrolytic membranes of solid oxide fuel cells has also been demonstrated [31] [32]. In the present study, the opportunities of using of fianite and ZrO_2 as antireflection and protective coatings of Si and III-V solar cells are considered.

With the purpose to deposit the coatings magnetron and electron-beam techniques were used. Fianite crystals of $(ZrO_2)_{100-x}$ $(Y_2O_3)_x$ with 15 mole percent Y_2O_3 content were used as the sputtering targets. Besides, the targets made of pure zirconium dioxide ZrO_2 (without Y_2O_3 stabilizing oxide)—the material similar to fianite as to its dielectric properties, was also used. Conventional wafers were used to determine optimal conditions of depositions of fianite and ZrO_2 films on Si, Ge and GaAs substrates. The deposition was carried out followed by a routine chemical treatment. Properties of the films were investigated using ellipsometry, scanning electron microscopy and X-ray diffractometry.

Scanning electron microscopy studies were used for determination of the films porosity. On the samples of 5 - 6 cm^2 square the pores with diameter exceeding 1 μm were absent. For comparison, it is noticeable that in low temperature pyrolytic SiO_2 oxides an average porosity has been found to be in the range of 4 - 8 cm^{-2}. Therefore, considering the porosity of ZrO_2 and fianite films obtained, these films are, at least, in one and a half order of magnitude better than those of SiO_2 on Ge substrates.

Density, surface roughness, as well as thickness of the films were also measured using X-ray studies. In our experiments the incident and reflected beams of the monochrome X-ray radiation beams form small angles adjacent to the surface of a sample. In this case a just-mirror reflection occurs and penetration depth sharply decreases. Under these conditions, the scattering becomes considerably more sensitive to inhomogeneities of various types in the near-surface regions of the crystal. The effect of mirror reflection is observed at those values of glancing angles, which are comparable with critical angle of the total external reflection

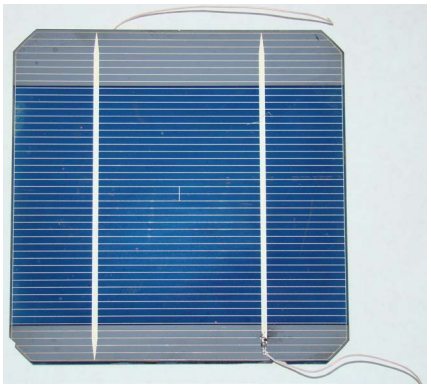
by an order of magnitude. If a crystal deposited on the surface of a substrate constitutes a thin film differing from the substrate by its electron density, then, pronounced oscillations of the thickness in the curve of total external reflection are observed. So, thickness, density and roughness of the film were readily determined by processing of the oscillating curves of the corresponding reflexes. ZrO_2 films obtained in the studies were amorphous but demonstrated sufficiently high density: the measured density values ρ_d = 5.56 g/cm^3 are close to those, obtained within the volume of one of a bulk crystal ρ_v = 5.83 g/cm^3. Roughness of the outer surface of the films, as well as of the semiconductor-film interface did not exceed 5 nm (that corresponds to only 3% of the total film thickness). The thickness values obtained by ellipsometry and the other X-ray techniques were found to be in conformity with each other within the accuracy of the measurements.

According to the modern conception, it is possible to reduce the reflection to zero if the refractive index of the antireflection film (n_d) corresponds to the expression: $n_d = \sqrt{n_s}$, where n_s is an optical refraction coefficient of a semiconductor. This coefficient is equal to 3.7 for Si and 3.5 for GaAs, hence, reflection is completely removed at $n_d = \sqrt{n_s}$ ~ 1.9. The refraction factor of SiO_2 (n = 1.47) is considerably less than the optimal value. With such n value the reflective loss cannot be reduced lower 10%. In practice, fianite and ZrO_2 meets this requirement. The ellipsometry studies allowed measuring thickness of the films, which for various samples were found to be in 60 - 1000 nm range. Coefficients of optical refraction n_d were measured simultaneously. The n_d values obtained were 1.85 and 2.1 for ZrO_2 and fianite film, respectively. These values are in conformity with experimental data obtained in the other studies [33]: for ZrO_2 the difference was only ~13%, as for fianite the values are practically similar. Therefore, application of such materials as antireflecting coatings of in Si and III-V-based SCs seems to be rather good idea. Rather prospects of zirconia-based antireflecting coatings for Si and III-V solar cells have been also confirmed in [34].

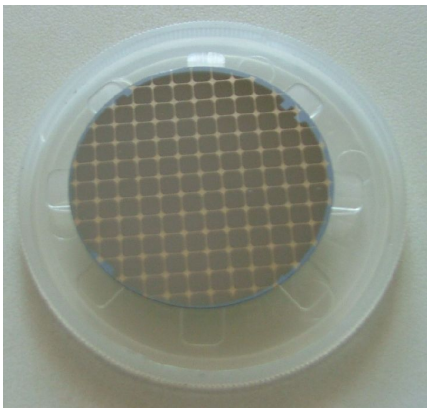
The results obtained also allow a comparison of the properties of fianite and ZrO_2 films. Optical and dielectric properties of these films are similar. Herewith, fianite is superior ZrO_2 by mechanical toughness and corrosive stability. In contrast to ZrO_2, fianite does not lend itself to etching even in strong acids and a sharp needle leaves no scratches on this material. Therefore, fianite provides better protection of a device.

The developed protective antireflecting YSZ coatings were deposited on industrial samples of Si solar cells (**Figure 6(a)**), as well as the solar cells based on III-V/Ge/Si (**Figure 6(b)**). These coatings featured with a mirror-smooth surface and high homogeneity in area with good adhesion. In addition, they had high hardness and toughness with excellent resistance to abrasion. This allows them to be used as protective coatings for touch screens, for example of smartphone (**Figure 6(c)**).

Thus, YSZ films have been shown to be suitable for the use as an ideal antireflecting material with high protective and anticorrosive properties.



(a)



(b)

(c)

Figure 6. YSZ coatings on the pilot industrial samples of Si SCs of 4-inch size (a) and of III- V/Ge/Si SCs with 2-inch diameter (b) and on the touch screen of smartphone (c).

5. Conclusions

At the moment solar cells have two significant drawbacks-high price and low efficiency. In this paper, we have considered some new ways to solve these problems for Si and III-V/Si solar cells:

1) New simple, energy-saving low-temperate, comparatively cheap and ecologically-friendly process of forming *p-n* junctions was elaborated for production of Si-based SCs. The process is based on the new effect of rapid redistribution of impurities in Si by irradiation of the sample by low energy (1 ÷ 50 keV) ions (for example Ar+) at low temperatures (<60˚C).

2) New GaAs/Ge/Si epitaxial substrates with thin Ge buffer layer featuring with $(1-2)\times 10^5$ cm^{-2} TDD in GaAs layer. Thin Ge buffer layer (200 nm) was obtained by HW-CVD and GaAs layer of 1 μm thick was grown by MOCVD. High crystal perfection, low surface roughness (less than 1 nm) and good photoluminescence properties along with high uniformity of the layer were demonstrated. The use of such substrates will actually reduce the cost of III-V/Si- based SCs to the level of silicon ones at significant improvement of its operational characteristics.

3) The conditions for growth of thin mirror-flat, homogeneous YSZ films on Si and GaAs substrates by means of magnetron and electron-beam techniques have been determined. The functional YSZ films were characterized by high antireflecting, stabilizing, protecting and insulating properties, high mechanical toughness, excellent abrasion, corrosion and radiation resistivity. This indicates the effectiveness of the use of YSZ coatings for SCs and other optoelectronic devices based on Si and GaAs compounds.

Acknowledgements

This work has been partially supported by Russian Foundation for Basic Research (grant No. 15-02-99664). Experimental investigations were performed using equipment of the Center of Collective Use at the Institute for Physics of Microstructures.

References

[1] Stone, B.D. (1981) Neutron Transmutation Doping of Silicon. In: Wang, F.F.Y., Ed., *Impurity Doping Processes in Silicon*, North-Holland Publishing Company, Amsterdam, 217-259.

[2] Kramer, H.G. (1981) The Selection of Starting Material for Neutron-Transmutation Doped Silicon. In: Caldberg, J., Ed., *Neutron-Transmutation-Doped Silicon*, Plenum Publishing Corporation, New York, 207-210.

[3] Luk'yanov, A.E., Buzynin, A.N., Butylkin, A.I. and Butylkina, N.A. (1992) SEM Investigation of *p-n* Junction in Homogeneous *p*-Si. *Scanning*, **14**, 358-359. https://doi.org/10.1002/sca.4950140608

[4] Buzynin, A.N., Luk'yanov, A.E., Osiko, V.V. and Voronkov, V.V. (1995) Inversion of Conductivity in *p*-Si after Ion Treatment. *Materials Research Society Symposium Proceedings,Pittsburg, PA*, **378**, 653-658.

[5] Buzynin, A.N., Luk'yanov, A.E., Osiko, V.V. and Voronkov, V.V. (2002) Non-

Equilibrium Impurity Redistribution in Si. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, **186**, 366-370. https://doi.org/10.1016/S0168-583X(01)00882-5

[6] Pichler, P. (2004) Intrinsic Point Defects, Impurities, and Their Diffusion in Silicon. Computational Microelectronics. Springer-Verlag, Wien, 77-227. https://doi.org/10.1007/978-3-7091-0597-9

[7] Popov, V.M., Shustov, Yu.M., Klimenko, A.S. and Pokanevich., A.P. (2009) Influence of Irradiation of Silicon by Low-Energy Ar Ions on the Formation of Electrically-Active Defects in It. *Technology and Design in Electronic Equipment*, **4**, 48-51. (In Russian)

[8] Zhou, H.P., Xu, L.X., Xu, S., Huang, S.Y., Wei, D.Y., Xiao, S.Q., Yan, W.S. and Xu, M. (2010) On Conductivity Type Conversion of p-Type Silicon Exposed to a Low-Frequency Inductively Coupled Plasma of Ar + H_2. *Journal of Physics D: Applied Physics*, **43**, Article No: 505402. https://doi.org/10.1088/0022-3727/43/50/505402

[9] Xiao, S.Q., Xu, S. and Ostricov, K. (2014) Low-Temperature Plasma Processing for Si Photovoltaics. *Materials Science and Engineering: R: Reports*, **78**, 1-29. https://doi.org/10.1016/j.mser.2014.01.002

[10] Mikoushkin, V.M., Bryzgalov, V.V., Nikonov, S.Yu., Solonitsyna, A.P. and Marchenko, D.E. (2016) Formation of a p-n Junction on the GaAs-Surface by an Ar+ Ion Beam. *Materials Science*. https://arxiv.org/ftp/arxiv/papers/1612/1612.06798.pdf

[11] Buzynin, A.N., Osiko, V.V., Luk'yanov, A.E. and Butylkina, N.A. (2014) New Ecologic Technique of *P*-N Junctions Fabrication in Si for Solar Cells. *Science Postprint*, **1**, Article No: e00025. http://www.spp-j.com/spp/1-1/spp.2014.06A0002

[12] Buzynin, A.N., Osiko, V.V., Luk'yanov, A.E. and Butylkina, N.A. (2006) Method for Forming P-N Junction in Si Using Ion Beam for Simplifying the Process and Reducing Fabrication Costs. Korea Patent No. 1020050072554. http://www.directorypatent.com/KR/1020050072554.html

[13] Samavedam, S.B., Currie, M.T., Langdo, T.A. and Fitzgerald, E.A. (1998) High-Quality Germanium Photodiodes Integrated on Silicon Substrates Using Optimized Relaxed Graded Buffers. *Applied Physics Letters*, **73**, 2125. https://doi.org/10.1063/1.122399

[14] Bolkhovityanov, Yu.B. and Pchelyakov, O.P. (2009) III-V Compounds-on-Si: Heterostructure Fabrication, Application and Prospects. *The Open Nanoscience Journal*, **3**, 20. https://doi.org/10.2174/1874140100903010020

[15] Jain, N. and Hudait, M.K. (2013) Impact of Threading Dislocations on the Design of GaAs and InGaP/GaAs Solar Cells on Si Using Finite Element Analysis. *IEEE Journal of Photonoltaics*, **3**, 528. https://doi.org/10.1109/JPHOTOV.2012.2213073

[16] Jain, N. and Hudait, M.K. (2014) III-V Multijunction Solar Cell Integration with Silicon: Present Status, Challenges and Future. *Energy Harvesting and Systems*, **1**, 121-145. https://doi.org/10.1515/ehs-2014-0012

[17] Sheftal, N.N. and Buzynin, A.N. (1972) Predominant Orientation of Crystals on a Substrate and the Effect of Scratches. *Vestnik Moskovskogo Universiteta*, **4**, 102-104.

[18] Sheftal, N.N., Klykov, V.I. Kokorish, N.P., Buzynin A.N. and Smorodina, T.A. (1974) The Method of Epitaxial Growth of Single-Crystal Layers on a Non-Orienting Substrate. USSR Patent No. 538639.

[19] Smith, H.I. and Flanders, D.C. (1978) Oriented Crystallization on Amorphous Substrates Using Artificial Surface-Relief Gratings. *Applied Physics Letters*, **32**, 349-351. https://doi.org/10.1063/1.90054

[20] Mori, H. (1981) 2-D Grating Graphoepitaxy of Silicon Films from Silicon-Gold Supersaturated Solution. *Japanese Journal of Applied Physics*, **20**, L905-L908.

[21] Givargizov, E.I. (1994) Artificial Epitaxy (Graphoepitaxy). In: Hurle, D.T.J., Ed., *Handbook of Crystal Growth*, *Volume* 3*A*-3*B*, *Thin Films and Epitaxy*, 2nd Edition, Elsevier, Amsterdam, 941-995.

[22] Ferraro, M.E., Truskett, T.M. and Bonnecaze, R.T. (2016) Graphoepitaxy for Translational and Orientational Ordering of Monolayers of Rectangular Nanoparticles, *Physical Review*, **93**, Article ID: 032606. https://doi.org/10.1103/physreve.93.032606

[23] Buzynin, Yu., Shengurov, V., Zvonkov, B., Buzynin, A., Denisov, S., Baidus, N., Drozdov, M., Pavlov, D. and Yunin, P. (2017) GaAs/Ge/Si Epitaxial Substrates: Development and Characteristics. *AIP Advances*, **7**, Article ID: 015304. https://doi.org/10.1063/1.4974498

[24] Bogumilowicz, Y., Hartmann, J.M., Rochat, N., Salaun, A., Martin, M., Bassani, F., Baron, T., David, S., Bao, X.-Y. and Sanchez, E. (2016) Threading Dislocations in GaAs Epitaxial Layers on Various Thickness Ge Buffers on 300 mm Si Substrates. *Journal of Crystal Growth*, **453**, 180. https://doi.org/10.1016/j.jcrysgro.2016.08.022

[25] Wen, L., Gao, F., Zhang, X., Zhang, S., Li, J., Guan, Y., Wang, W., Zhou, S., Lin, Z. and Li, G. (2014) Effect of InGaAs Interlayer on the Properties of GaAs grown on Si (111) Substrate by Molecular Beam Epitaxy. *Journal of Applied Physics*, **116**, Article ID: 193508.

[26] Kohen, D., Made, R.I., Bao, S., Lee, K.H., Lee, K.E.K., Tan, C.S., Yoon, S.F. and Fitzgerald, E.A. (2015) Fabrication of III-V Virtual Substrate on 200 mm Silicon for III-V and Si Devices Integration. *CS MANTECH Conference*, Scottsdale, Arizona, 18-21 May 2015, 75.

[27] Buzynin, A. (2012) Fianite in Photonics. In: Hallman, D., Ed., *Advanced Photonic Sciences*, In Tech Europe, Croatia, 133-176. https://www.intechopen.com/books/advanced-photonic-sciences/fianite-in-photonics https://doi.org/10.5772/28812

[28] Buzynin, A.N., Buzynin, Y.N., Osiko, V.V., Panov, V.A., *et al*. (2011) Antireflection Fianite and ZrO_2 Coatings for Solar Cells. *Bulletin of the Russian Academy of Sciences*: *Physics*, **75**, 1213-1216. https://doi.org/10.3103/S106287381109005X

[29] Buzynin, A.N., Osiko, V.V., Buzynin, Yu.N., Zvonkov, B.N. and Zaslavski V.Y. (2010) Solar Cell. Russia Patent No. 99243.

[30] Buzynin, A.N., Buzynin, Yu.N. and Panov, V.A. (2012) Applications of Fianite in Electronics. *Advances in OptoElectronics*, **2012**, Article ID: 907560. http://www.hindawi.com/journals/aoe/2012/907560/ https://doi.org/10.1155/2012/907560

[31] Hill, T. and Huang, H. (2011) Fabricating Pinhole-Free YSZ Sub-Microthin Films by Magnetron Sputtering for Micro-SOFCs. *International Journal of Electrochemistry*, **2011**, Article ID: 479203. https://doi.org/10.4061/2011/479203

[32] Park, J., Lee, Y., Chang, I., Cho, G.Y., Ji, S., Lee, W. and Cha, S.W. (2016) Atomic Layer Deposition of Yttria-Stabilized Zirconia Thin Films for Enhanced Reactivity and Stability of Solid Oxide Fuel Cells. *Energy*, **116**, 170-176. https://doi.org/10.1016/j.energy.2016.09.094

[33] Qi, N., Sharma, W.J., Fretwell, R., Chen, J., Lee, X., Banerjee, J.C. and Electrical, S. (2000) Properties of ZrO_2 Gate Dielectric on SiGe. *Applied Physics Letters*, **76**, 502-504. https://doi.org/10.1063/1.125801

[34] Uzum, A., Kuriyama, M., Kanda, H., *et al*. (2017) Sprayed and Spin-Coated Multilayer Antireflection Coating Films for Nonvacuum Processed Crystalline Silicon Solar Cells. *International Journal of Photoenergy*, **2017**, Article ID: 3436271. https://doi.org/10.1155/2017/3436271