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An Explicit Surface-Potential Based Biaxial Strained-Si n-MOSFET Model for Circuit Simulation

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Abstract

In this paper, a charge sheet surface potential based model for strained-Si nMOSFETs is presented and validated with numerical simulation. The model considers sub band splitting in the 2-DEG at the top heterointerface in SiGe layer and also the dependence of electron concentration at heterointerface with the gate oxide. The model is scalable with strained-Si material parameters with physically derived flat-band voltages. An explicit relation for surface potential as a function of terminal voltages is developed. The model is derived from regional charge-based approach, where regional solutions are physically derived. The model gives an accurate description of drain current both in the weak and strong inversion regions of operation. The results obtained from the model developed are benchmarked with commercial numerical device simulator and is found to be in excellent agreement.

1. Introduction

As conventional Si MOSFETs are scaled into nanometer regime, maintaining performance enhancement beyond 90-nm technology node is becoming extremely difficult. Stress/strain engineering has now become indispensable to meet the performance targets of the International Technology Roadmap for Semiconductors (ITRS) for devices [1]. According to the ITRS roadmap, a precisely controlled process flow for the incorporation of new material such as, strained-Si in Si CMOS technology is becoming crucial for deep sub-micron CMOS devices.

Among the possible solutions, engineered substrates, in particular, substrate-induced strained silicon (strained-Si) has been identified as very promising for channel engineered MOSFETs as it improves the CMOS performance [2-6]. In this case, the strain is introduced at the substrate level before the transistor is built (opposite to process-induced strain currently being used in 45 nm technology node).

Due to strain introduction at the starting materials stage, global or wafer-scale strained-Si is more universal in nature and some of its attributes or specifications can be addressed more generally. The approach depends largely on materials engineering, rather than device design. The strain stretches the silicon lattice by about 1%.

For strained-Si, a graded layer of silicon germanium (SiGe) is grown on top of a bulk silicon wafer. A typically 2 μm thick SiGe layer having a 20-30% germanium concentration, with a higher concentration of germanium atoms at the top is used. Then a relatively thin layer of silicon, about 20-nm thick, is deposited on top of the SiGe layer. For detail, the reader may refer to the special issue on strained-Si: materials and devices [7]. The technology for the growth of high quality strained-Si layer on completely relaxed, step-graded, SiGe buffer layer has been reviewed by Maiti *et al*. [8-10].

Since early 1990s, strained-Si on silicon germanium (SiGe) substrates is being explored in an effort to boost CMOS performance [8,11,12]. The mobility advantage the strain offers at no significant additional processing cost which makes it an important candidate among various choices for performance enhanced devices. Until now, the substrate-induced biaxial strain has offered the best results for long channel (over 100% mobility enhancement) which, however, indeed occurs at low electric field and for high strain.

For biaxial tensile strain, the key component of the enhanced mobility results from the lowest energy subband having a low conductivity effective mass. Biaxial tension in strained-Si grown on relaxed-$Si_{1-x}Ge_x$ virtual substrates alters the Si band structure by splitting the

subband degeneracy in both the conduction and valence bands and reducing the band gap [13,14].

2. Strained-Si CMOS Technology

Towards strained-Si CMOS technology development, low temperature oxidation and the deposition of other dielectric film formation such as nitride, oxynitride on strained-Si have been reviewed in reference [15]. However, many issues remain unresolved. Currently, research in this area is mainly focused on its use for low power digital circuit design. However, as with all CMOS generations, there will eventually be strong interest in mixed-signal applications. The efficiency in the design of both the digital and analog integrated circuits depends very much on the accuracy of the analytical transistor models involved in the circuit simulation. In particular analog circuit simulation requires an accurate prediction of drain current as a function of the applied voltage.

Compact MOSFET models can be broadly classified into three categories, *i.e.* 1) threshold voltage based models, 2) inversion charge based models and 3) surface potential based models. The earliest MOSFET model included in the SPICE circuit simulator was threshold voltage based. However, inherent discontinuities in capacitances and conductances across different operating regions limit the use of this model [16]. Complexity is also an important constraint for the so-called compact transistor models; the model used should be as simple as possible in order to limit circuit simulation time. Moreover, it has been found that it fails to predict correctly the harmonics of intermodulation distortion in RF circuits [17]. Several compact models for bulk-Si MOSFETs have been developed and are in use for efficient IC design. Surface potential and inversion charge based compact models have been developed to avoid above problems [18-21].

The surface potential based model (SPBM) for the bulk MOSFET has now been widely accepted as the de-facto industry standard as it is able to predict the output characteristics accurately. But the problem with SPBMs is that an implicit equation has to be solved [22] to evaluate the correct surface potential (SP) in all regions of operation. However, the solution of these equations iteratively, using numerical algorithms [23], results in computational inefficiency and non-convergence in circuit simulators. In order to reduce computation time, an explicit, yet accurate, relation between surface potential Φ_s and the terminal voltages is preferable.

Several analytical models for threshold voltage have been reported in the literature [24-27]. However, to the best of our knowledge, there is no surface potential based analytical model of drain current for strained-Si n-MOSFETs considering the sub band splitting in the

two-dimensional electron gas (2-DEG). Such models would be necessary in order to incorporate these devices in the next generation CMOS VLSI circuit design.

In this paper, we report on the surface potential based analytical model for drain current of heterostructure strained-Si n-MOSFETs considering the carrier transport at the strained-Si/SiGe heterointerface as well as at strained-Si/SiO$_2$ interface. The physics-based model includes a regional approximated expression for weak and strong inversion and is scalable with the terminal bias and also strained-Si material parameters, such as, Ge mole fraction (x), strained-Si layer thickness (t_{SSi}) and wide doping range (N_{SSi}) considered in the investigation. The key idea is to derive physical relations of the flat-band voltages (V_{FB}) for the strained-Si devices and apply them to the regional surface-potential (Φ_s) and charge-based solutions that can be added to form a unified solution. In this work, our main focus has been in the weak to strong inversion region and to derive relations which are suited for circuit simulation. In Section 3, the analytical model for the current-voltage (I-V) characteristics for strained-Si n-MOSFETs has been developed. The results are compared with numerical simulated data in Section 4.

3. Analytical Model

3.1. Device Structure and Operation of Strained-Si n-MOSFETs

A schematic diagram of a strained-Si n-MOSFET is shown in **Figure 1**, where V_G, V_{ds}, and V_{bs} represent the gate, drain, and bulk voltages, respectively. It may be noted that for the n-MOSFET, V_G and V_{ds} are positive voltages while V_{bs} is usually negative. The device consists of a SiO$_2$ gate dielectric layer of thickness t_{ox}, and strained-Si layer of thickness t_{StSi}, and a relaxed SiGe buffer layer of thickness t_{SiGe}. These layers are grown on a p-type substrate.

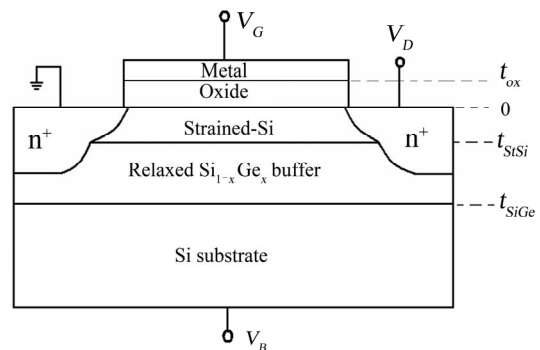Other important parameter for strained-Si MOSFETs

Figure 1. Cross-sectional view of a strained-Si n-MOSFET.

is the Ge mole fraction (x) in $Si_{1−x}Ge_x$, which not only determines the conduction-band discontinuity (ΔE_C) at the $Si/Si_{1−x}Ge_x$ heterointerface but also the mobility of electrons in the 2-DEG. The typical values of these parameters are t_{ox} = 10 nm, t_{SSi} = 20 nm, x = 0.20, and N_{SSi} = 1 × 10^{17} cm$^{−3}$. The depletion-layer width (W) in the doped silicon substrate extended as V_G is made more positive and reached a maximum value at V_G = V_{TSiGe}, when strong inversion occurs at the top heterointerface (x = t_{StSi}). With further increase in V_G, the sheet electron concentration in the 2-DEG in SiGe at the StSi/SiGe heterointerface will increase, resulting in an increased potential drop across the strained silicon and oxide layers. **Figure 2** shows the energy band diagram of the metal/SiO₂/strained-Si/SiGe/p-Si structure under this condition. At V_G = V_{TSSi}, the bands bend sufficiently to create inversion at the Si/SiO₂ interface. When $V_G > V_{TSSi}$, the drain-current (I_{ds}) is due to the flow of electrons in the strained-Si/SiGe heterojunction as well as the StSi/SiO₂ interface. For analytical modeling of the drain current of strained-Si/SiGe n-MOSFETs, it is necessary to obtain suitable expressions for the electron concentrations in both the channels as a function of V_G. This is discussed in the next two sub-sections.

3.2. Position of Fermi Level in Strained-Si Layer

The lattice mismatch between Si and Ge, which is 4.2% at room temperature, requires tensile or compressive strain of the active $Si_{1−x}Ge_x$ layer to match the in-plane lattice when it is pseudomorphically grown on a $Si_{1−y}Ge_y$ substrate layer ($x \neq y$) [2]. Strain changes the band structure and form band offset between the active material and the substrate material. This paper focused on the biaxial tensile strained-Si on relaxed SiGe heterostructure. Biaxial strain is composed of uniaxial extension in growth direction and a hydrostatic strain in all directions
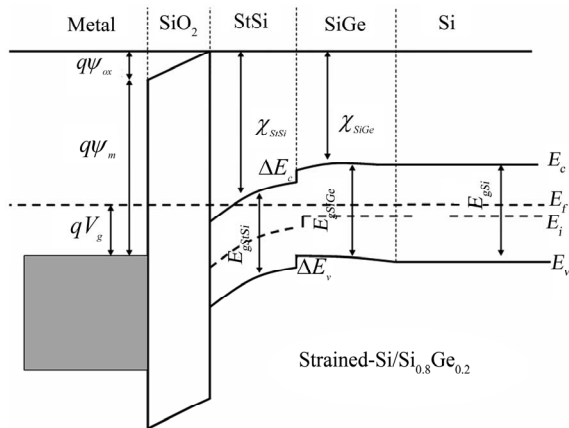

Figure 2. Energy band diagram of metal/SiO₂/SSi/SiGe/p-Si structure.

[2]. The uniaxial components give rise to splitting of degenerate energy levels, whereas the hydrostatic component give rise to uniform shift of the center of gravity [8]. Hydrostatic strain shifts the average position of the valence and the conduction band by $\Delta E_{v,av}$ and $\Delta E_{c,av}$, respectively [8],

$$\Delta E_{v,av} = a_v \left(2\varepsilon_\parallel + \varepsilon_\perp\right) = 2\varepsilon \frac{1-2\nu}{1-\nu} a_v \quad (1)$$

$$\Delta E_{c,av} = a_v \left(2\varepsilon_\parallel + \varepsilon_\perp\right) = 2\varepsilon \frac{1-2\nu}{1-\nu} a_c \quad (2)$$

where ν is Poisson's ratio. a_v and a_c are the numerical values of the hydrostatic deformation potentials. $\varepsilon_\parallel$ and $\varepsilon_\perp$ represents parallel (in-plane) and perpendicular (to the interface) strain tensor. ε represents the strain state of the semiconductor. For simplicity we assume the perpendicular direction in [001], a threefold degenerate valence band at k = 0 (light holes 1, heavy holes 2, spin-orbit split-off holes 3) and an indirect conduction band with sixfold degenerate Δ valleys (in the (100) directions). The biaxial strain in the epitaxial plane can be considered as hydrostatic deformation superposed by an uniaxial strain $(\varepsilon_\perp − \varepsilon_\parallel = E)$ perpendicular to the plane. In the absence of strain the threefold degeneracy of the valence band is already lifted by the spin orbit interaction and splits the bands by an amount of Δ_0. With respect to the average band position $E_{v,av}$ two bands are shifted up by an amount of $\frac{1}{3}\Delta_0$ (the light and heavy hole bands, which are denoted E_{v1}, E_{v2}), while one band is shifted down by an amount $\frac{2}{3}\Delta_0$ (the spin-orbit split-off band, which we denote E_{v3}). For completeness the relations of band offset, lifting of the valence band degeneracy by strain and spin-orbit interaction have been considered. The superposition of both effects is nonlinear for the light hole and spin orbit split-off band. The energy splitting of the valance bands is given by [8,28],

$$\Delta E_{v1} = -\frac{1}{6}\Delta_0 + \frac{b}{2}E + \frac{1}{2}\sqrt{\Delta_0^2 + 2\Delta_0 bE + 9b^2 E^2} \quad (3)$$

$$\Delta E_{v2} = \frac{1}{3}\Delta_0 - bE \quad (4)$$

$$\Delta E_{v3} = -\frac{1}{6}\Delta_0 + \frac{b}{2}E - \frac{1}{2}\sqrt{\Delta_0^2 + 2\Delta_0 bE + 9b^2 E^2} \quad (5)$$

Under the action of uniaxial strain along [001] direction, the bands along [100] and [010] directions split off from the one along the [001] direction, *i.e.* it lifts the sixfold degeneracy of the conduction band into the fourfold degenerate bands with energy minima lying in-plane and the twofold degenerate band with energy minima

lying perpendicular to the (001) plane. The uniaxial induced energy shifts of the conduction bands are given by [28]

$$\Delta E_{c,2}^{001} = \frac{2}{3} b_c \left(\varepsilon_\perp - \varepsilon_\parallel \right) = -\frac{2}{3} b_c \varepsilon \frac{1+\nu}{1-\nu} \qquad (6)$$

$$\Delta E_{c,4}^{100,010} = -\frac{1}{3} b_c \left(\varepsilon_\perp - \varepsilon_\parallel \right) = \frac{1}{3} b_c \varepsilon \frac{1+\nu}{1-\nu} \qquad (7)$$

For $a_v = 2$ eV, $a_c = 3$ eV, $b_v = -2.5$ eV, $b_c = 9$ eV, $\Delta_0 = 0$, $\nu = 1/3$ under either tensile biaxial strain of magnitude 0.01 the band average $E_{v,av}$ is shifted up by 20 meV. Tensile strain further shifts up the light hole (l h) energy levels by 100 meV while heavy holes (hh) are lowered by 50 meV and the spin-orbit split-off holes (soh) are degenerate ($\Delta_0 = 0$) with heavy holes at $k = 0$. As a result of tensile strain the light holes energy (E_{v1}) are lifted by 120 meV, while the heavy holes ($E_{v2} = E_{v3}$) are lowered by 30 meV.

The conduction band splitting ($\Delta E_{c,splitting}$) between the lower *m*-fold degenerate bands and the raised *n*-fold degenerate bands may be determined from Equations (6) and (7); where for tensile strain, $m = 2$ and $n = 4$ and in the case of compressive strain, $m = 4$ and $n = 2$. The effective density of states in the conduction band, $N_{c,SSi}$ is therefore defined by [29,30]:

$$N_{c,SSi} = 2 \left(m + n \exp \left(-\frac{\Delta E_{c,splitting}}{k_B T} \right) \right) \times \left(\frac{m k_B T}{2\pi \hbar^2} \right)^{3/2} \quad (8)$$

where k_B is the Boltzman constant, m is effective mass of electron. In the valance band, strain causes the splitting of degenerate valance bands at the Γ point. The splitting reduces the occupation in the lowered subvalleys and therefore decreases the density of states. The valance band splitting ($\Delta E_{v,splitting}$) can be obtained from Equations (3), (4) and (5). Thus $N_{v,SSi}$ can be obtained using an analysis analogous for $N_{c,SSi}$ [29,30]:

$$N_{V,SSi} = 2 \left(m_U^{3/2} + m_M^{3/2} \exp \left(-\frac{\Delta E_{v,splitting}}{k_B T} \right) \right) \times \left(\frac{k_B T}{2\pi \hbar^2} \right)^{3/2} \quad (9)$$

where m_U and m_M are the effective hole masses of the raised and lower band respectively. The contribution of spin split-off band ($v3$) have been neglected because it is far from the top of the valance band edge. The band gap and affinity can be expressed as:

$$E_{g,SSi} = E_{g,SiGe} + \Delta E_C - \Delta E_V \qquad (10)$$

$$\chi_{SSi} = \chi_{SiGe} - \Delta E_C \qquad (11)$$

where the indexes 'SSi' corresponds to the bandgap and affinity values for strained-Si. χ_{SiGe} is the electron affinity of the SiGe. Since, we are concerned with the strained-Si channel, valance and conduction band off-set are calculated with respect to strained-Si layer. Ge mole

fraction dependent expressions are given by [31,32]:

$$E_{g,SiGe}(x) = 1.155 - 0.43x + 0.0206x^2 \text{ [eV]} \ (0 < x < 0.85) \qquad (12)$$

$$N_{C,SiGe}(x) = \left[2.80 + (1.04 - 2.80)x \right] \times 10^{19} \text{ [cm}^{-3}] \qquad (13)$$

$$N_{V,SiGe}(x) = \left[1.04 + (0.60 - 1.04)x \right] \times 10^{19} \text{ [cm}^{-3}] \qquad (14)$$

where $E_{g,SiGe}$, $N_{C,SiGe}$, and $N_{V,SiGe}$ are the band gap, conduction and valence band densities of states in SiGe, respectively. To estimate the permittivity of the $Si_{1-x}Ge_x$ alloy, we use the Clausius-Mossotty relationship [33]:

$$\frac{\varepsilon_{SiGe} - 1}{\varepsilon_{SiGe} + 2} = (1-x) \frac{\varepsilon_{Si} - 1}{\varepsilon_{Si} + 2} + x \frac{\varepsilon_{Ge} - 1}{\varepsilon_{Ge} + 2} \qquad (15)$$

Based on the above relation, the following simplified expression may be obtained as:

$$\varepsilon_{SiGe} = \frac{2(A+B)+1}{1-(A+B)} \qquad (16)$$

where $A = (1-x) \frac{\varepsilon_{Si} - 1}{\varepsilon_{Si} + 2}$ and $B = x \frac{\varepsilon_{Ge} - 1}{\varepsilon_{Ge} + 2}$.

The above models are incorporated in the Sentaurus device [34] simulator (for comparison study) as well as in our analytical model. The intrinsic carrier density of strained-Si and SiGe layer may be expressed as,

$$n_{i,SSi} = \sqrt{N_{C,SSi} N_{V,SSi}} \left(-\frac{E_{g,SSi}}{2kT} \right) \qquad (17)$$

$$n_{i,SiGe} = \sqrt{N_{C,SiGe} N_{V,SiGe}} \left(-\frac{E_{g,SiGe}}{2kT} \right) \qquad (18)$$

where $N_{C,SSi}$ and $N_{V,SSi}$ are the conduction and valence band densities of states in strained-Si, respectively. Now an average Fermi potential in for strained-Si can be expressed as:

$$\phi_{F,SSi} = \frac{kT}{2q} \left[\ln \left(\frac{N_{SSi}}{n_{i,SSi}} \right) + \left[\ln \left(\frac{N_{SSi}}{n_{i,SiGe}} \right) \right] \right] \qquad (19)$$

3.3. Sheet Electron Concentrations in Channels as Functions of V_G

For strained-Si MOSFETs, the bandgap, affinity, density of states, and intrinsic carrier density of the strained-Si and SiGe layers are function of stress and Ge mole fraction in the $Si_{1-x}Ge_x$ layer. An accurate determination of the voltages at which electron accumulation at different interfaces occurs is the key to the physical modeling of the charges in strained-Si MOSFETs. Here we use subscripts "1" and "2" to denote physical quantities at the strained-Si/SiO_2 and strained-Si/SiGe interfaces, respectively. The strained-Si flat band (ignoring depletion

within a thin layer of Debye length) is defined as the voltage at which the accumulation starts at the strained-Si/SiO$_2$ interface and is given by,

$$V_{FB1} = \phi_M - \left(\chi_{SSi} + \frac{E_{g,SSi}}{2} + \phi_{F,SSi} \right) - \frac{Q_{ox}}{C_{ox}} \quad (20)$$

Hole accumulation at the strained-Si/SiGe interface occurs when V_{GB} reaches the flat band voltage V_{FB2}, at which the top strained-Si layer is depleted of mobile charges. At $V_{GB} = V_{FB2}$, a thin layer equivalent to the Debye length is also depleted. V_{FB2} can be calculated from the Poisson's solution as

$$V_{FB2} = \phi_M - \left(\chi_{SiGe} + \frac{E_{g,SiGe}}{2} + \phi_{F,SSi} \right) - \frac{Q_{ox}}{C_{ox}} +$$

$$\frac{q\left(t_{SSi} N_{SSi} + N_{SiGe} L_D\right)}{C_{ox}} + \frac{q N_{SSi} t_{SSi}^2}{2\varepsilon_{SSi}} + \frac{q N_{SiGe} L_D t_{SSi}}{\varepsilon_{SiGe}} + \frac{q N_{SiGe} L_D^2}{2\varepsilon_{SiGe}}$$

$$= V_{FB1} + \Delta V_{FB}$$

$$(21)$$

where $\Delta V_{FB} = \Delta E_C + \frac{\Delta E_g}{2} + \Delta V_{fb} \quad (22)$

$$V_{fb} = \frac{q\left(t_{SSi} N_{SSi} + N_{SiGe} L_D\right)}{C_{ox}} + \frac{q N_{SSi} t_{SSi}^2}{2\varepsilon_{SSi}}$$

and

$$+ \frac{q N_{SiGe} L_D t_{SSi}}{\varepsilon_{SiGe}} + \frac{q N_{SiGe} L_D^2}{2\varepsilon_{SiGe}} \quad (23)$$

is the flat band shift due to the charges and potential drops in the strained-Si and the Debye length in SiGe is, given by

$$L_D = \sqrt{\frac{kT \varepsilon_{SiGe}}{q^2 N_{SiGe}}} \quad (24)$$

The depletion region should lie between V_{FB2} and V_t, since below $V_{FB2,}$ holes start to accumulate at the strained-Si/SiGe interface.

3.4. Drain-Current Model

The Pao-Sah relation [35] for surface potential based bulk Si MOSFET is given by,

$$V_{GB} - V_{FB} - \phi_s =$$

$$\gamma \sqrt{\phi_s + u_t \left[\exp\left(-\frac{\phi_s}{u_t}\right) - 1 \right] + u_t \exp\left(\frac{-V - 2\phi_F}{u_t}\right) \times \left[\exp\left(\frac{\phi_s}{u_t}\right) - 1 \right]}$$

$$(25)$$

where V_{FB} is the flatband voltage, u_t is the thermal voltage defined by kT/q, ϕ_F is the strained-Si Fermi potential defined by Equation (19) and γ is the body factor defined by $\sqrt{2q\varepsilon_{Si} N_{SSi}} / C_{ox}$ and the gate oxide capacitance per unit area C_{ox} is given by ε_{ox}/t_{ox}. The bulk referenced quasi-Fermi potential V is equal to V_{bs} and V_{bd} at

the source and drain end, respectively. The above relation is valid for all values of gate-bulk voltage V_{GB} and gives an accurate description in all regions of operation (accumulation, depletion and inversion). In the useful range of operation (depletion and inversion region), ϕ_s is positive and generally $\gg u_t$. So, the Pao-Sah relation reduces to

$$V_G - V_{FB} - \phi_s = \gamma \sqrt{\phi_S + u_t \exp\left(\frac{\phi_s - V - 2\phi_F}{u_t}\right)} \quad (26)$$

In the weak-threshold region ($V_{FB1} < V_G < V_t$) or ($0 < \phi_{s1} < 2\phi_F + V$), the exponential term in Equation (26) becomes negligible and we get a quadratic equation for surface potential. They are calculated from Pao-Sah equation as

$$\phi_{wi,1} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_G - V_{FB1}} \right)^2 \quad (27)$$

and $Q_{b,wi,1} = -C_{ox} \gamma \sqrt{\phi_{wi,1}} \quad (28)$

For strong inversion region ($V_G > V_t$) or ($\phi_s > 2\phi_F + V$), the exponential term in Equation (25) becomes dominant. A fairly accurate approximate expression of surface potential in this region can be obtained by considering all the ϕ_s apart from the dominant exponential term of Equation (26) to be constant at a value of $2\phi_F + V$. Thus,

$$\phi_{SSi,1} = 2\phi_F + V + u_t \times \ln\left[\frac{1}{u_t} \times \left\{ \left(\frac{V_G - V_{FB1} - \phi_B}{\gamma} \right)^2 - \phi_B + u_t \right\} \right]$$

$$(29)$$

For conduction in the s-Si/SiGe interface, the depletion region should lie between V_{FB2} and V_t, since below V_{FB2}, holes start to accumulate at the strained-Si/SiGe interface. Thus the regional depletion charge from Poissons solution is given by

$$Q_{b,wi,2} = -C_{ox} \gamma \sqrt{\phi_{wi,2}} \quad (30)$$

where $\phi_{wi,2} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_G - V_{FB2}} \right)^2 \quad (31)$

As for the other interface, a smoothing parameter is used to avoid negative square roots in the equation for surface potential and to make it continuous with the accumulation region. However, we have not included the accumulation region yet in our model. On similar lines, for strong inversion region,

$$\phi_{SSi,2} = 2\phi_F + V +$$

$$u_t \times \ln\left[\frac{1}{u_t} \times \left\{ \left(\frac{V_G - V_{FB2} - \phi_B}{\gamma} \right)^2 - \phi_B + u_t \right\} \right] \quad (32)$$

For any interface, at any region total current is the sum of the drift component (I_{drift}) and the diffusion component (I_{diff}) with the surface potential being used in the relations corresponding to the regions of weak or strong inversion for the different interfaces. For the calculation of the drain current I_{ds}, the stress induced mobility μ have been taken [35]. Again under the assumption of the gradual channel approximation and the charge sheet approximation, the drain current may be written as [36-38]:

$$I_{ds} = I_{drift} + I_{diff} \tag{33}$$

where the drift component I_{drift} and diffusion component I_{diff} are given by:

$$I_{drift} = \mu C_{ox} \frac{W}{L} \left\{ \left(V_G - V_{FB} - \frac{\phi_{sL} + \phi_{s0}}{2} \right) (\phi_{sL} - \phi_{s0}) - \frac{2}{3} \gamma \left(\phi_{sL}^{3/2} - \phi_{s0}^{3/2} \right) \right\} \tag{34}$$

and

$$I_{diff} = \mu C_{cox} \frac{W}{L} u_t \left\{ \gamma \left(\phi_{sL}^{1/2} - \phi_{s0}^{1/2} \right) + \left(\phi_{sL} - \phi_{s0} \right) \right\} \tag{35}$$

Here ϕ_{s0} and ϕ_{sL} denote the electrostatic surface potential at the source and drain side, respectively and required to calculate I_{ds}, are obtained numerically under the following boundary conditions

$$\phi_s = \begin{cases} \phi_{s0} & for \ V = V_{sb} \\ \phi_{sL} & for \ V = V_{sb} + V_{ds} \end{cases} \tag{36}$$

where V_{sb} and V_{ds} are the source to substrate and drain voltage, respectively. In sub-threshold region, ϕ_{s0} is almost equal to ϕ_{sL}, and even a small error in the value of ϕ_{s0} and ϕ_{sL} can lead to a large error in the diffusion current (I_{diff}), which depends on difference of $\phi_{sL} - \phi_{s0}$. Therefore, an accurate value is required for surface potential, particularly for current calculations. With the help of Equation (26), the above difficulty can be simplified by rewriting Equation (35) as:

$$I_{diff} = \mu C_{cox} \frac{W}{L} u_t \gamma \{ (\sqrt{\phi_{s0} + u_t \exp(\frac{\phi_s - V_{SB} - 2\phi_F}{u_t})} - \sqrt{\phi_{sL} + u_t \exp(\frac{\phi_s - V_{DB} - 2\phi_F}{u_t})}) + \left(\phi_{sL}^{1/2} - \phi_{s0}^{1/2} \right) \} \tag{37}$$

In our model, we have considered the two drain-current components separately, *i.e.*, I_{ds}^{SiGe} at the 2-DEG in SiGe and I_{ds}^{SSi} at the strained-Si/SiO$_2$ interface.

1) *Current in the 2-DEG in SiGe I_{ds}^{SiGe}*: The dominant component of the current in the weak inversion region is due to the diffusion of electrons in SiGe layer and in strong inversion region is due to the drift of electrons in the 2-DEG in SiGe due to the application of a drain voltage (V_{ds}). When the current flows in SiGe layer, the channel potential with respect to the source rises con-

tinuously from source to the drain. For $V_{FB1} < V_G < V_{FB2}$, current is dominated only by diffusion component.

2) *Current at the strained-Si/SiO$_2$ Interface I_{ds}^{SSi}*: The dominant component of the current in the weak inversion region is due to the diffusion of electrons in strained-Si layer and in strong inversion region is due to the drift of electrons in the 2-DEG in strained-Si due to the application of a drain voltage (V_{ds}). When the current flows in strained-Si layer, the channel potential with respect to the source rises continuously from source to the drain. When $V_{FB2} < V_G < V_{TSiGe}$, the diffusion components of current in strained-Si and SiGe layer are dominant. V_{TSiGe} is the threshold voltage for strained-Si/SiGe heterolayers.

So,

$$I_{ds} = I_{ds,diff}^{SSi} + I_{ds,diff}^{SiGe} \tag{38}$$

Now, we consider a threshold voltage for the channel at the strained-Si/SiO$_2$ interface denoted by V_{TSSi} which is defined as the gate voltage at which the potential at the strained-Si/SiO$_2$ interface is equal to $2\phi_F$. For $V_{TSiGe} < V_G < V_{TSSi}$ current is flowing for the drift component of the current in SiGe layer and diffusion component of current in strained-Si layer. Thus

$$I_{ds} = I_{ds,drift}^{SiGe} + I_{ds,diff}^{SSi} \tag{39}$$

Also, for $V_G > V_{TSSi}$ drift currents flow through both the layers in the strong inversion region. Hence

$$I_{ds} = I_{ds,drift}^{SiGe} + I_{ds,drift}^{SSi} \tag{40}$$

4. Results and Discussion

The surface potential ϕ_s as a function of gate voltage (V_G) for bulk-Si and strained-Si MOSFETs are shown in **Figure 3**. To reduce the computational time and maintain the accuracy, an explicit description of surface potential with regional approximations has to be made to Equation (25). A distinction can be made between weak inversion and strong inversion, as indicated in **Figure 3**. In the weak inversion region $0 < \phi_s < 2\phi_F + V_G$, the exponential term in Equation (25) is negligible as shown in Equations (27) and (31). In the strong inversion region, $\phi_s > 2\phi_F + V_G$ and the exponential term in Equation (25) becomes dominant. Accurate expression for surface potential in strong inversion is expressed in Equations (29) and (32) [35]. The surface potential becomes practically independent of high gate voltage and become saturate.

The drain current for an ideal long-channel MOSFET given by Equations (38), (39) and (40), has been calculated using surface potential values. The complete current-voltage (I_{ds}-V_G) characteristics obtained using the surface potential model (dashed-dot lines), are shown in **Figure 4.** The figure shows the drain current (I_{ds}) and its component diffusion current (I_{diff}) and drift current (I_{drift}),
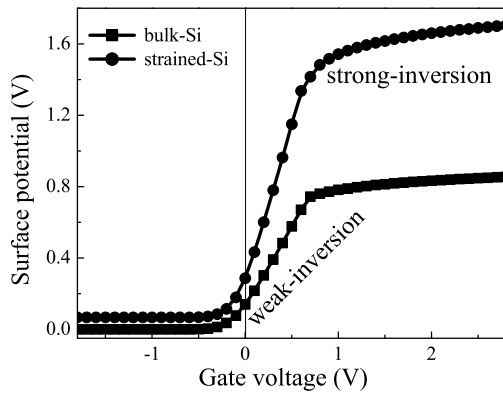
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Figure 3. The electrostatic surface potential Φ_s as a function of gate voltage V_G. The results of the weak and strong inversion approximation are shown for bulk-Si and strained-Si MOSFETs.

Figure 4. The drain current as a function of gate voltage (V_G) based on surface-potential model. Diffusion current (I_{diff}), drift current (I_{drift}), and total current ($I_{ds} = I_{diff} + I_{drift}$) for both bulk-Si and strained-Si MOSFETs.

as a function of V_G at V_{ds} = 0.1 V and V_{sb} = 0 V. As can be seen from the figure, in strong inversion $I_{ds} \approx I_{drift}$ (dotted line) so that the current is mainly due to drift velocity of electrons. In weak inversion $I_{ds} \approx I_{diff}$ (dotted line) and the current is mainly due to diffusion of electrons.

The model has been successfully implemented in MATLAB. To validate our model, the results obtained from MATLAB are compared with the simulated data obtained using Sentaurus device simulator [34]. **Figure 5** shows current-voltage characteristics comparison between the results obtained from the model with results obtained from Sentaurus simulation. In practice, however, the electrical characteristics of a MOSFET deviate from the simulated behavior. This is due to the fact that various physical effects, such as, mobility reduction, velocity saturation, series resistance, channel length modulation, static feedback, drain induced barrier lowering and weak-avalanche amongst others can be fully captured in simulation. In the following, we develop the drain current model for strained-Si nMOSFETs based on regional approximations to circumvent the implicit relations for Φ_s discussed above. This is done by separately modeling weak and strong inversion regions. However, there is a region between the weak and strong inversion, called the moderate inversion, where both the drift and diffusion components are important and this region can be easily modeled using a smoothing function [39]. We have employed polynomial fits to get good accuracy in moderate inversion region. A close match is found with simulated data considering 4th order polynomial fit. This type of model can be used for circuit simulation because of its simplicity and accuracy. Device simulations have been performed using Sentaurus device tool [34]. The transport parameters used in the drift-diffusion simulation have been taken from the *StrainedSilicon.par* parameter file.
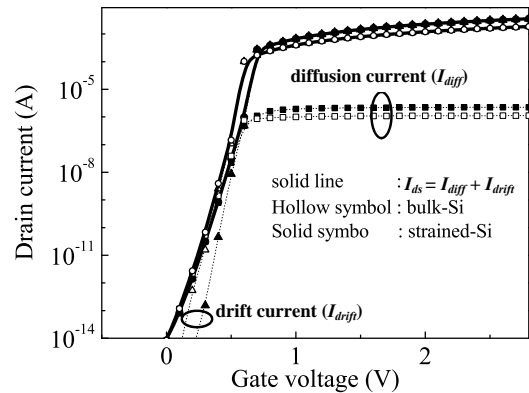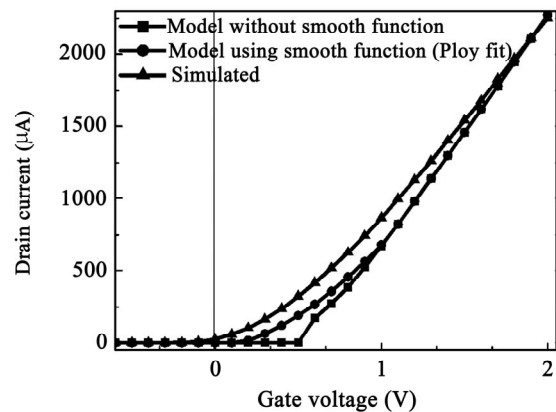

Figure 5. Comparison of current-voltage characteristics obtained from the model developed with results obtained from Sentaurus simulation.

5. Conclusions

A charge sheet surface potential based analytical model for strained-Si MOSFETs is presented and validated with numerical simulation. The model considers the sub band splitting in the 2-DEG at the top heterointerface in the SiGe layer and also the heterointerface at the strained-Si/SiO$_2$ interface. The model is scalable with strained-Si material parameters with physically derived flat band voltages. The model is developed based on the regional charge-based approach, where regional solutions are physically derived. The developed model may be used for circuit simulation involving strained-Si MOSFETs for the next generation ULSI circuits. The modeling of ultra-short (below 90 nm) channel strained-Si devices, however, will require further developments on precise description of physical effects such as series resistance, velocity saturation, channel length modulation, static

feedback, self-heating and drain induced barrier lowering.

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