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Quasi-Square Wave Mode Phase-Shifted PWM LCC Resonant Converter for Regulated Power Supply

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Abstract

This paper presents an improved self sustained oscillating controller circuit using LCC components for improving the overall efficiency of the system. It has a micro controller based active controller, which controls the performance from no-load up to full-load. The steady state characteristics are developed and a design example is given in detail. The proposed controller allows zero current switching at any loading condition which results in a reasonable reduction of power loss during switching with a promising efficiency. Analytical and experimental results verify the achievement the design specifications.

Keywords: Zero Voltage Switching, Zero Current Switching, DC-DC Converter, Resonant Converter, Soft Switching

1. Introduction

With ever increasing concerns about electromagnetic compatibility (EMC) issues, more attention is being paid to resonant converters as they provide better sinusoidal waveforms. Furthermore, resonant converters can make use of natural oscillation to achieve zero voltage switching (ZVS) and/or zero current switching (ZCS) thus eliminating switching losses [1]. As such both higher power-packing densities and conversion efficiencies can be achieved at high switching frequencies without snubbers. The full-bridge converter is widely used in power dc–dc conversions because it can achieve soft-switching with the help of LCC components added in the circuit [2]. The soft-switching techniques for PWM full bridge converter can be classified into two kinds: one is zero-voltage-switching (ZVS) and the other is zero-current-switching (ZCS). For dc-dc power conversion applications, the conventional phase-shift full-bridge dc/dc converter has drawn more attention in recent decades due to its advantages: high conversion efficiency, high power density, and low electro magnetic interference [3–8]. In order to obtain high conversion efficiency for dc-dc power conversion applications, a soft-switched dc/dc converter with a LCC primary-side energy storage elements based on [9–12] is studied and implemented in this paper.

Section II presents the principle of operation of the LCC resonant converter. Successively, the Section III deal with the mathematical analysis of converter. The performance characteristics of the converter are obtained from the mathematical analysis in section IV. An optimum design procedure of this converter is proposed in section V paper only after having a study on the performance characteristics of the LCC resonant converter and it can be considered as a design reference for other engineers. Finally, a 100-kHz, 48W (40V/1.2A) laboratory-made prototype is built up to verify all the theoretical analysis and evaluation. The highest full-load conversion efficiency of this converter reaches about 95.56%. Compared with the traditional dc/dc converter, its advantage in high conversion efficiency shows good potential for various dc-dc power converter applications. Finally, some conclusions of the work are provided in Section IX.

2. Principle of Operation

Like switch mode dc-to-dc converter, resonant converters are used to convert dc-to-dc through an additional conversion stage: the resonant stage in which dc signal is converted to high frequency ac signal. The potential

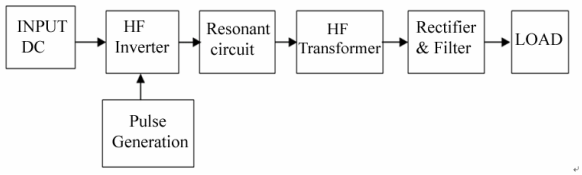

Figure 1. Block diagram.

advantage of resonant converter include the natural commutation of power switches, resulting in low switching power dissipation and reduced component stresses, which in terns results in increased power efficiency and increased switching frequency; higher operating frequencies results in reduced size and weight of equipment and results in faster responses; possible reduction in EMI problems. Since the size and weight of the magnetic components (inductors and transformers) and capacitors in a converter are inversely proportional to the converter switching frequency, many power converters have been designed at progressively higher frequencies in order to reduce excessive size and weight and obtain fast converter transients. In recent years, the market demand for wide applications that need variable speed drives, highly regulated power supplies, uninterruptible power supplies, and the desire to have smaller size and lighter weight power electronics systems has been increased. There are many soft witching techniques available in the literature to improve the switching behavior of dc-to-dc resonant converters. At the time of writing these words, intensive research in soft switching is under way to further improve efficiency with increased switching frequency of power electronic circuits**.**

A dc-to-dc resonant converter can be described by the major circuit blocks as shown in Figure 1. The dc-to-ac input inversion circuit, the resonant energy buffer tank circuit, and the ac-to-dc output rectifying circuit. Typically, the dc to ac inversion is achieved by using a various types of switching network topologies. The resonant tank which serves as an energy buffer between the input and output is normally synthesized by using lossless frequency selective network. The purpose of that network is to regulate the energy flow from the source to the load. Finally, the ac-to-dc conversion is achieved by incorporating rectifier circuits at the output section of the converter.

3. Mathematical Analysis of Converter

Figure 2 shows the A.C. equivalent circuit of LCC

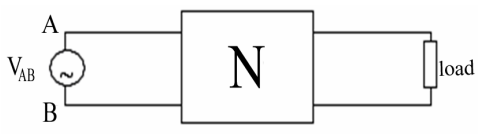

Figure 2. A.C equivalent circuit of LCC resonant converter.

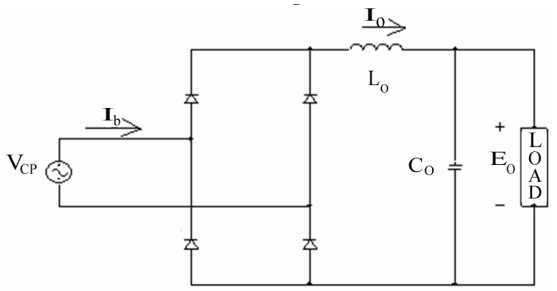

Figure 3. Output circuit of bridge rectifier and filter component to resonant converter.

resonant converter. The following assumptions are used in the mathematical analysis of the series parallel resonant converter.

1) The switches, diodes, inductors, capacitors and snubber components used are ideal.

2) The effects of snubber are neglected.

3) The filter inductance is large enough to keep the load current constant.

4) The high frequency transformer is ideal and has unity turns ratio.

Where N - is the resonant network, R_{ac} - AC equivalent load resistance, V_{AB} - RMS fundamental component of $V_{AB.}$

From the output circuit of bridge rectifier and filter component to resonant converter fig.3, V_{cp} and I_b represent the rms fundamental component of V_{cp} (t) and I_b (t) respectively. The output circuit consists of the diode bridge rectifier and inductive filter present in the output circuit.

The D. C. output voltage is obtained as the average of A.C. input voltage, V_{cp}

$$E_0 = \frac{1}{\pi}\int_0^{\pi} \sqrt{2}V_{cp} \sin \omega t d(\omega t) \tag{1}$$

$$E_0 = \frac{2\sqrt{2}}{\pi} V_{cp} \tag{2}$$

$\omega = 2\pi f$ and f is the switching frequency. The rms value of the fundamental component of Diode Bridge current is calculated using Fourier analysis as

$$I_b = \frac{1}{\sqrt{2}\pi}\int_0^{2\pi} i_b(t) \sin \omega t d(\omega t) \tag{3}$$

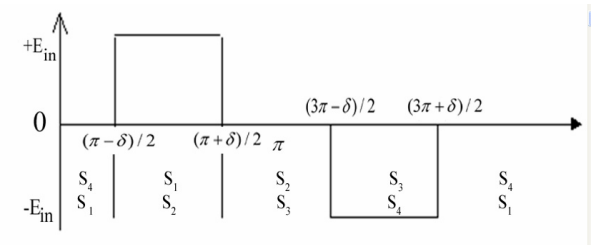

Figure 4. Quasi-square voltage waveform of LCC resonant converter.

$$I_b = \frac{2\sqrt{2}}{\pi} I_0 \tag{4}$$

Using Equation (2) & (4) the equivalent A. C. resistance as seen at the input of the rectifier bridge is given by

$$R_{ac} = \frac{V_{cp}}{I_b} = \frac{\pi^2}{8} R_L \tag{5}$$

δ and D are related by:

$$\delta = \pi D \tag{6}$$

The duty ratio D is defined as the ratio of the time duration for which the switch S_1 & S_2 or S_3 & S_4 are switched on simultaneously i.e. t_{on} to the half of the switching period (T/2) i.e., D = t_{on}/ (T/2).When the switches S_1 and S_2 (S_3 or S_4) are switched on simultaneously, the voltage across A and B is the input voltage E_{in}.

The R.M.S. fundamental Voltage across A and B is given by:

$$V_{AB} = \frac{1}{\sqrt{2}\pi} \int_0^{2\pi} V_{AB}(t) \sin \omega t d(\omega t) \tag{7}$$

$$V_{AB} = \frac{1}{\sqrt{2}\pi} \left[\int_{(\pi-\delta)/2}^{(\pi+\delta)/2} E_{in} \sin \omega t d(\omega t) - \int_{(3\pi-\delta)/2}^{(3\pi+\delta)/2} E_{in} \sin \omega t d(\omega t) \right] \tag{8}$$

$$V_{AB} = \frac{2\sqrt{2} E_{in} \sin \delta/2}{\pi} \tag{9}$$

The equivalent circuit of the converter across the terminal A and B shown in Figure 2 is replaced by its equivalent circuit shown in Figure 5. In order to simplify the presentation, all the equations are normalized using the following base quantities.

Base voltage = E_{in}

Base impedance = $\omega_0 L$

Base current = $E_{in} / \omega_0 L$

Base frequency $\omega_0 = 1/\sqrt{LC}$

The RMS fundamental voltage across the parallel

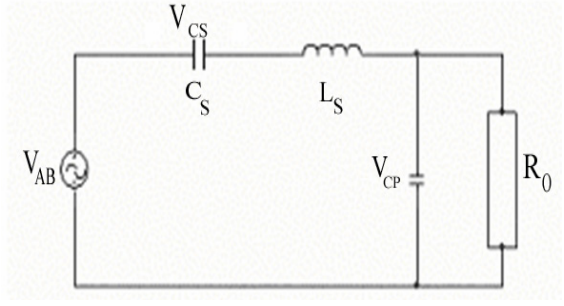

Figure 5. AC equivalent circuit of resonant converter.

capacitor C_p is given by:

$$V_{cp} = \left[\frac{V_{AB}}{j(X_L - X_{cs}) + \frac{1}{\frac{1}{R_{ac}} - \frac{1}{jX_{cp}}}} \right] \times \left(\frac{1}{\frac{1}{R_{ac}} - \frac{1}{jX_{cp}}} \right) \tag{10}$$

here

$$X_L = \omega L,\ X_{cs} = 1/\omega C_s,\ X_{cp} = 1/\omega C_p \tag{11}$$

Substituting the Equation (11) in Equation (10), the equation becomes

$$V_{cp} = \frac{V_{AB}}{1 + \frac{C_P}{C_S} - \omega^2 L C_P + j\frac{8}{\pi^2}} \times \frac{\omega L}{R_L} - \frac{1}{\omega C_S R_L} \tag{12}$$

Substituting the Equation (9) in Equation (12) and after simplification, the equation becomes

$$V_{cp} = \frac{2\sqrt{2} E_{in} \sin \delta/2}{\pi \times \left[\left(\frac{m+1}{m} \right)(1 - y^2) + \frac{8}{\pi^2} jQ \left(y - \frac{1}{(m+1)y} \right) \right]} \tag{13}$$

where

$$m = C_s / C_p,\ Q = \omega_o L / R_L = 1/\omega_o C R_L,\ y = \omega/\omega_o \tag{14}$$

Substituting Equation (13) in Equation (2) and after normalization, the equation becomes

$$\frac{E_0}{E_i} = \frac{\sin \delta/2}{\frac{\pi^2}{8}\left(\frac{m+1}{m} \right)(1 - y^2) + jQ\left(y - \frac{1}{(m+1)y} \right)} \tag{15}$$

The equivalent impedance across the terminals A and B is given by

$$Z_{eq} = j(X_L - X_{CS}) + \frac{1}{\frac{1}{R_{ac}} - \frac{1}{jX_{CP}}} \tag{16}$$

Substituting Equation (5), Equation (11) in Equation (14), the equation becomes

$$Z_{eq} = \left[j\left(\frac{\omega L}{R_L} - \frac{1}{\omega C_S R_L} \right) + \frac{1}{\frac{8}{\pi^2} + j\omega C_P R_L} \right] \tag{17}$$

Using Equation (11) in Equation (17) and after simplification, the equation becomes

$$Z_{eq} = \left[jR_L Q \left(y - \frac{1}{(m+1)y} \right) + \frac{1}{\frac{8}{\pi^2} + j\frac{y(m+1)}{Qm}} \right] \tag{18}$$

After simplification and rearranging the terms we get

$$Z_{eq} = \omega_0 L \frac{B_1 + jB_2}{B_3} \tag{19}$$

where

$$B_1 = \frac{8Q}{\pi^2}\left[\frac{m}{y(m+1)}\right]^2 \quad (20)$$

$$B_2 = \left[y - \frac{1}{y(m+1)}\right]B_3 - \frac{m}{y(m+1)} \quad (21)$$

$$B_3 = 1 + \left[\frac{8Qm}{\pi^2 y(m+1)}\right] \quad (22)$$

Normalizing Equation (19), the equation becomes

$$Z_{eqpu} = \frac{B_1 + jB_2}{B_3} = \left|Z_{eqpu}\right| e^{j\Psi} \quad (23)$$

$$\left|Z_{eqpu}\right| = \frac{\sqrt{B_1^2 + B_2^2}}{B_3^2} \quad (24)$$

Impedance angle

$$\Psi = \tan^{-1}\frac{B_1}{B_2} \quad (25)$$

The resonant link current I

$$I = \frac{V_{AB}}{Z_{equ}} \quad (26)$$

$$I = \left|I\right| \angle -\psi \quad (27)$$

where

$$\left|I\right| = \frac{V_{AB}}{\left|Z_{equ}\right|} \quad (28)$$

Substituting Equation (9) in Equation (4) and after normalization, the equation becomes

$$\left|I\right|_{pu} = \frac{2\sqrt{2}\sin\frac{\delta}{2}}{\pi\left|Z_{equ}\right|} \quad (29)$$

Peak Inductor is given by

$$\left|I\right|_{ppu} = \sqrt{2}\left|I\right|_{ppu} = \frac{4\sin\frac{\delta}{2}}{\pi\left|Z_{equ}\right|} \quad (30)$$

$$\left|V_{cs}\right|_{ppu} = \left|I\right|\frac{X_{cs}}{\omega_0 L} \quad (31)$$

Using (30) Peak Voltage across C_s is calculated as

$$\left|V_{cs}\right|_{ppu} = \frac{\left|I\right|_{ppu}}{y(m+1)} \quad (32)$$

The peak Voltage across C_P is obtained using Equation (1) and rearranging the terms.

$$\left|V_{cp}\right|_{ppu} = \frac{\pi}{2}\left|\frac{E_O}{E_{in}}\right| \quad (33)$$

The load ripple voltage is given by,

$$V_{ac} = \left[V_{crms}^2 - V_c^2\right]^{1/2} \quad (34)$$

V_{crms} is the total rms load voltage. V_o is the average load voltage.

The Voltage ripple factor, which is a measure of the ripple content, is given by the equation

$$RF = \frac{V_{ac}}{V_c} \quad (35)$$

Similarly the Voltage ripple factor using the filter elements is given by the equation

$$RippleFactor = \frac{V_{2rms}}{V_c} \quad (36)$$

where V_{2rms} represents the rms value of the second harmonic component.

$$V_{2rms} = \frac{V_m}{3\sqrt{2}\pi\omega^2 LC} \quad (37)$$

where V_m represents the maximum value of voltage after rectification.

The efficiency of the converter is calculated using the expression

$$\%\eta = \frac{P_{out}}{P_{in}} \times 100 \quad (38)$$

4. Performance Characteristics

4.1. Variation of Input Impedance Magnitude and Phase Angle vs. Normalized Switching Frequency

The effect of impendence on circuit performance has been studied using Equation (19) to Equation (22) and have been used to draw the curves of the variation of the normalized input impedance magnitude and impedance phase angle, with change in normalized switching yield stress for various values of Q are shown in Figure 6 and Figure 7 respectively.

It can be seen that for a particular value of quality factor Q the impedance magnitude decreases as the frequency increases up to a certain value, after which it increases with frequency, but with less effect. The effect of quality factor variation can also be observed. As Q decreases the input impedance magnitude verses normalized switching frequency curve shifts towards higher frequency. It is observed that at about 0.9pu frequency, all the input

impedance magnitude curve converges and diverges as the frequency increases.

From impedance phase angle curves the boundary between operation below and above resonance can be identified. The frequency at which the impedance phase angle Ψ is equal to zero is defined as f_r. This frequency forms boundary between leading power factor and lagging power factor operation. For $f<f_r$, Ψ<0, the resonant circuit represents a capacitive load (below resonance operation), for $f>f_r$, Ψ>0 the resonant circuit represents an inductive load (above resonance operation). It is seen from Figure 7 that f_r depends on Q.

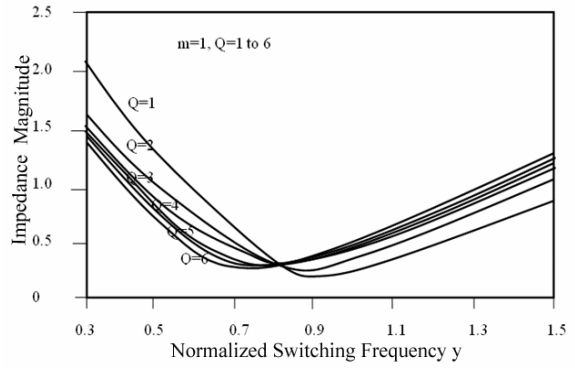

Figure 6. Variation of impedance magnitude versus normalized switching frequency for various values of Q with m = 1.

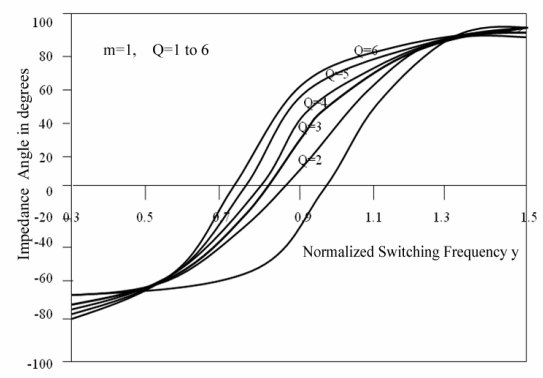

Figure 7. Variation of impedance angle in degrees versus normalized switching frequency for various values of Q with m = 1.

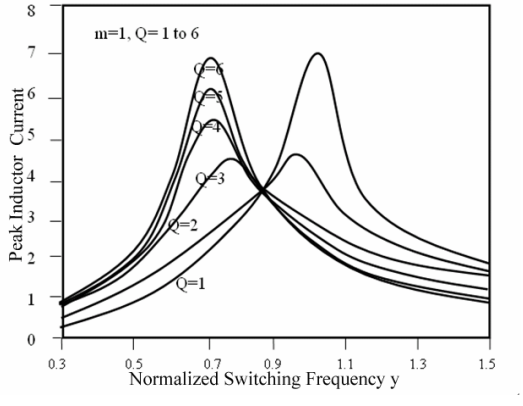

Figure 8. Variation of peak inductor current versus normalized switching frequency for various values of Q with m = 1.

4.2. Variation of Peak Inductor Current vs. Normalized Switching Frequency

Equation 30 shows that peak inductor current is a function of Q and y. Figure 8 shows that peak inductor current increases with increase in Q, since the output voltage decreases for the same output power. But for a given value of y, it can be seen peak current decreases as load current increases with increase in value of Q.

4.3. Variation of Duty Ratio vs. Q for M=1

The qualitative analysis of the relationship between duty ratio and quality factor Q is made. Figure 9 to Figure 16 show how the duty ratio D varies as Q changes, to keep output load voltage constant at particular value. These curves are obtained by solving Equation 15 numerically for duty ratio as a function of Q for various values of converter gain Eo/Ein (for 0.7 to 1.0) and various switching frequency (yield stress = 0.7 to 0.9).

It is observed that as the Eo/Ein decreases, the duty ratio versus Q curves shifts downwards. The increase in value of yield stress results in shrinkage of D vs. Q Curve ranges. However when Cs/Cp ratio is observed that the above two characteristics are intensified. The detailed analysis offers each figure is given in the following paragraphs.

If the normalized frequency is further increased, the graphs show similar pattern as described above. Figure 10, Figure 11 and Figure 12 are shown for yield stress y= 0.8,

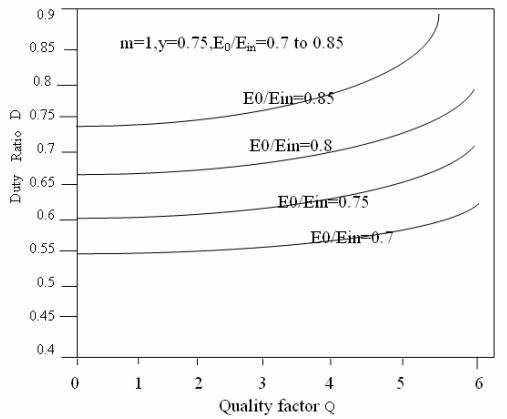

Figure 9. Variation of duty ratio versus quality factor with m = 1, y = 0.75.

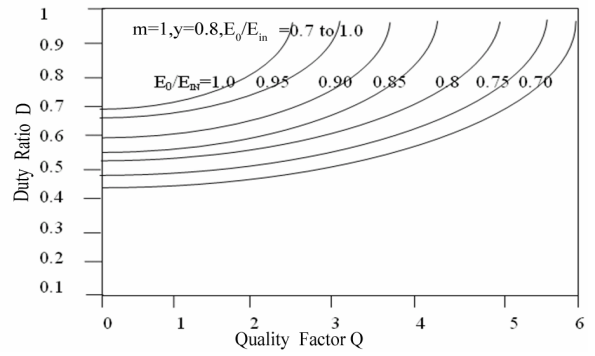

Figure 10. Variation of duty ratio versus quality factor with m = 1, y = 0.80.

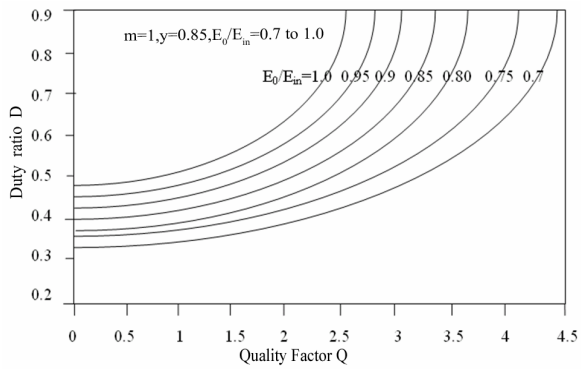

Figure 11. Variation of duty ratio versus quality factor with m = 1, y = 0.85.

0.85 and 0.9 respectively**.** Figure 13,14,15,16 show the effect of increased capacitance ratio of 2. From these graph, it is observed that as the value of yield stress changes from 0.85 to 0.9, the range of Q becomes narrower with increasing of Eo/Ein, (0.7 to 1.0). Also, at light load (Q is small), when Eo/Ein increases, the duty ratio increases while the spread of duty ratio decreases. Similarly, it becomes narrower and shifts to smaller values of duty ratio D as yield stress increases.

4.4. Variation of Duty Ratio vs. Q for m=2

Figure 13 to Figure 16 show how the duty ratio D varies as Q changes, to keep output load voltage constant at particular value. These curves are obtained by solving Equation 15 numerically for duty ratio as a function of Q for various values of converter gain Eo/Ein (for 0.7 to 1.0) and various switching frequency (yield stress = 0.7 to 0.9).

It is observed that as the Eo/Ein decreases, the duty ratio versus Q curves shifts downwards. The increase in value of yield stress results in shrinkage of D vs. Q Curve ranges. However when Cs/Cp ratio is observed that the above two characteristics are intensified. The detailed analysis offers each figure is given in the following paragraphs.

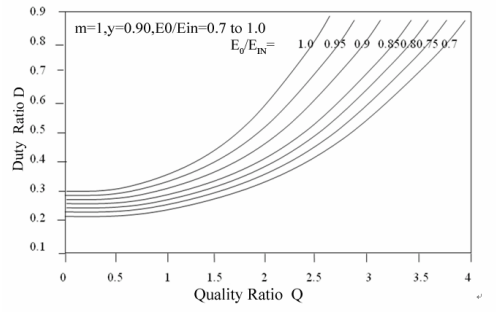

Figure 12. Variation of duty ratio versus quality factor with m = 1, y = 0.9.

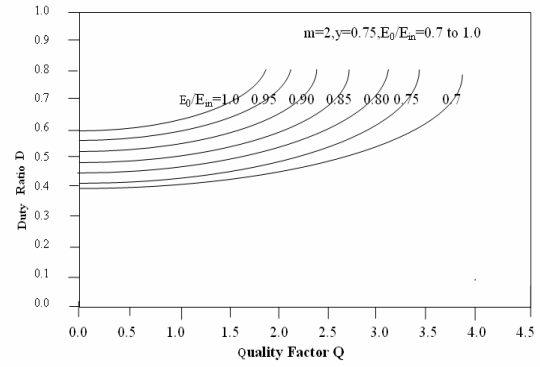

Figure 13. Variation of duty ratio versus quality factor with m = 2, y = 0.75.

If the normalized frequency is further increased, the graphs show similar pattern as described above. Figure 13, Figure 14, 15 and 16 show the effect of increased capacitance ratio of 2. From these graph, it is observed that as the value of yield stress changes from 0.85 to 0.9, the range of Q becomes narrower with increasing of Eo/Ein, (0.7 to 1.0). Also, at light load (Q is small), when Eo/Ein increases, the duty ratio increases while the spread of duty ratio decreases. Similarly, it becomes narrower and shifts to smaller values of duty ratio D as yield stress increases.

5. Design of Series Parallel Resonant Converter

Following criteria has been taken into account in order to obtain optimum design of series - parallel resonant converters.

1) Normalized switching frequency `y', such that maintains the lagging power factor conditions.

2) Minimum inverter output peak current for small rating and losses.

3) Minimum stress in series & parallel capacitor.

4) Minimum variation of Duty ratio from full load to no load i.e. good voltage regulation.

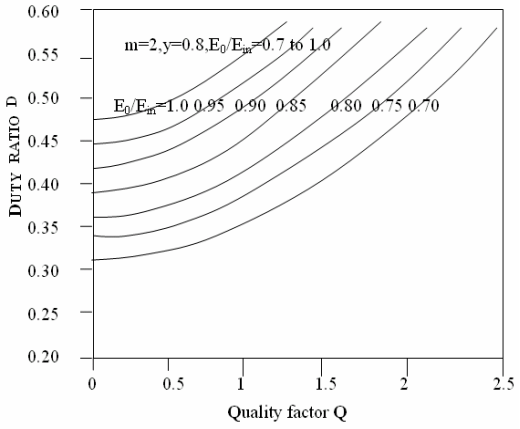

Figure 14. Variation of duty ratio versus quality factor with m = 2, y = 0.80.

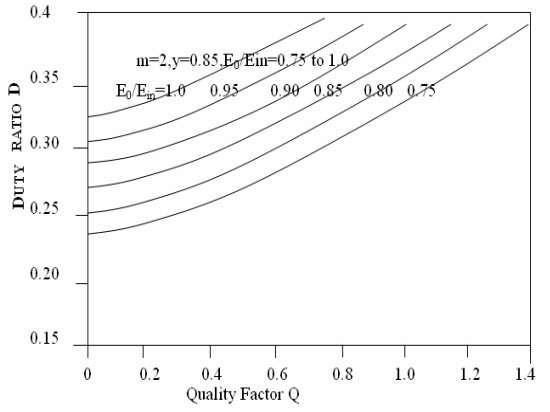

Figure 15. Variation of duty ratio versus quality factor with m = 2,y = 0.85.5.Design of series parallel resonant converter.

5.1. Selection of Cs/Cp (m)

It is observed from Figure 10 and Figure 14 that as m increases, the variation in the duty ratio required to keep the output constant decreases. For regulation of output voltage, the duty ratio has to be varied over larger range for m = 1.compared to m = 2. The effect of m on equivalent input impedance of the resonant network should be considered

while taking the values of m. From Equation (19) which is used to plot the variation of equivalent input impedance Zeqpu with the variation on normalized switching frequency and is shown in Figure 6. From the equation it is observed that as m increases from 1 to 2 the equivalent input impedances Zeqpu of resonant network decrease. This result in increased peak current through various components and consequently increased power loss. So from these considerations, the value of m = 1 should be taken.

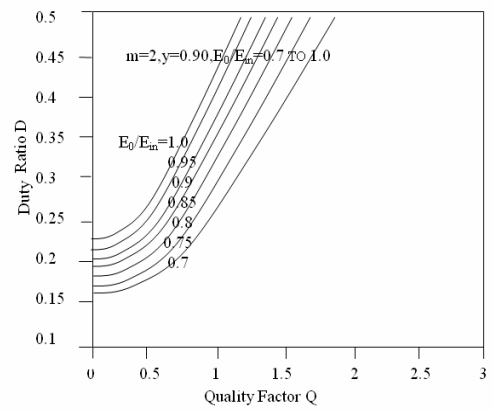

Figure 16. Variation of duty ratio versus quality factor with m = 2, y = 0.90.

5.2. Selection of Normalized Switching Frequency

The output voltage is regulated at all load by proper selection of y. In Figure 10 for y = 0.75 the output voltage can be regulated at Eo/Ein = 0.8 for the variation in Q up to 6. But at y =0. 8, the output voltage can be maintained at this value of only up to Q = 5 (Figure 11). As y increases further, the range of Q up to which the converter can be regulated decreases. This implies that too high value of y cannot be chosen especially when wide load variations are expected. Besides, y should not be of low value. Otherwise operation above resonance may not possible. Keeping these two factors in mind, y = 0.8 have been chosen. It can be seen from figure 10 that for variation in Q up to 5, Eo/Ein =0.8 can be maintained. As shown in Figure 7, for y =0.8, the input impedance angle changes from positive to negative as the values of Q is changed from 5 corresponding to full load to 1 for light load. This means that near full load, the converter operates above resonance and at partial loads the converter operates below resonance.

5.3. Selection of Tank Circuit Q at Full Load

Size of tank depends upon the value of quality factor Q and it should not be large. Equation (19), Equation (20), Equation (21), Equation (22) and Equation (30) show that peak inductor current is a function of Q and y. Figure 8 shows that peak inductor current increases with increase in Q, since the output voltage decreases for the same output power. But for a given value of y, it can be seen that the peak inductor current decreases as load current increases with increase in value of Q. However this decrease is not drastic for values of Q greater than 5. A compromised value of Q = 5 is chosen in this design.

5.4. Selection of Normalized Converter Gain

It is clear from the circuit topology that output current is

rectified and averaged tank current reflected to the secondary side of the transformer. Since the tank current is directly related to the output current, therefore we should choose a large conversion ratio, so that the turns ratio is minimized, resulting in the smallest possible tank current on the primary for a specified output current on the secondary. Hence the conversion ratio should be chosen close to one. Based on above consideration, the following optimum values are selected in the design of the converter.
Normalized frequency y = 0.8.
Cs/Cp ratio m = 1
Q of tank circuit at full load = 5

6. Design

Input voltage E_{in} = 50 volts. Output voltage E_o =40 volts. Output Current = 1.2 Amps. Switching frequency = 100 kHz

From the performance characteristics, the following values are considered for design.m=C_s/C_p = 1, Q=5, y=1.1
Load resistance R=V_0/I_0=32Ω

$$R = \frac{\omega_0 L}{Q} = \frac{1}{Q} \times \sqrt{\frac{L}{C}}$$

$$\sqrt{\frac{L}{C}} = Q \times R = 5 \times 32 = 160$$

Resonant frequency f_o is given by $f_o = f/y$ = 100,000/1.1 = 90.9 kHz
But

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$\frac{1}{\sqrt{LC}} = 2\pi \times 90.9 \times 10^3$$

The values of L & C are L = 280μH and C = 0.01 μ F.

7. Experimental Results

This section aims to validate the concepts developed in the previous sections. This section is intended to highlight the compliance of the proposed converter with the desired design specifications. Some testing results are presented in this section to verify the theoretical predictions of previous sections. An experimental proto type has been implemented for a resistive load as shown in Figure 17. The load rating is 40V, 50W, 1.2A. The resonant inductor is 0.28mH and the inductor is wound around ferrite core and the series resonant capacitor is 0.01μF and the capacitor used is of polypropylene film type.

The switching frequency is 100 KHz. All the four switches used is of IRF450 with an external fast recovery diode BYE26E connected across each switching device. In the secondary side, the diodes used for rectification are FR306. The filter inductor is 40μH and is wound around ferrite core. The filter capacitance is 100μF, 63V and the capacitor used is of electrolytic type. Figure 16 to Figure 18 shows the experimental output obtained. In each Figure, (a) shows the voltage across the series inductor and (b) shows the output voltage across the load after connecting the filter elements.

Table 3 efficiency obtained with conventional method (without LC) for variable I/P D-C supply voltage and switching frequency = 100 kHz

Table 4 efficiency obtained for series parallel resonant converter (proposed method) for I/P D-C supply voltage = 30 V and switching frequency = 100 kHz.

Table 1&2 give the Comparison of Results between Calculated and experimental results respectively of Series parallel resonant converter for an input DC supply voltage of 50V and switching frequency of 100 kHz**.**

Table 1. Calculated results.

Load %	Duty Ratio D	Series capacitor voltage Vcs(peak) volts	Series inductor voltage V_{LS}(peak) volts	Output current I_0 amps	Output voltage V_0 volts	Ripple Factor without filter %	Ripple Factor with filter %
100	0.8	385.4	468.9	1.2	40	18.1	0.0048
80	0.71	318.5	394.2	0.96	40	17.5	0.0034
60	0.64	245.6	325.6	0.72	40	16.6	0.0029
40	0.57	158.6	247.2	0.48	40	15.3	0.0016
20	0.49	73.1	143.4	0.24	40	14.9	0.0007
10	0.42	46.5	86.9	0.12	40	13.6	0.0001

Table 2. Experimental results.

Load %	Duty Ratio D	Series capacitor voltage Vcs(peak) volts	Series inductor voltage V_{LS}(peak) volts	Output current I_0 amps	Output voltage V_0 volts	Ripple Factor without filter %	Ripple Factor with filter %
100	0.8	398.8	487.4	1.2	40	20.2	0.0051
80	0.7	335.6	418.5	0.96	40	19.4	0.0042
60	0.62	268.4	345.9	0.72	40	18.5	0.0035
40	0.54	185.9	265.2	0.48	40	17.3	0.0028
20	0.45	105.1	168.4	0.24	40	16.9	0.0017
10	0.39	70.6	96.4	0.12	40	15.6	0.0009

Table 3. Experimental results.

Duty Ratio	Input Current (amps)	Input Voltage (volts)	Output Current (amps)	Output Voltage (volts)	Efficiency %
0.7	1.41	50	1.2	55.9	95.56
0.7	1.19	50	1.0	56.3	94.51
0.7	0.98	50	0.8	57.6	93.44
0.7	0.76	50	0.6	58.9	92.78
0.7	0.53	50	0.4	61.2	91.96
0.7	0.27	50	0.2	62.9	91.19

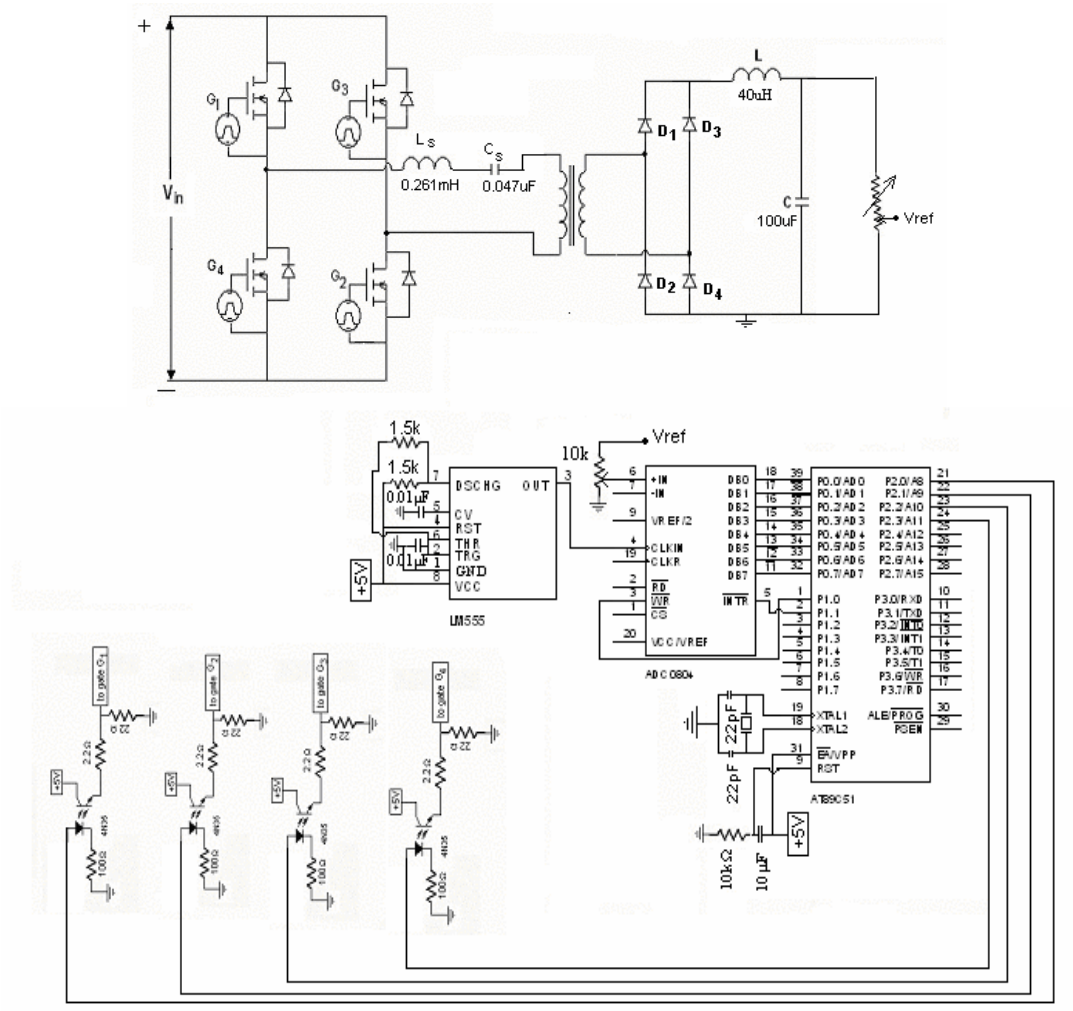

Figure 17. Experimental circuit.

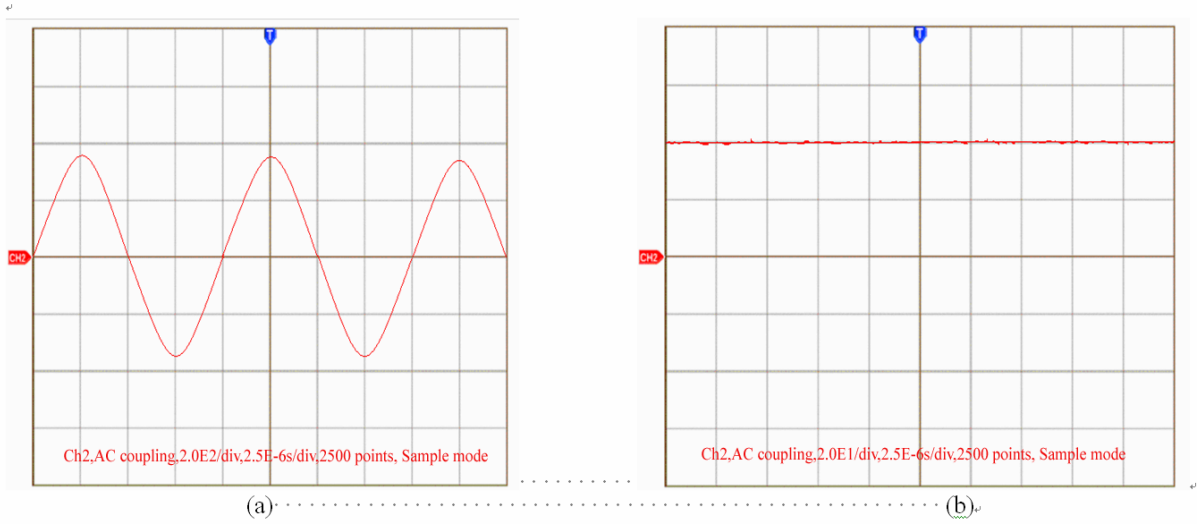

Figure 18. Experimental results for series parallel resonant converter at 60% load with m=1: (a) V_{LS}, (b) V_0 with filter.

Table 4. Experimental results.

Duty Ratio	Input Current (amps)	Input Voltage (volts)	Output Current (amps)	Output Voltage (volts)	Efficiency %
0.7	1.29	50	1.2	48.2	89.53
0.7	1.08	50	1.0	48.3	88.76
0.7	0.88	50	0.8	48.4	87.62
0.7	0.67	50	0.6	48.5	86.48
0.7	0.45	50	0.4	48.6	85.49
0.7	0.23	50	0.2	48.8	84.32

8. Conclusions

This paper presents a new front-end dc–dc power supply based on the series parallel resonant converter. A detailed design procedure has been given to select the values of the resonant components for a design case. Experimental results show that the proposed converter enjoys a high efficiency. It can be concluded from the experimental output that the variation of the working efficiency with output load power for different duty ratio is in direct proportion with the load.

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