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Performance Analysis of a Boost Converter with Components Losses

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Abstract

A theoretical study of a conventional boost converter is presented. Based on the real behavior of the components, two models of the boost converter are introduced: one dealing only with losses through inductor and capacitor and another taking into account switching losses in addition to resistive ones. From these two models, the detailed analytical expressions of both voltage gain factor and conversion efficiency are established taking into account the losses through parasitic resistances and switching losses. The behavior of the converter is then analyzed for each model by simulation for the voltage gain factor and the conversion efficiency.

Keywords

Boost, Gain Factor, Efficiency, ESR

1. Introduction

Actually, the demand for clean energy sources is actively growing leading to the development of new or alternative energy technologies. These alternative energy technologies are essentially the renewable ones. The most promising renewable energy sources are wind energy, photovoltaic (PV) cells, and fuel cells (FC) [1] [2] [3]. However, renewable energy sources have low output voltage characteristics. So, due to this low voltage generation associated to generally high input current requirement, a high step-up DC-DC converter with high efficiency is needed to convert the low DC input to the required voltage, current, and frequency. This is particularly true in the case where a microinverter [4]-[9] is provided to each PV module of solar PV systems. Such a microinverter has generally two stages; the first stage uses the high step-up DC-DC converter to meet the voltage demand of the second stage and also act as a maximum power point

tracker in order to get maximum power from the PV module. The second stage is a DC to AC inverter to meet the load demand.

Many high step-up DC-DC converters have been designed [10] [11] [12] [13] [14] with advantages and disadvantages but all of them derive from the conventional boost converter [15]-[20].

The conventional boost converter has many disadvantages like high voltage stress across the switching device and reverse recovery problem of output diode. It is also well know that its performance is limited due to higher on state resistance leading to more conduction losses in the switch, losses in the inductor series resistance and the ESR of the output capacitor [21] [22] [23] [24].

These disadvantages are the major limitation of the use of that type of converter. Many works [25] [26] [27] [28] have been carried out dealing with loss models or loss calculation platforms in order to analyze and optimize the power converters before using them into real operation. Some of them use only conduction loss, missing the switching loss and core loss, which take a large part in the high frequency system losses. Some others took into account switching loss and core loss. A third category used mixed loss model that are able to synthetically and analytically calculate and analyze the component losses and system losses as functions of voltages, power, switching frequency, operating temperature of the heatsink on the semiconductors and so on. Unfortunately, these studies were not carried out on the basic boost converter but on some, more sophisticated structure [28] [29]. Even for studies conducted on boost converter, the inductor loss is calculated in number of turn associated to core loss with magnetic effects [30] [31] [32] but not directly versus inductor parasitic resistance. Thus, it is important to know exactly how resistive losses and switching losses affect the performance of the converter and what is the contribution of both resistive and switching losses relative to each other and compared to the total losses in the converter. That is the aim of this present study. Based on two loss models of the boost converter, this study will present a detailed mathematical formulation of the voltage gain factor and the conversion efficiency for a conventional boost converter. Simulations are then performed in order to exhibit the effects of the different losses but also to quantify these losses compared to the ideal model.

2. Modeling of the Converter and Mathematical Formulation

The studied converter is presented in **Figure 1**; assuming that all components are ideal and the converter is operating in Continuous Conduction Mode (CCM) [33] as this operating mode is more suited for photovoltaic applications, the basic equations are as follows [34]:

$$v_L = L\frac{\mathrm{d}i_L}{\mathrm{d}t} = \begin{cases} V_{in} & 0 < t < \alpha T \\ V_{in} - V_0 & \alpha T < t < T \end{cases} \tag{1}$$

$$V_0 = \frac{V_{in}}{(1-\alpha)} \tag{2}$$

with α being the steady state duty cycle and T the switching period.

When taking into account resistive losses through inductor and capacitor, the boost converter can be presented as shown in Figure 2 and the power balance is written as:

$$P_I = P_0 + P_{r_L} + P_{r_C} \tag{3}$$

P_I, P_O, P_{r_L}, P_{r_C} are respectively the input power, the output power, the power losses through the inductor series resistance r_L and the power losses through the capacitor series resistance r_C. Expressing the different terms in Equation (3), see **Appendix**, Equation (3) can be rewritten in the form:

$$V_{in} * \frac{V_0}{(1-\alpha)} = V_0 * \frac{V_0}{R} + r_L * \frac{V_0^2}{(1-\alpha)^2 R^2} + r_C * \frac{\alpha V_0^2}{(1-\alpha)^2 R^2} \tag{4}$$

R is the load resistor.

We can then derive the gain factor G as:

$$G = \frac{(1-\alpha)R}{(1-\alpha)R^2 + r_L + r_C\alpha(1-\alpha)} \tag{5}$$

The conversion efficiency η is defined by:

$$\eta = \frac{P_0}{P_0 + P_{r_L} + P_{r_C}} \tag{6}$$

Replacing P_O, P_{r_L}, P_{r_C} by their respective expressions, the conversion efficiency becomes:

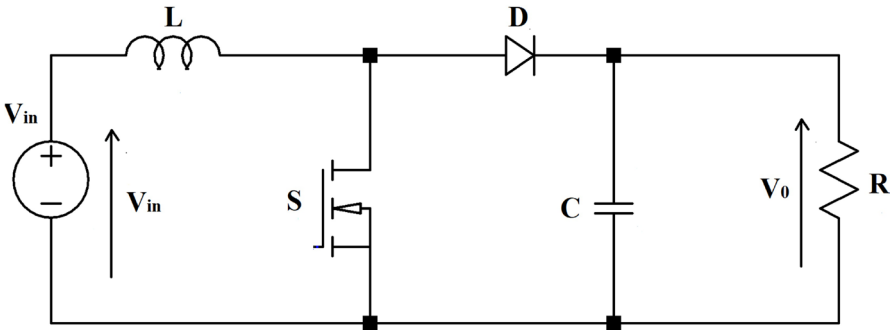

Figure 1. Ideal model of the boost converter.

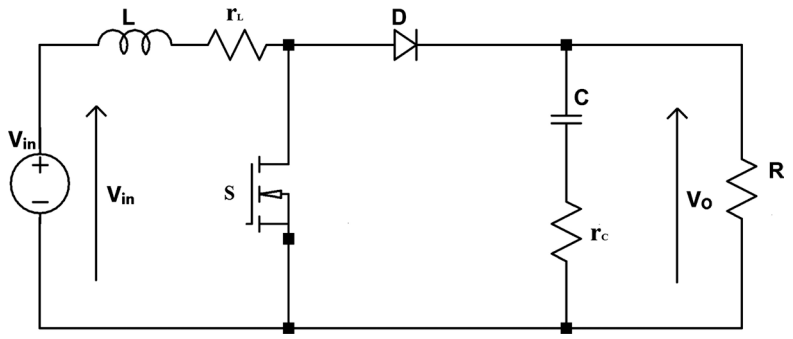

Figure 2. Boost converter with series losses through inductor and capacitor (model 1).

$$\eta = \frac{1}{1 + \dfrac{r_L + r_C \alpha (1-\alpha)}{R(1-\alpha)^2}} \tag{7}$$

The model presented above (model 1) did not take into account the switching losses through active components (the Mosfet T and the diode D). The following model of the converter (Figure 3, model 2) do take into account these losses.

The power balance for the converter is:

$$P_I = P_0 + P_{r_L} + P_{r_C} + P_{FET} + P_D \tag{8}$$

P_{FET}, P_D are respectively the power losses though the switch T and the diode D.

After some mathematical manipulations, we obtain (see **Appendix**):

$$\begin{aligned} V_{in} * \frac{V_0}{(1-\alpha)} = V_0 * \frac{V_0}{R} + r_L * \frac{V_0^2}{(1-\alpha)^2 R^2} + r_C * \frac{\alpha V_0^2}{(1-\alpha) R^2} \\ + \frac{\alpha r_{DS} V_0^2}{(1-\alpha) R^2} + \frac{1}{2} f_S C_0 V_0^2 + \frac{R_F V_0^2}{(1-\alpha) R^2} + \frac{V_F V_0}{R} \end{aligned} \tag{9}$$

f_S, r_{DSon}, C_O are respectively the transistor switching frequency, on resistance and output capacitance; r_F and V_F are the diode dynamic resistance and forward voltage.

The voltage gain factor G is then deduced as:

$$G = \frac{(1-\alpha) R}{(1-\alpha) R^2 + r_L + r_C \alpha (1-\alpha) + \alpha r_{DS} + \dfrac{1}{2} f_S C_0 (1-\alpha)^2 R^2 + \dfrac{V_F}{V_0} (1-\alpha)^2 R + R_F (1-\alpha)} \tag{10}$$

For the conversion efficiency, we have:

$$\eta = \frac{P_0}{P_0 + P_{r_L} + P_{r_C} + P_{FET} + P_D} \tag{11}$$

This leads to:

$$\eta = \frac{1}{1 + \dfrac{r_L + \alpha r_{DS}}{R(1-\alpha)^2} + \dfrac{R_F + r_C \alpha}{R(1-\alpha)^2} + \dfrac{V_F}{V_0} + \dfrac{1}{2} f_S C_0 R} \tag{12}$$

3. Results and Discussions

Based on the above mathematical formulation, simulations were performed by

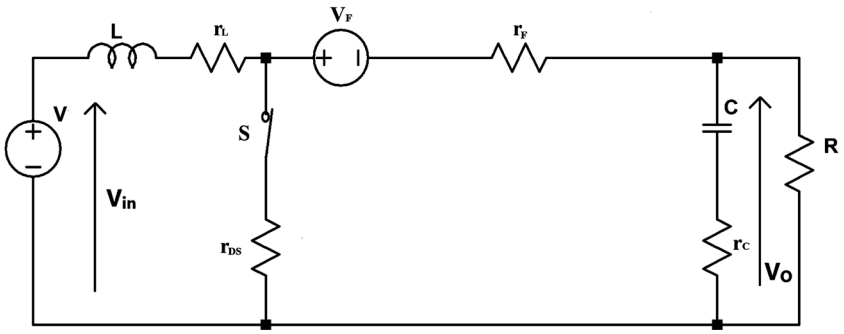

Figure 3. Boost converter with series losses and switching losses (model 2).

varying duty cycle, series resistances, and choosing different transistors and diodes parameters. This is done for the two models and the effects of the series resistances are pointed out, as well as transistor and diode losses.

3.1. Voltage Gain Factor

Define We present in **Figure 4** the voltage gain factor G versus duty cycle α for various inductor series resistance r_L considering small capacitor series resistance r_C (**Figure 4(a)**) and then larger r_C (**Figure 4(b)**).

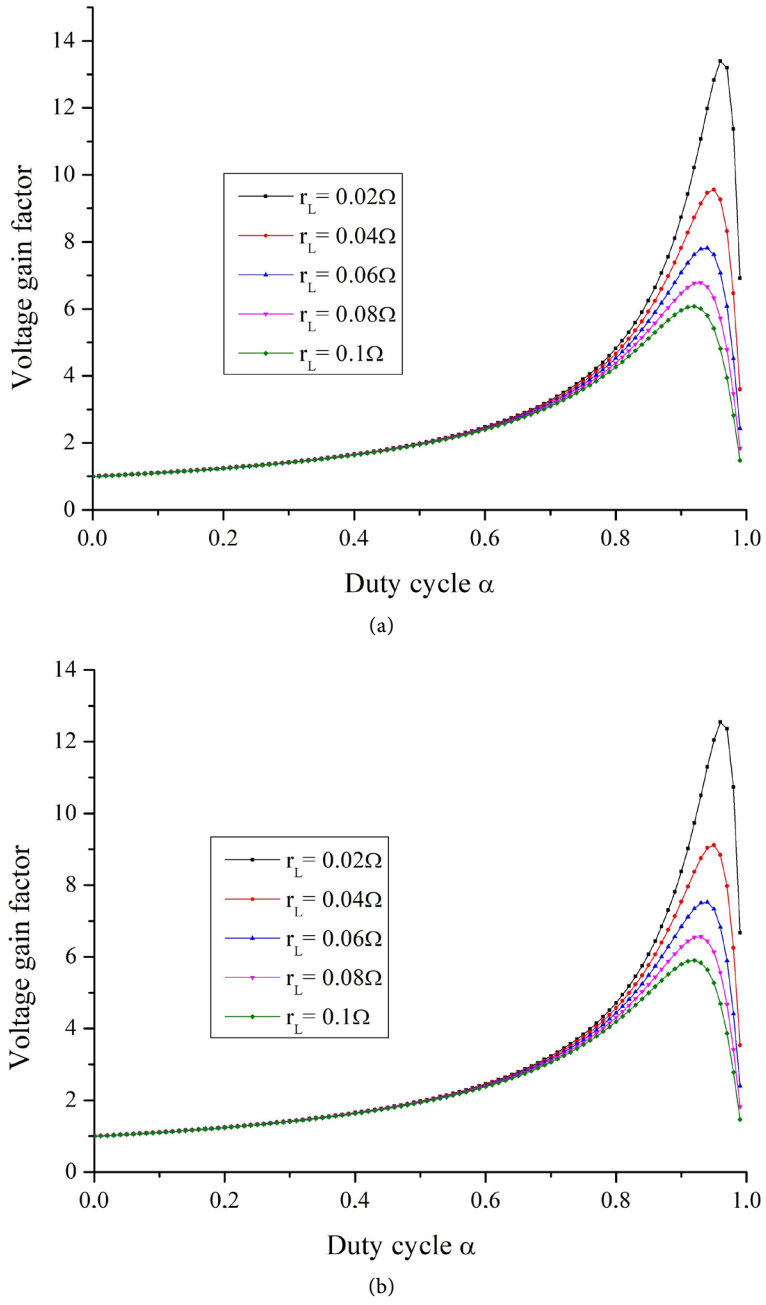

Figure 4. Voltage gain factor versus duty cycle for various inductor's series resistance values. (a) $r_C = 0.02\ \Omega$; (b) $r_C = 0.1\ \Omega$.

These figures show that voltage gain factor first increase until a certain duty cycle α_0 value from which it began decreasing. In fact, when the duty cycle is increasing the losses in the series resistance of the inductor also increase to a threshold from which the losses are so important that the voltage gain factor begin decreasing for duty cycle approaching unity. We can see that this threshold depend directly on the series resistance value r_L. For low r_L the threshold is reached very close to duty cycle equal to unity but for increasing r_L the threshold is reached far from duty cycle equal to unity. This means that the maximum voltage gain factor (corresponding to a duty cycle α_0) is shifted left as r_L increases. As losses in the inductor increase, the voltage gain factor decrease very rapidly. This means that in practical design the value of r_L must be absolutely know otherwise the output voltage could not be guaranteed. **Figure 4(a)** & **Figure 4(b)** also show that, regarding the voltage gain factor, there is no significant differences between low r_C values and high r_C values.

We plotted in **Figure 5** the voltage gain factor G versus duty cycle α for various r_C considering small r_L (**Figure 5(a)**) and larger r_L (**Figure 5(b)**).

These two figures illustrate very well the above situation; for low r_L value as for high r_L value, the effect of the capacitor series resistance is very negligible on the voltage gain factor. That is, the effect of the capacitor series resistance could be neglected in a first approach in a practical design contrary to the inductor series resistance.

Taking into account inductor's series resistance could lead up to about 54% lower value of the voltage gain factor than that of ideal calculation ($r_L = 0$); for the case of r_C, the gain factor is only up to about 8% lower than ideal calculation ($r_C = 0$). If the output voltage ripple must be kept as low as possible, then the capacitor resistance should be very low, typically about 10 mΩ (example for X5R/X7R capacitors). Given that inductor losses also depend on operating frequency the selected inductor must have high quality factor value, typically before quality turning point.

The effect of the output diode is related to its forward voltage V_F; this forward voltage has to be as low as possible with also a low dynamic resistance value. This goal can be reached by choosing an appropriate Schottky diode.

For a given operating frequency and a set of inductor, capacitor and diode, the voltage gain factor only depend on the switching transistor characteristics.

Figure 6 illustrates the importance of the transistor intrinsic parameters on the voltage gain.

We can see that the major problem comes from the r_{DSon} resistance value for a given operating frequency: the r_{DSon} value dictate the choice of the switching transistor when power-rating conditions are satisfied. It can also be noted that the quality of inductor plays a role only when r_{DSon} is low (nearly 50% decrease for a poor quality inductor); indeed, for higher r_{DSon} values the losses in the transistor prevail on those from the inductor. When r_{DSon} decrease, the losses through the transistor become negligible and the inductor losses prevail.

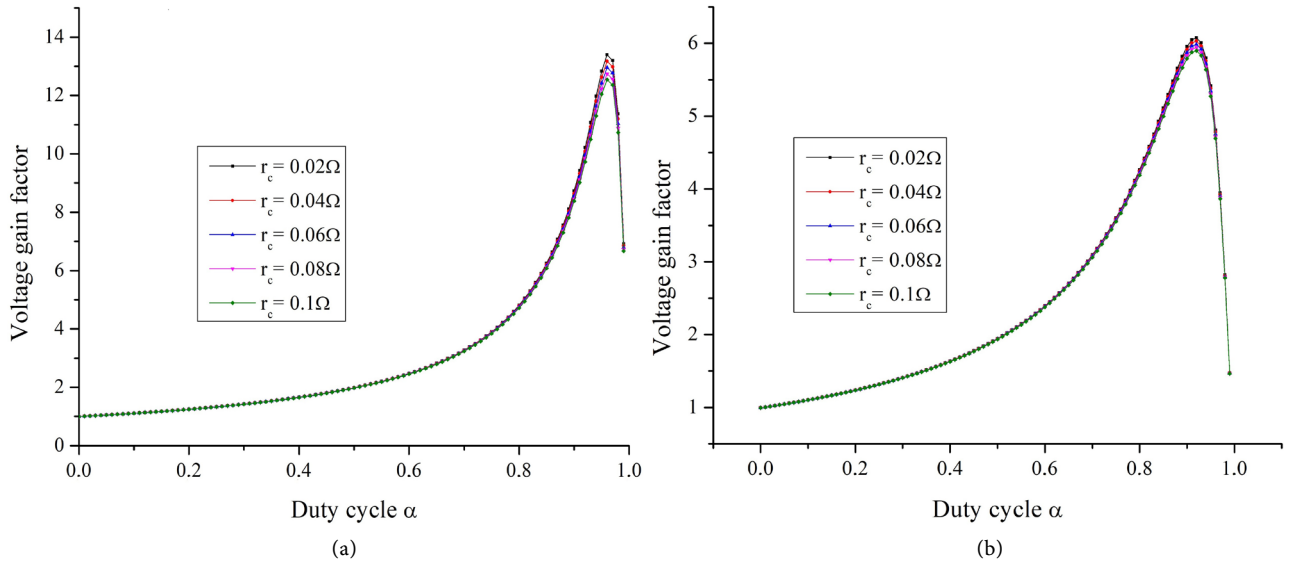

Figure 5. Voltage gain factor versus duty cycle for various capacitor's series resistance values. (a) $r_L = 0.02\ \Omega$; (b) $r_L = 0.1\ \Omega$.

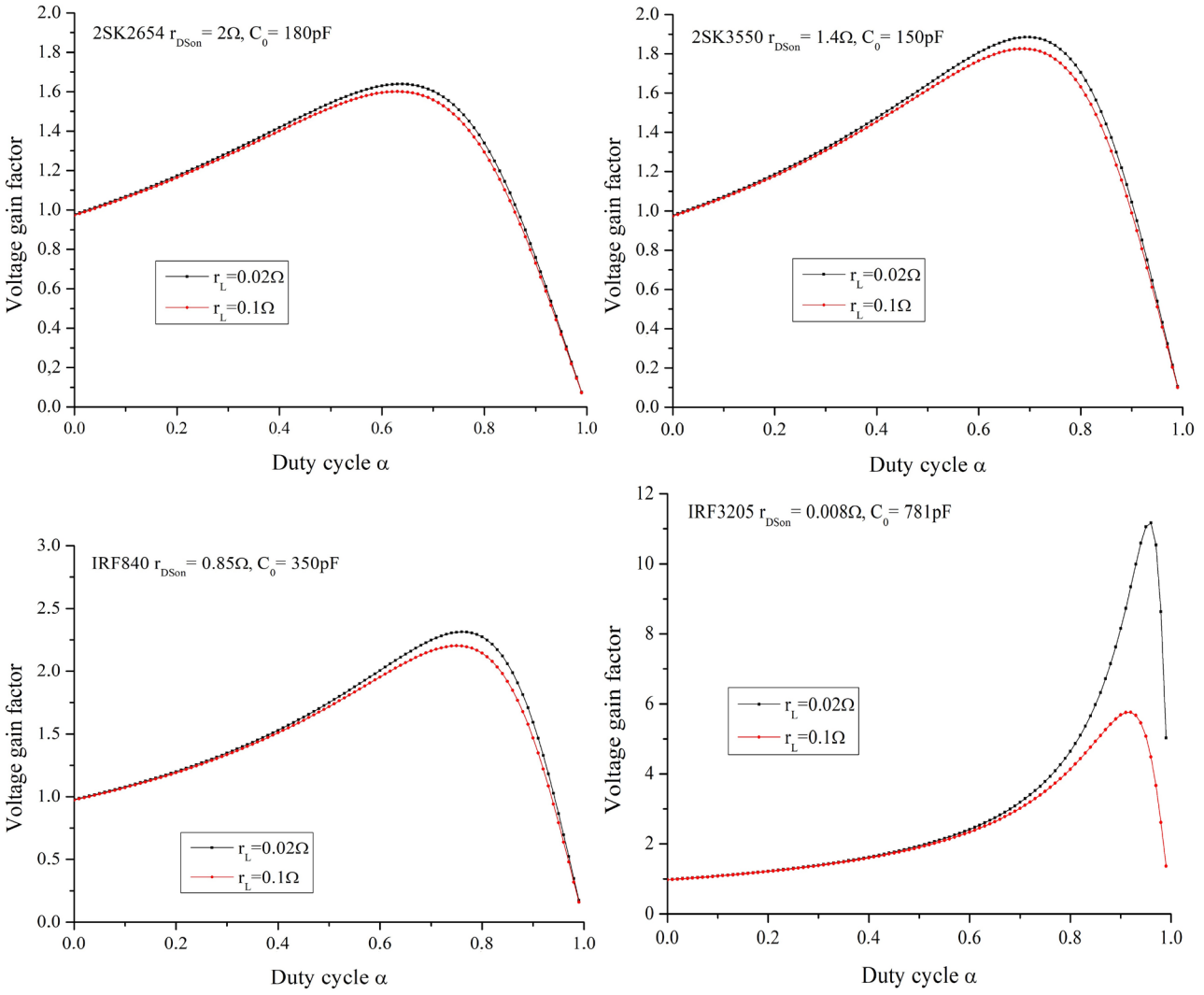

Figure 6. Voltage gain factor versus duty cycle for transistors: 2SK2654, 2SK3550, IRF840 and IRF3205.

3.2. Conversion Efficiency

Figure 6 shows the conversion efficiency profile versus duty cycle for various r_L values considering small r_C (Figure 6(a)) and larger r_C (Figure 6(b)).

This figure shows that as the duty cycle increases, the conversion decrease and this decrease is very marked for duty cycles close to unity if the series resistance r_L of the inductor is small. When r_L is high, the losses in the inductor prevail as duty cycle increase leading to the observed decrease of the conversion efficiency.

It can be noted that the effect of r_L is very important for both low and high capacitor's series resistance. Taking into account r_L could lead to an efficiency difference up to about 40% compared to unity (ideal conversion efficiency).

In Figure 8 the Conversion efficiency profile is presented versus duty cycle for various r_C values considering small r_L (Figure 8(a)) and larger r_L (Figure 8(b)).

As observed before (Figure 5), we can see in Figure 8 that the effect of the series resistance of the capacitor is smaller than that of the series resistance of the inductor.

With both Figure 7 and Figure 8, we can see that it is recommended to not operate at duty cycles more than 0.8 as series resistances effect are more marked in that area. In fact operating with duty cycle close to unity increase the semiconductor stress and then decrease markedly the lifetime of the converter.

We now present in Figure 9 the conversion efficiency versus duty cycle for different transistors to illustrate transistor characteristics effect on the conversion efficiency for a given operating frequency and a set of inductor, capacitor and diode.

Figure 9 shows that r_{DSon} is a very important parameter as noted before in Figure 6; for high r_{DSon} the conversion efficiency decrease very markedly as the duty cycle increase. This decrease can reach 20% or more in the conversion efficiency depending on the operating duty cycle. This point out the importance of

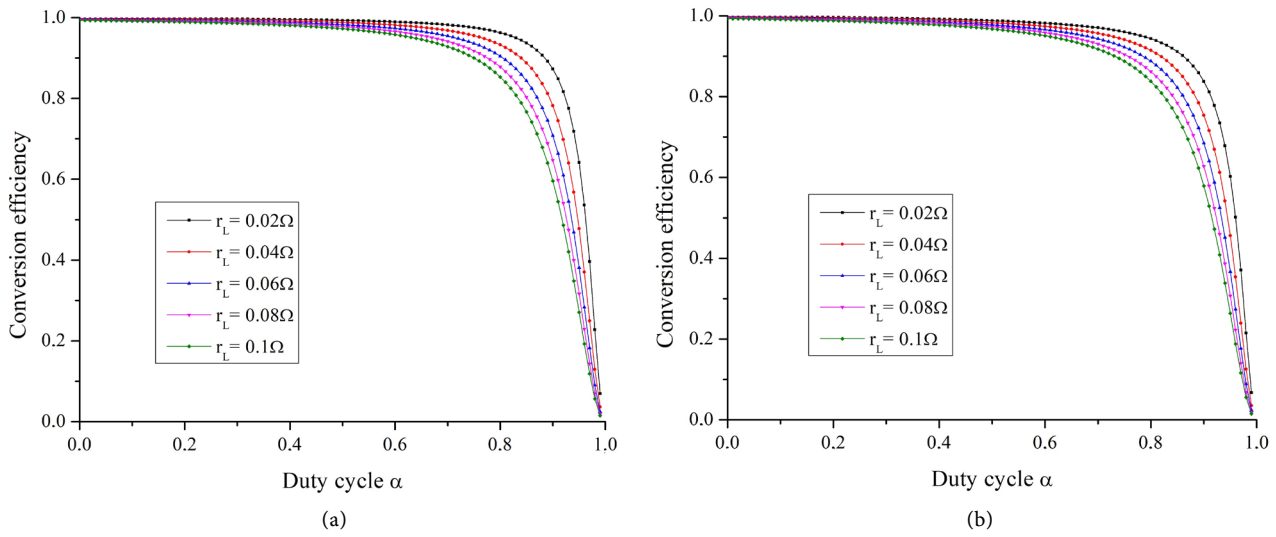

Figure 7. Conversion efficiency versus duty cycle for various inductor's series resistance values. (a) r_C = 0.02 Ω; (b) r_C = 0.1 Ω.

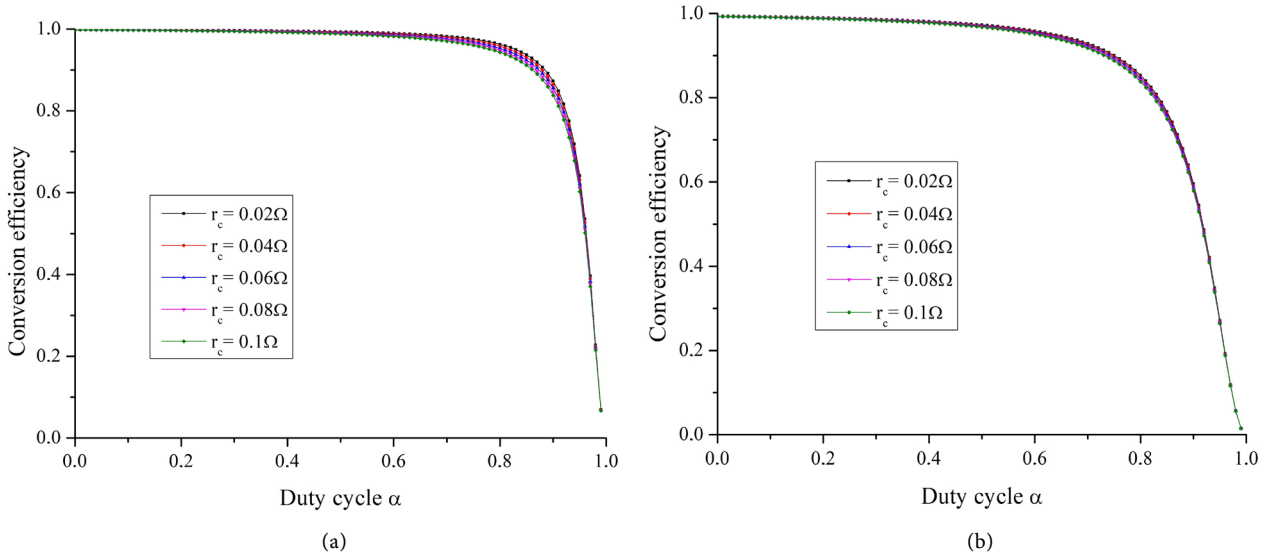

Figure 8. Conversion efficiency versus duty cycle for various capacitor's series resistance values. (a) r_L = 0.02 Ω; (b) r_L = 0.1 Ω.

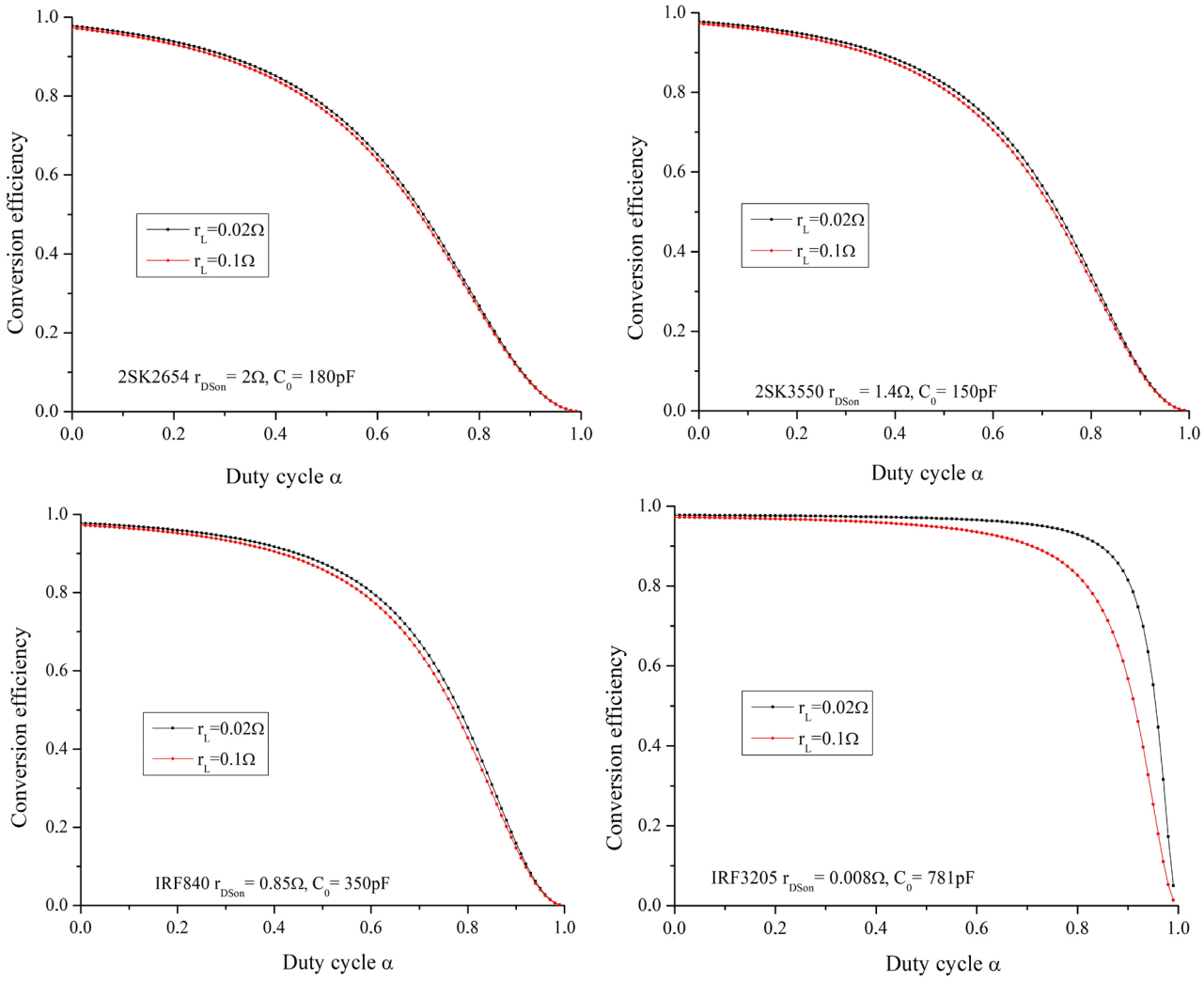

Figure 9. Voltage gain factor versus duty cycle for transistors: 2SK2654, 2SK3550, IRF840 and IRF3205.

the choice of the switching transistor. The good transistor should then have and r_{DSon} value as low as possible and in that case inductor losses are the main source of losses. The capacitance of the transistor is also a limiting factor at high frequencies.

4. Conclusions

We have presented in this paper a detailed theoretical study of a conventional boost converter. We have taken into account the real behavior of the passive and active component of the boost converter and we analyzed its voltage gain factor and conversion efficiency. It has been showed that inductor series resistance and transistor r_{DSon} resistance play the most important role leading to a decrease to up to 50% in the voltage gain factor. We also showed that it is not recommended to use duty cycle close to unity because losses effects are most important there with a markedly decrease of both voltage gain factor and conversion efficiency.

The effect of the capacitor series resistance is negligible for the voltage gain factor (less than 8%) and conversion efficiency; however, the designer must keep in mind that the series resistance of the capacitor directly affect the output ripple voltage and the control loop stability. The last parameter is the switching transistor r_{DSon} that must be as low as possible as the conversion efficiency of the converter will decrease markedly as duty cycle increase (up to 20%).

Despite its low voltage gain factor, a well-designed conventional boost converter can reach the fixed goal with the advantage of a simpler control loop leading to a cost effective and more robust design.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

References

[1] Kesraoui, M., Korichi, N. and Belkadi, A. (2011) Maximum Power Point Tracker of Wind Energy Conversion System. *Renew Energy*, **36**, 2655-2662. https://doi.org/10.1016/j.renene.2010.04.028

[2] Shuhui, L., Timothy, A.H., Dawen, L. and Fei, H. (2011) Integrating Photovoltaic and Power Converter Characteristics for energy Extraction Study of Solar PV Systems. *Renew Energy*, **36**, 3238-3245. https://doi.org/10.1016/j.renene.2011.02.016

[3] Renewables (2017) Global Status Report, REN21.

[4] Wang, T. and Tang, Y. (2013) A High Step-Up Voltage Gain DC/DC Converter for the Micro-Inverter. *IEEE 8th Conference on Industrial Electronics and Applications* (*ICIEA*), Melbourne, 19-21 June 2013, 1089-1094.

[5] Ternifi, Z.E.T., Petit, P., Bachir, G. and Aillerie, M. (2017) New Topology of Photovoltaic Microinverter Based on Boost Converter. *Energy Procedia*, **119**, 938-944. https://doi.org/10.1016/j.egypro.2017.07.106

[6] Variath, R.C., Andersen, M.A.E., Nielsen, O.N. and Hyldgard, A. (2010) A Review of Module Inverter Topologies Suitable for Photovoltaic Systems. 2010 *Conference*

Proceedings IPEC, Singapore, 27-29 October 2010, 310-316.

[7] Li, Q. and Wolfs, P. (2008) A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies with Three Different DC Link Configurations. *IEEE Transactions on Power Electronics*, **23**, 320-1333.

[8] Haibing, H., Qian, Z., Xiang, F., Shen, Z.J. and Batarseh, I. (2011) A Single Stage Micro-Inverter Based on a Three-Port Flyback with Power Decoupling Capability. *Energy Conversion Congress and Exposition* (*ECCE*), Phoenix, 17-22 September 2011, 1411-1416.

[9] Petreuş, D., Daraban, S., Ciocan, I., Patarau, T., Morel, C. and Machmoum, M. (2013) Low Cost Single Stage Micro-Inverter with MPPT for Grid Connected Applications. *Solar Energy*, **92**, 241-255. https://doi.org/10.1016/j.solener.2013.03.016

[10] Kazimierczuk, M.K. (2015) Pulse-Width Modulated DC-DC Power Converters. John Wiley and Sons, Hoboken.

[11] Li, W., Lv, X., Deng, Y., Liu, J. and He, X. (2009) A Review of Non-Isolated High Step-Up DC/DC Converters in Renewable Energy Applications. 2009 *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington DC, 15-19 February 2009, 364-369.

[12] Wu, G., Ruan, X. and Ye, Z. (2018) Non-Isolated High Step-Up DC-DC Converter Adopting Auxiliary Capacitor and Coupled Inductor. *Journal of Modern Power Systems and Clean Energy*, **6**, 384-398. https://doi.org/10.1007/s40565-017-0342-8

[13] Taghvaee, M.H., Radzi, M.A.M., Moosavain, S.M., Hizam, H. and Marhaban, M.H. (2013) A Current and Future Study on Non-Isolated DC-DC Converters for Photovoltaic Applications. *Renewable and Sustainable Energy Reviews*, **17**, 216-227. https://doi.org/10.1016/j.rser.2012.09.023

[14] Wu, K.C. (1997) Pulse Width Modulated DC-DC Converters. Springer, Berlin. https://doi.org/10.1007/978-1-4615-6021-0

[15] Ayop, R. and Tan, C.W. (2018) Design of Boost Converter Based on Maximum Power Point Resistance for Photovoltaic Applications. *Solar Energy*, **160**, 322-335. https://doi.org/10.1016/j.solener.2017.12.016

[16] Winder, S. (2017) Power Supplies for LED Driving. 2nd Edition, Newnes, Oxford and Boston.

[17] Dash, S.S. and Nayak, B. (2015) Control Analysis and Experimental Verification of a Practical DC-DC Boost Converter. *Journal of Electrical Systems and Information Technology*, **2**, 378-390. https://doi.org/10.1016/j.jesit.2015.08.001

[18] Abusorrah, A., Al-Hindawi, M.M., Al-Turki, Y., Mandal, K., Giaouris, D., Banerjee, S., Voutetakis, S. and Papadopoulou, S. (2013) Stability of a Boost Converter Fed from Photovoltaic Source. *Solar Energy*, **98**, 458-471. https://doi.org/10.1016/j.solener.2013.09.001

[19] Wu, K. (2016) Power Converters with Digital Filter Feedback Control. Academic Press, Cambridge.

[20] Sadek, U., Sarjaš, A., Svečko, R. and Chowdhury, A. (2015) FPGA-Based Control of a DC-DC Boost Converter. *IFAC-PapersOnLine*, **48**, 22-27. https://doi.org/10.1016/j.ifacol.2015.08.102

[21] Erickson, R.W. and Maksimovic, D. (2004) Fundamentals of Power Electronics. 2nd Edition, Kluwer Academic Publishers, New York.

[22] Das, M. and Agarwal, V. (2012) A Novel, High Efficiency, High Gain, Front end DC-DC Converter for Low Input Voltage Solar Photovoltaic Applications. 38*th Annual Conference of the IEEE Industrial Electronics Society*, Montreal, 25-28 Oc-

tober 2012, 5744-5749.

[23] Rajesh, R. and Mabel, M.C. (2015) A Comprehensive Review of Photovoltaic Systems. *Renewable and Sustainable Energy Reviews*, **51**, 231-248. https://doi.org/10.1016/j.rser.2015.06.006

[24] Mahela, O.P. and Shaik, A.G. (2017) Comprehensive Overview of Grid Interfaced Solar Photovoltaic Systems. *Renewable and Sustainable Energy Reviews*, **68**, 316-332. https://doi.org/10.1016/j.rser.2016.09.096

[25] Bae, J.Y., Kim, Y., Lee, D.H., Kwon, S.D., Kim P.S. and Han, D.H. (2004) A Study on the Loss Model and Characteristic Comparison of Three Level Converter and Full-Bridge Converter through the Conduction Loss Analysis of Power Devices. *IEEE IECON*, **3**, 2314-2320.

[26] Hayashi, Y., Takao, K., Shimizu, T. and Ohashi, H. (2007) Power Loss Design Platform for High Output Power Density Converters. *European Conference on Power Electronics and Applications*, Aalborg, 2-5 September 2007, 1-10.

[27] Deng, S., Mao, H., Wu, T., Xiao, S. and Batarseh, I. (2004) Power Losses Estimation Platform for Power Converters. *IEEE 19th Annual Applied Power Electronics Conference and Exposition*, Anaheim, 22-26 February 2004, Vol. 3, 1784-1789.

[28] Wang, Y., Haan, S. and Ferreira, J.A. (2008) Methods for Experimental Assessment of Component Losses to Validate the Converter Loss Model. *IEEE 13th International Power Electronics and Motion Control Conference*, Poznan, 1-3 September 2008, 187-194.

[29] Beldjajev, V., Roasto, I. and Zakis, J. (2013) Impact of Component Losses on the Efficiency of a New Quasi-Z-Source-Based Dual Active Bridge. *Doctoral Conference on Computing, Electrical and Industrial Systems*, Costa de Caparica, 15-17 April 2013, 485-492.

[30] Gadalla, B.S.A., Schaltz, E., Siwakoti, Y.P. and Blaabjerg, F. (2017) Analysis of Loss Distribution of Conventional Boost, Z-Source and Y-Source Converters for Wide Power and Voltage Range. *Transaction on Environment and Electrical Engineering*, **2**, 1-9. https://doi.org/10.22149/teee.v2i1.68

[31] Tsai, M.-Y., Liang, T.-J. and Lin, Y.-M. (2017) Loss Analysis and Optimized Design of DC-DC Converter for Battery Module. *IEEE 3rd International Future Energy Electronics Conference and ECCE Asia*, Kaohsiung, 3-7 Jun 2017, 692-697.

[32] Hinov, N., Arnaudov, D., Valchev, V. and Vuchev, S. (2017) Comparative Loss Analysis of Boost and Synchronous Boost DC-DC Converters. *International Scientific Conference Electronics*, Sozopol, 13-15 September 2017, 1-4.

[33] Durán, E., Andújar, J.M., Segura, F. and Barragán, A.J. (2011) A High-Flexibility DC Load for Fuel Cell and Solar Arrays Power Sources Based on DC-DC Converters. *Applied Energy*, **88**, 1690-1702. https://doi.org/10.1016/j.apenergy.2010.11.002

[34] Dokić, B.L. and Blanuša, B. (2015) Power Electronics: Converters and Regulators. 3rd Edition, Springer International Publishing, Berlin.

Appendix

When the switch S is on, we have:

$$v_L = V_{in} = L\frac{\mathrm{d}i_L}{\mathrm{d}t} \tag{A.1}$$

Integrating this equation give rise to the current flowing through the coil L:

$$i_L(t) = I_{Lm} + \frac{V_I}{L}t \tag{A.2}$$

with I_{Lm} being the minimum of i_L.

When T is off, the voltage across L can be written as:

$$v_L = V_I - V_0 = L\frac{\mathrm{d}i_L}{\mathrm{d}t} \tag{A.3}$$

This above equation give rise to i_L in the form:

$$i_L(t) = I_{LM} + \frac{V_I - V_0}{L}t \tag{A.4}$$

with now I_{LM} being the maximum of i_L.

I_{LM} and I_{Lm} are reached respectively at the switching on and off of S and are related by:

$$I_{Lm} = I_{LM} + \frac{V_I - V_0}{L}(T - \tau)$$

$$I_{LM} = I_{Lm} + \frac{V_I}{L}\tau$$

with T being the switching period, α the duty cycle and $\tau = \alpha T$. Combining these two equations, we obtain the output voltage V_0 as (2):

$$V_0 = \frac{V_{in}}{(1-\alpha)}$$

The power dissipated through r_L is:

$$P_{r_L} = r_L + I_{ISR}^2 \tag{A.5}$$

with

$$I_{ISR} = I_I = \frac{I_0}{(1-\alpha)} \tag{A.6}$$

The power dissipated through r_C is given by:

$$P_{r_C} = r_C + I_{C_{rms}}^2 \tag{A.7}$$

with

$$I_{C_{rms}} = \sqrt{\frac{1}{T}\int_0^T i_C^2 \mathrm{d}t} \tag{A.8}$$

and

$$i_C = \begin{cases} -I_0 & 0 < t < \alpha T \\ I_I - I_0 & \alpha T < t < T \end{cases} \tag{A.9}$$

replacing i_C by the above equation leads to:

$$I_{C_{rms}} = I_0\sqrt{\frac{\alpha}{(1-\alpha)}} \tag{A.10}$$

The output current I_O is:

$$I_0 = \frac{V_0}{R}$$

The power dissipated in the switch can be written as:

$$P_{FET} = P_{r_{DS}} + \frac{1}{2}P_{SW} \tag{A.11}$$

where $P_{r_{DS}}$ is the losses through the drain-source on resistance r_{DS} and P_{SW} the switching losses. We then have:

$$P_{r_{DS}} = r_{DS} * I^2_{S_{rms}} \tag{A.12}$$

where

$$I_{S_{rms}} = \sqrt{\frac{1}{T}\int_0^T i_S^2 \mathrm{d}t} \tag{A.13}$$

and

$$i_C = \begin{cases} I_I = \dfrac{I_0}{(1-\alpha)} & 0 < t < \alpha T \\ 0 & \alpha T < t < T \end{cases} \tag{A.14}$$

Inserting Equation (A.14) into Equation (A.13) we obtain:

$$I_{S_{rms}} = I_0\frac{\sqrt{\alpha}}{(1-\alpha)} \tag{A.15}$$

The switching losses are given by:

$$P_{SW} = f_S C_0 V^2_{SM} = f_S C_0 V_0^2 \tag{A.16}$$

The total losses in the switch S are then:

$$P_{FET} = r_{DS} I_0^2 \frac{\alpha}{(1-\alpha)^2} + \frac{1}{2} f_S C_0 V_0^2 \tag{A.17}$$

The power losses in the diode D is

$$P_D = P_{R_F} + P_{V_F} \tag{A.18}$$

where

$$P_{R_F} = R_F * I^2_{D_{rms}}$$

and

$$I_{D_{rms}} = \sqrt{\frac{1}{T}\int_0^T i_D^2 \mathrm{d}t}$$

with i_D being:

$$i_D = \begin{cases} 0 & 0 < t < \alpha T \\ I_I = \dfrac{I_0}{(1-\alpha)} & \alpha T < t < T \end{cases}$$

These above equations lead to:

$$I_{D_{rms}} = \frac{I_0}{\sqrt{(1-\alpha)}}$$

and then:

$$P_{R_F} = R_F \frac{I_0^2}{(1-\alpha)} \tag{A.19}$$

The last term in the power losses in the diode D is:

$$P_{V_F} = V_F I_D = V_F I_0 \tag{A.20}$$