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Progress of High Voltage Trenched and Implanted 4H-SiC Vertical JFET

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ABSTRACT

A silicon carbide (SiC) vertical channel junction field effect transistor (VJFET) was fabricated based on in-house SiC epitaxial wafer with trenched and implanted method. Its forward drain current is in excess of 3.12 A (170 W/cm^2) with a current gain of I_D/I_G = 19746 at gate bias V_G = 3 V and drain bias V_D = 5.5 V. The SiC VJFET device's related specific on-resistance 54 mΩ·cm^2. The BV gain is 250 V with V_g from -10 V to -4 V and is 350 V with V_g from -4 V to -2 V. Self-aligned floating guard rings provide edge termination that blocks 3180V at a gate bias of −14 V and a drain-current density of 1.53 mA/cm^2.

Keywords: 4H-SiC; VJFET; Ohmic; Trench; Implant

1. Introduction

The unique material properties of SiC are favorable for high power applications. The JFET is a voltage controlled, majority carrier device, and so it is one version of a field effect transistor (FET), where the voltage on the gate modulates the current flow between the drain and source regions. Compared to other transistors, FETs using a metal or junction gate are particularly well suited to high power or high speed applications. On the other hand, they are subject to substrate leakage current and the rather poor compactness of the structure limits the maximum current per device. But these drawbacks are in fact inherent to the usual horizontal configuration and are solved by a vertical orientation of the device. SiC power VJFETs have no reverse recovery charge thanks to unipolar MOSFET-like characteristics and are the solution for a unipolar SiC high power switch and are ideal candidates for next generation vehicle power conditioning systems [1, 2]. On account of the recent progress in device process and the quality of SiC substrates and epitaxial films, high voltage level SiC VJFET devices are available. Several large-area 1200-V-class SiC JFETs have been developed to meet the current handling requirements of modern power conditioning systems. The Infineon CoolSiC^{TM}, with its ultrafast body diode and dedicated Driver IC, represents the best solution for solar, UPS and industrial drives applications by combining best performance, reliability, safety and ease of use. A dedicated driver IC operates both normally-on JFET and p-MOS enables a normally-off behavior and best controllability of the JFET.

Previously, we have demonstrated 5.06 mΩ·cm^2, 395 A/ cm^2, 1200V and 5 A, 1300 V Trenched and Implanted 4H-SiC VJFETs with a vertical-channel structure fabricated in-house [3, 4]. In this article, we report our progress research on DC and experimental results of 3180 V blocking voltage and 3.12 forward current 4H-SiC VJFETs. The fabrication process is also described in detail. Overall, the vertical-channel JFET of **Figure 1** was fabricated in seven photolithographic levels with no epitaxial regrowth and with a single masked p^+ ion-implantation event that defined the gate and guard-ring edge-termination regions. A 10 mm^2 normally-off in excess of 3100 V blocking voltage 4H-SiC VJFET with a channel having uniform doping concentration of 5×10^{15} cm^{-3} and rectifying junctions formed using zero-degree Al ion-implantation and 1850℃ annealing.

2. Experimental

The n-type channel layer is used to form the vertical channel and the drift layer is designed to block over 3000 V. The implanted and lift-off trenched gate is formed by ICP etching and Al implantation. To simplify fabrication of the vertical-channel normally on JFET, the channel sidewall regions of the vertical pillars do not get implanted. On the other hand, the use of zero degree Al ion implantation can significantly reduce the amount of implantation damage propagating to the channel laterally

thereby significantly reducing the effect of the current saturation. In the case of using ion implantation to form non-uniform doping profiles, such profiles would experience the valleys between the concentration peaks corresponding to implantation energies. In order to minimize the influence of such valley between the concentration peaks, the implantation schedule must be designed carefully. The implantation energy may range from 40 Kev to 360 Kev and the implantation dose may range from $1\times10^{13}\,cm^{-2}$ to $1\times10^{15}\,cm^{-2}$. The computer simulation example is shown in **Figure 2**.

The gate is of the PN junction type which presents several advantages. To obtain the forward current, a positive gate voltage must be applied to the gate. The single chip has a total area of 10 mm^2. The SiC VJFETs

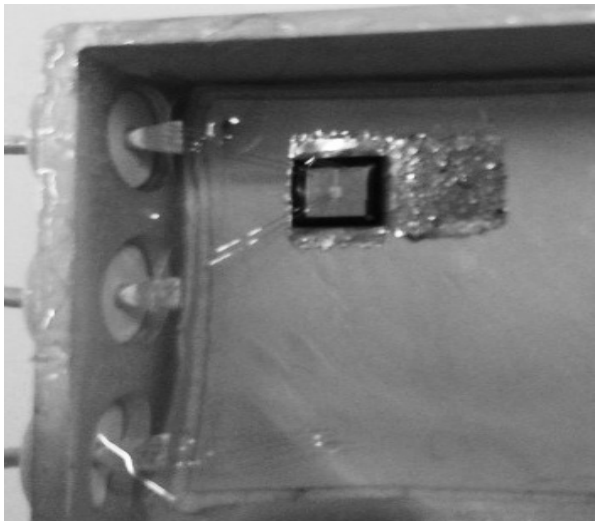

Figure 1. A 10 mm^2 normally-off in excess of 3100 V blocking voltage 4H-SiC VJFET.

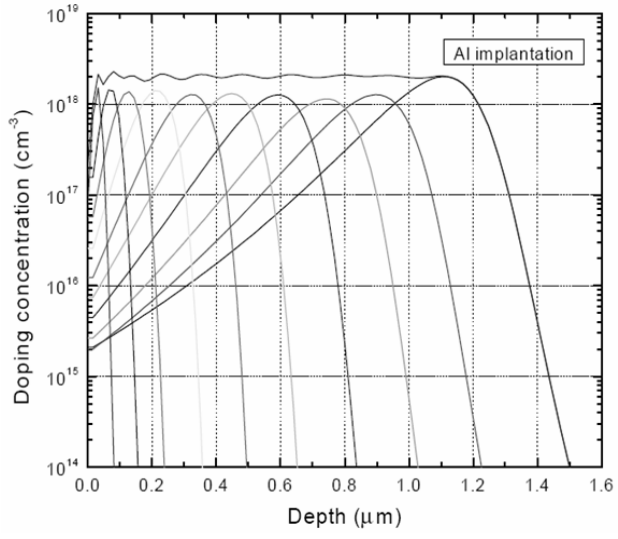

Figure 2. Computer simulation result of Al ion implantation multi energy and dose schedule.

are fabricated on a highly doped n^+ 4° off-axis Si-face 3-inch 4H-SiC substrate with epitaxially grown n^+ buffer, n^- drift, n^-channel, and n^+ source layers. The source layer is heavily doped to $n^+ > 2\times10^{19}\,cm^{-3}$ for Ni/SiC source ohmic contact formation. The n^- channel layer is 1.6 μm thick and doped to $1.6\times10^{16}\,cm^{-3}$. The drift layer is 50 μm thick and doped to $9\times10^{15}\,cm^{-3}$. The n+ buffer layer is 1 μm thick and doped to $1\times10^{18}\,cm^{-3}$. Edge termination is provided by a self-aligned floating guard-ring structure, which is p+ implanted simultaneously with the gates. The guard-ring structure serves to reduce the amount of field crowding at the main junction by spreading the depletion layer past consecutively lower potential floating junctions (rings). These independent junctions act to increase the depletion layer spreading, thereby decreasing the high electric field at the main junction [5]. The n-source and p-gate regions are simultaneously metalized with Ni in a single metal evaporation and lift-off processes. The gates and sources Ni ohmic metal layers are sintered at 950℃ to form nickel silicide ohmic contacts. Subsequent metal deposition and photoresist assisted metal lift-off create thick source and gate metallization. Dielectric layers are deposited for isolation, and ICP etching opens windows for thick gold interconnect metallization.

3. Results and Discussions

For reliable operation at the extreme condition, it was very important to form the stable metal/SiC contacts. Agilent B1500 A is used to measure the ohmic contact parameters. Tektronix 371 is used to measure the devices. To turn on the normally-off VJFET, a positive voltage must be applied to the gate. The maximum gate voltage is limited by the build-in voltage of the junction between the gate p+ region and the drift layer N-. From **Figure 3**, we can know that the SiC VJFET device yielded a drain current 3.12 A at a drain voltage of 3 V. The threshold voltage of V_{gd} = +2 V.

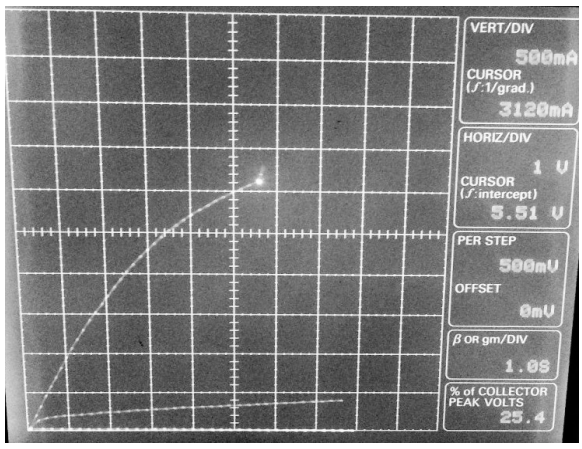

Figure 3. Forward I-V characteristics up to 3.12 A for SiC VJFET, Gate voltage from 0 V to 3 V by step 0.5 V.

In the linear region, the channel resistance is proportional to the channel length and inversely proportional to the doping concentration and the cross-sectional area of the current pass. In the saturation region, the channel resistance grows drastically that making this region of little use in most power switching applications. The device has a specific on-resistance of 54 $m\Omega \cdot cm^2$ not considering the guarding rings area. The non-uniformly doped channel can be used to control the current flow in normally-off SiC VJFET. The distance between the rectifying junctions in the JFET can be selected to provide a desired threshold voltage and we choose the width of source 1.7 um. The height of the vertical channel is one of the critical parameters for the high voltage normally-off VJFET. The leakage current density increases sharply with the decrease of height of the vertical channel, so the larger vertical channel height is needed. The height of our choice is 2 um.

In junction field-effect devices used in power switching applications, it is often highly desirable to not only reduce the channel resistance but also provide a MOSFET-like switching behavior. In particular, once the channel is pinched-off by the threshold voltage applied to the gate, it would be desirable if the device can block the maximum or rated voltage. Such device property requires infinitely high voltage blocking gain ß. In junction field-effect devices, low channel resistance and high voltage blocking gain are typically viewed as competing device characteristics. In long channel enhancement-mode JFETs such as power SiC VJFETs that can provide high voltage-blocking gain, the current saturates too early to fully utilize relatively low on-state channel resistance in the linear region. As a result, the development of normally-off switching devices has been impaired [6]. As illustrated in **Figure 4**, the SiC VJFETs' blocking voltage exceeds 3100 V at gate bias V_G = -14 V. The BV gain is 250 V with V_g from -10 V to -4 V and is 350 V with V_g from -4 V to -2 V.

As **Figure 5** shows, the gate voltage turn on the VJFET is 2.2 V and the change of this gate voltage is small as the drain voltage range from 1 V to 5 V.

4. Conclusions

A 3180-V 4H-SiC vertical-channel JFET of 10-mm^2 chip area was manufactured in seven photolithographic levels with no epitaxial regrowth and with a single masked p+ ion implantation event. The VJFET exhibits low gate-to-source and drain-to-source leakage currents with sharp onsets of breakdown. At a gate bias of 3 V, the VJFET outputs 3.12 A at a forward drain-voltage drop of 5.5 V (170 W/cm^2) with a specific on-state resistance of 54 $m\Omega \cdot cm^2$ and a current gain of I_D/I_G = 19746. The BV gain is 250 V with V_g from -10 V to -4 V and is 350 V with V_g from -4 V to -2 V. Self-aligned floating guard rings

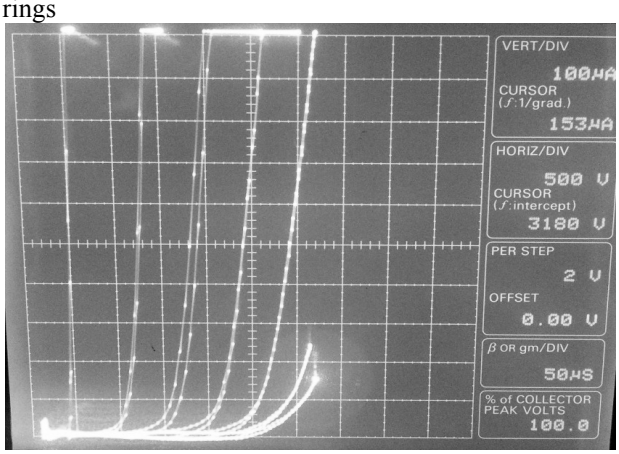

Figure 4. Reverse I-V characteristics up to 3180V (V_G= -14V) for SiC VJFET, Gate voltage from 0V to -14V by step -2V.

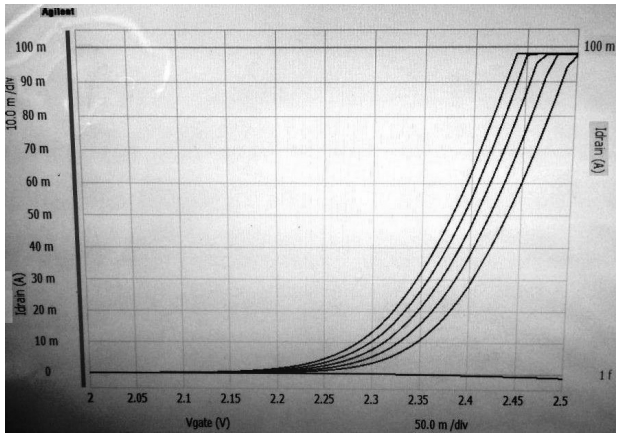

Figure 5. Forward I_d-V_g characteristics.

provide edge termination that blocks 3180 V at a gate bias of −14 V and a drain-current density of 1.53 mA/cm^2. VJFET switching characterization will be the subject of future investigation.

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