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# The Research on Stability of DC/DC in Parallel System

**Ye Xu, Pengfei Hou, Jinquan Wang, Lei Xu, Chaohong Shi**
PLA University of Science & Technology, Nanjing, China
Email: 19890224hpf@163.com

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## ABSTRACT

In this paper, a main structure of DC distributed power system is introduced; the stability of the output voltage in parallel system is put forward. This paper analyses the output impedance of master-slave current sharing mode and average current sharing, analyses the stability of parallel system through simulation, there is Right-half plane (RHP) polar in the Bode plot of input impedance. At last this paper distinguishes whether this system is stability and verifies the validity of the simulation.

**Keywords:** DC; Parallel System; Output Impedance; Bode; RHP Polar

## 1. Introduction

With the development of distributed power system, the role of power electronic devices is more and more important. In the actual power system，power supply module is inevitably involved in cascade, parallel, series, combination of collaborative work form. The interaction between each subsystem effects on the overall performance of the power system including stability analysis, dynamic performance, steady state harmonic power influence the quality and electromagnetic interference and other related fields. Meanwhile, each module may come from different suppliers; the power supply module is gradually standardized to meet industry needs at the same time. The compatibility match also needs to standardize the definition in order to ensure the universality and interchangeability. The integrated system performance degradation even be shocked.

For DC Distributed Power System, usually diesel units after rectifier connected to the DC grid, the battery after a bidirectional DC/DC connected to the grid. Supply power to the DC load side by DC/DC transformer, Supply power to the AC load side by DC/AC transformer. As shown in **Figure 1** for DC Distributed System.

The method of stability analysis of the previous system needs to know module structure and parameter while the criterion is complex, the method based on single module impedance measurement only needs Current-sharing method of parallel system and working condition. Measuring the output impedance of single module independently is through the relationship between total output impedance and output impedance of parallel system with a single module to get the total output impedance, according to whether the output impedance of parallel system has the right half plane pole to judge the stability of the parallel system.

## 2. Total Output Impedance of Parallel System Based on Master-slave Current Sharing Mode

As shown in **Figure 2** is equivalent circuit model based on master-slave current sharing mode. When the current communication line interface is hanged, voltage loop plays a role and current-sharing loop is invalid. When the flow line of communication interface is connected with constant voltage source, current disturbance is 0, Output impedance contains all information flow regulator [1].

$$Z_{csi} = \frac{Z_{csi}^{*}}{1+\frac{Z_{csi}^{*}-Z_{oi}}{Z_{oM}}} \tag{1}$$

Among them $Z_{oM}$ is the output impedance of the main module, $Z_{oi}$ is output impedance of i when module communication line is hanged, $Z_{csi}^{*}$ is output impedance of $i$ when module communication line is connected with constant voltage source. The total output impedance of the system is:

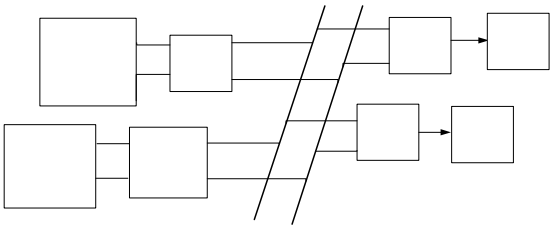

**Figure 1. DC distributed power system.**

 

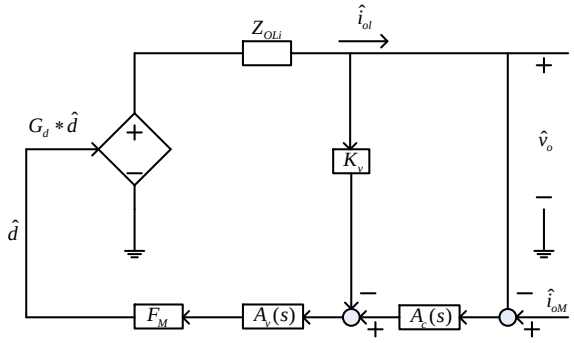


**Figure 2. Circuit model of parallel system based on master-slave current sharing mode.**

$$Z_s = \frac{1}{\sum 1/Z_{csj}} \tag{2}$$

## 3. Total Output Impedance of Parallel System Based on Average Current Sharing Mode

The same, as shown in **Figure 3** is equivalent circuit model based on average current sharing mode [4].

Output impedance of module i is:

$$Z_{csi} = \frac{Z^*_{csi}}{1+(Z^*_{csi}-Z_{oi})\cdot\sum\frac{1}{Z^*_{csi}}/\sum\frac{Z_{oi}}{Z^*_{csi}}} \tag{3}$$

$Z_{oi}$ is output impedance of i when module communication line is hanged, $Z_{csi}$ is output impedance of i when module communication line is connected with constant voltage source [2]. Hence, The total output impedance of the system is:

$$Z_s = \frac{1}{\sum 1/Z_{csj}} = \frac{1}{n}\cdot\sum\frac{Z_{oj}}{Z^*_{csj}}/\sum\frac{1}{Z^*_{csj}} \tag{4}$$

Among them $Z_{csj}$ is the output impedance of j when modules are worked in parallel, $Z_{csj}$ is output impedance of j when module communication line is hanged. $Z_{csj}$ is output impedance of *j* when module communication line is connected with constant voltage source [3].

## 4. Simulation of Parallel System

As shown in **Figure 4** is Bode graph of total output impedance of the parallel system based on master-slave current sharing mode. The graph shows that the output impedance of the amplitude and phase changes with frequency, the upper one is the direct measurement result and the lower one is computing result. As can be seen by comparing, the measurement results and the computing results are in agreement. Therefore the acquisition method of output impedance of parallel system based on master-slave current sharing mode is validated.

As shown in **Figure 5** is Bode graph of total output impedance of the parallel system based on average current sharing mode. The lower one is the direct measurement result and the upper one is computing result. As can be seen by comparing, the measurement results and the

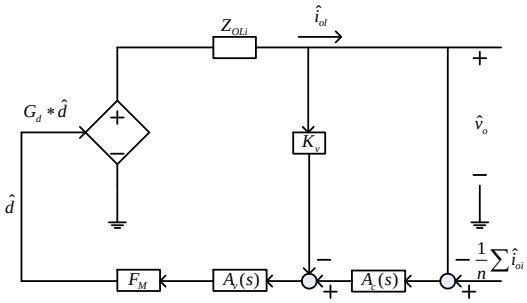


**Figure 3. Circuit model of parallel system based on average current sharing mode.**

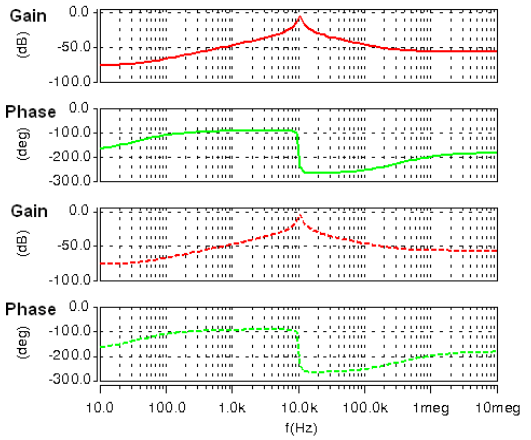


**Figure 4. Total output impedance of the parallel system based on master-slave current sharing mode: Direct measurement result (up), computing result (down).**

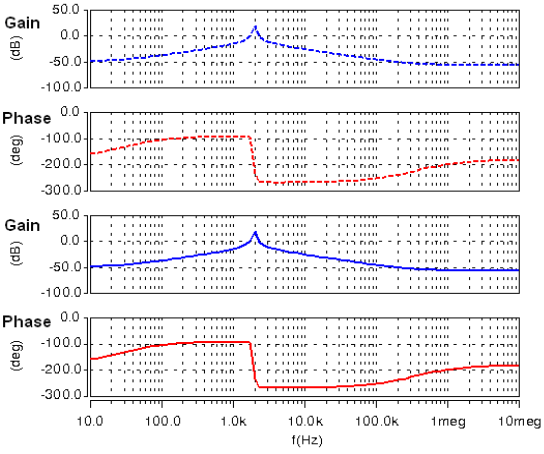


**Figure 5. Total output impedance of the parallel system based on average current sharing mode: Direct measurement result (down), computing result (up).**

 

computing results are in agreement. Therefore the acquisition method of output impedance of parallel system based on average current sharing mode is validated.

## 5. Simulation Analysis of Parallel System Stability

For the total output impedance of parallel systems, the parallel system is stable if there are not RHP poles in the total output impedance; the parallel system is not stable while there are RHP poles.

As shown in **Figure 6** is Bode graph of total output impedance obtained from simulation in stable parallel system, there are no RHP poles in the graph.

As shown in **Figure 7** is simulation results in time domain of parallel system, it shows two parallel converter output current signal and the output voltage signal, from the graph we can see the output voltage is stable.

As shown in **Figure 8** is Bode graph of total output impedance obtained from simulation in unstable parallel system, there are RHP poles in the graph. From the graph we can see there are RHP poles around 7.2 kHz.

As shown in **Figure 9** is simulation results in time domain of parallel system, from the graph we can see there is turbulence in the output voltage of parallel system and there is ripple in output current, it proves that the system is unstable.

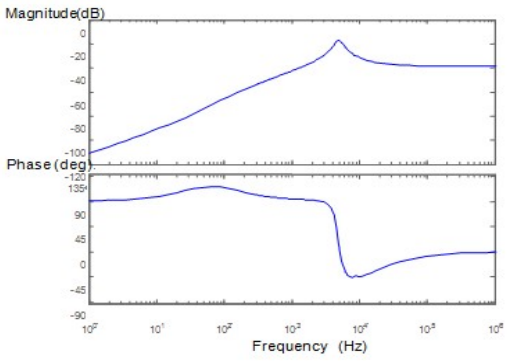


**Figure 6. Bode graph of total output impedance in stable parallel system.**

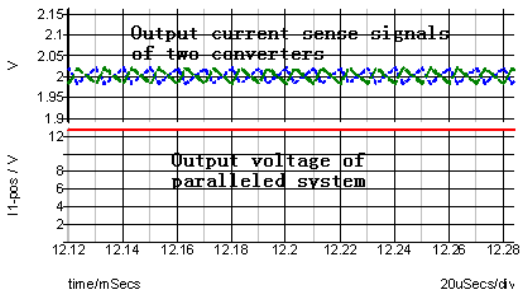


**Figure 7. Simulation results of parallel system in time domain.**

## 6. Experiment on Validating Stability of Parallel System

Through the above analysis, DC power is put as the power supply for the parallel system, two DC/DC power electronic loads work in parallel, measuring the output impedance of parallel system by network analyzer. Both a stable system (Experiment 1) and an unstable system (Experiment 2) are measured.

As shown in **Figure 10** is Bode graph of total output

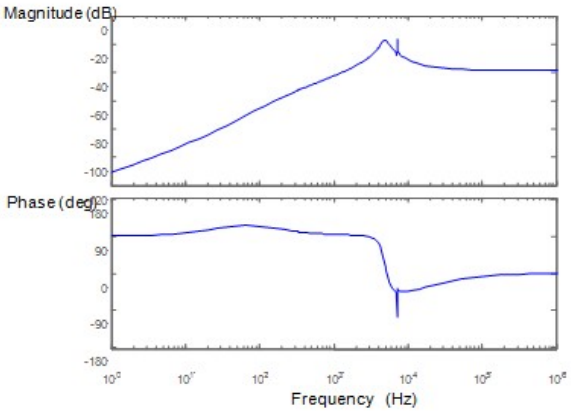


**Figure 8. Bode graph of total output impedance in unstable parallel system.**

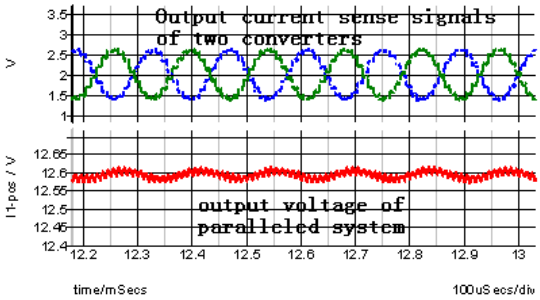


**Figure 9. Simulation results of parallel system.**

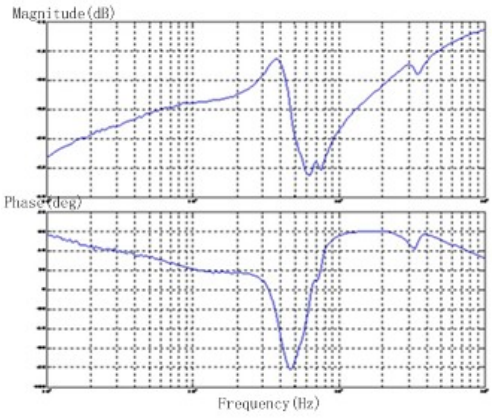


**Figure 10. The experimental result of experiment 1.**

 

impedance obtained from experiment 1.There are no RHP poles, so the system is stable.

For the output voltage of parallel system corresponding with the experiment 1, simulation results in the time domain are shown in **Figure 11**:

Experiment verifies the simulation results, for the simulation of stable system, the experimental system is stable at the same time, and there are no RHP poles in output impedance.

As shown in **figure 12** is Bode graph of total output impedance obtained from experiment 1.There are RHP poles around 5 kHz, so the system is unstable.

Simulation results of experiment 2 in the time domain are shown in **Figure 13**.

For unstable system in experiment 2, there are a large number of ripples in output voltage, the system is unstable. There are RHP poles in Bode graph of output impedance, the experiment is verified through simulation.

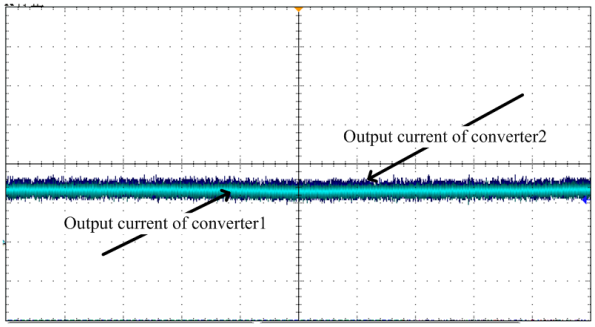


**Figure 11. Simulation results in the time domain of experiment 1.**

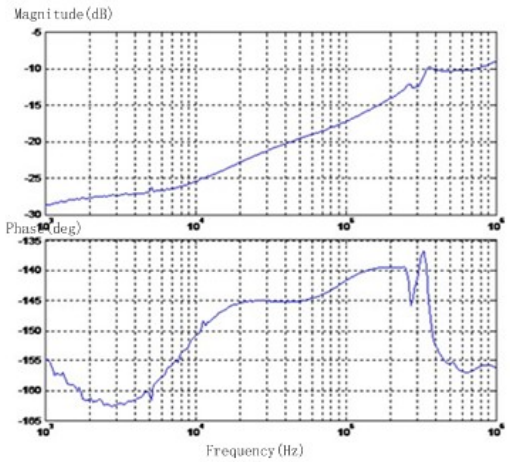


**Figure 12. The experimental result of experiment 2.**

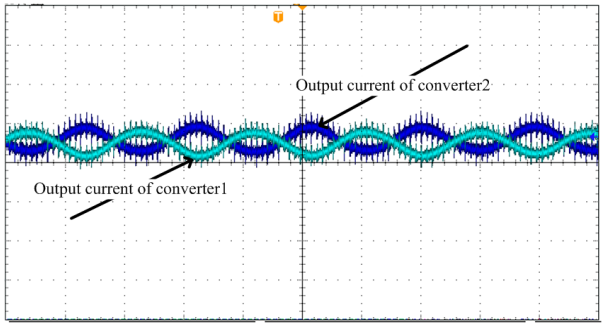


**Figure 13. Simulation results of experiment 2.**

## 7. Conclusions

This paper analyzes the DC distributed system structure firstly. In parallel with a plurality of power electronic module in DC distributed system will cause instability, then it analyses the output impedance of master-slave current sharing mode and average current sharing, and verify the method of obtaining output impedance in parallel system, after that it simulates the stability of the parallel system. At last experiment verifies the correctness of the simulation.

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