Energy and Power Engineering, 2012, 4, 107-116
http://dx.doi.org/10.4236/epe.2012.43015 Published Online May 2012 (http://www.SciRP.org/journal/epe)

Modeling and Current Programmed Control of a Bidirectional Full Bridge DC-DC Converter

Shahab H. A. Moghaddam, Ahmad Ayatollahi, Abdolreza Rahmati
School of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran
Email: shahab.h.moghaddam@gmail.com, {ayatollahi, rahmati}@iust.ac.ir

Received February 7, 2012; revised February 28, 2012; accepted March 16, 2012

ABSTRACT

Modelling of bidirectional full bridge DC-DC converter as one of the most applicable converters has received significant attention. Mathematical modelling reduces the simulation time in comparison with detailed circuit response; moreover it is convenient for controller design purpose. Due to simple and effective methodology, average state space is the most common method among the modelling methods. In this paper a bidirectional full bridge converter is modelled by average state space and for each mode of operations a controller is designed. Attained mathematical model results are in a close agreement with detailed circuit simulation.

Keywords: Average State Space; Bidirectional; Detailed Circuit Simulation; Full Bridge DC-DC Converter; Mathematical Modeling

1. Introduction

Modeling of DC-DC converter as one of the most applicable industrial converters has aroused a lot of interest. Since modeling gives us information about static and dynamic of the system, it is a crucial factor in design and control. Moreover, attained mathematical model can reduce the simulation time in comparison with the simulation time provided by "cycle by cycle" solving the differential equations of the circuit, as is the case in matlab/simulink.

With respect to renewable energy systems and optimum use of regenerated energy, interface converters should be capable of transferring power in both directions. So bidirectional DC-DC converters (BDC) are one of the most important interfaces that have applications such as: hybrid or electrical vehicles [1], aerospace systems [2], telecommunications, solar cells, battery chargers [3], DC motor drive circuits [4], uninterruptable power supplies [5-7], etc. so far many BDCs topologies have been introduced and surveyed [8,9]. In applications that transferred power is more than 750 watts, full bridge topology is a proper one [10].

Bidirectional full bridge (FB) converters have been studied in many papers like [11-13]. A general modeling method that develops the discrete time average model is proposed in [12]. The operation period is divided to 3 intervals, the equivalent circuit and the differential equations for each interval are written in matrix form. After solving equations and applying approximation of Taylor expansion, the averaging state vector in half cycle gives us the final answer. Since time domain method employs numerical integration to solve differential equations the analysis is complicated and computationally intensive. Moreover the information about the dependence of the converter's operating conditions on the circuit parameters is not provided [14].

Reference [13] proposes a discrete Small signal model with the amount of considerable calculation, just to predict the peak response of state vectors. There are also some identification-based methods like NARMAX [15, 16] and Hammerstein [17,18] to model the DC-DC converter. Hammerstein model involves of a static nonlinearity followed by a linear discrete-time and time-invariant model, but identification based methods consider the system as a black/gray box, therefore they do not provide any insight into circuit details. So many references use circuit oriented methods to model the converter. Vorperian and Tymerski *et al*. [19,20] provide the circuit switch model with replacing the PWM switch with its equivalent circuit in order to model the converter. This method may pose some complexity especially in non-basic topologies. Another circuit oriented method that is introduced by Middlebrook and Cuk [21-23] in 1977 is the average state space. An advantage of the state-space averaging method is its efficiency compared to that of the switched model because there is not any switching frequency ripple and, consequently, the simulation time required by the averaged model is much lower than required by the switched model. Among all methods of

modeling, average state space seems to be one of the most common, simplest, and effective methods, so in this paper we model a bidirectional full bridge DC-DC converter with average state space to gain the appropriate transfer functions for controller design purpose in both modes of operation.

2. Principle of Operation

Figure 1 shows the proposed bidirectional full bridge converter where arrows represent the direction of power flow. There are so many configurations for FB converters [11,14,24] with the same basic topology which differs from one another in the case of switching scheme or employing the elements of converter for the purpose of achieving ZVS or ZCS. Since modeling of this converter is the main purpose of this study and Changing modes of operation rely on conditions of application; these conditions are not taken into consideration.

Detailed Circuit description can be reviewed in the literature [24,25]. There are some long and short intervals in each mode, since the short ones are not as significant as long ones they can be left out. Meanwhile **Figure 2** shows the basic waveforms and pulse gating of switches in boost mode operation, ignoring the short subintervals, **Figure 3** depicts the buck mode waveforms. Small signal

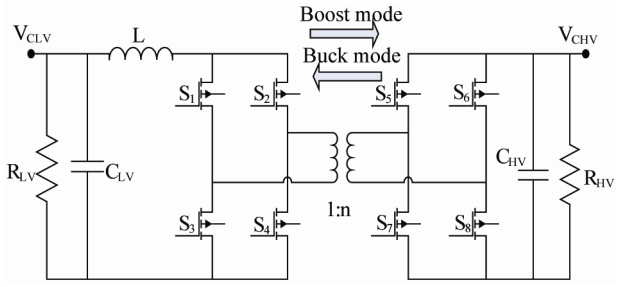

Figure 1. Basic topology of the proposed FB bidirectional converter.

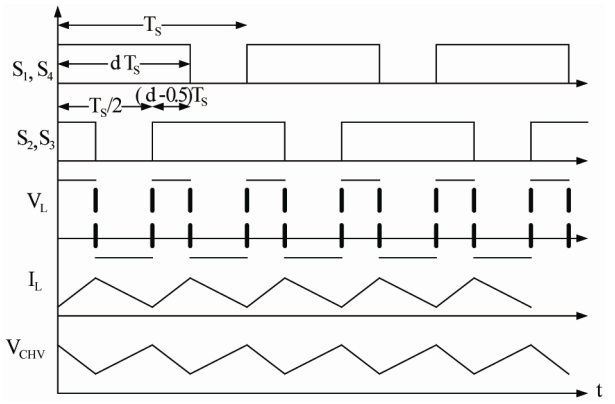

Figure 2. Ideal steady-state voltage and current waveforms of the converter in boost mode operation during one switching cycle.

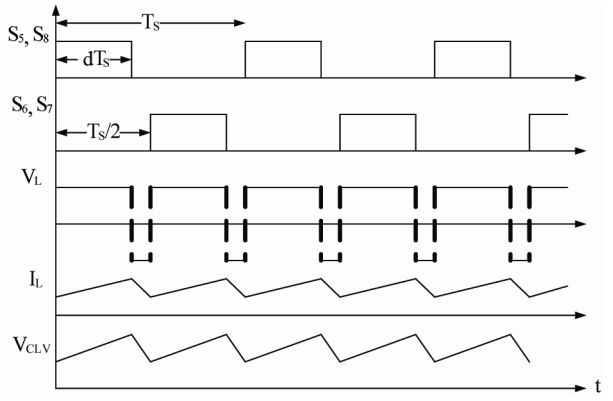

Figure 3. Ideal steady-state voltage and current waveforms of the converter in buck mode operation during one switching cycle.

model of each mode will be extracted. For simplicity of control, gating circuit, and analysis, it is assume that in every mode only switches of one side are gated meanwhile the opposite ones are operating in their diode modes.

2.1. Boost Mode Operation

In boost mode with respect to pulse gating signals, there are two main intervals, consisting of four switches on and two diagonal switches on. When four switches turn on, input inductor voltage is equal to input source (low voltage side) and the inductor current increase proportional to the applied voltage. In this interval inductor saves the energy to transfer it in the next interval. While at the high voltage (HV) side the load is fed by the energy that has been transferred to the output filter (C) during pervious interval.

Next interval usually is known as the energy transfer interval. For instance, assume that S_1 and S_4 are on and S_2 and S_3 are off. The input voltage plus inductor voltage is applied to transformer and is scaled by n factor, ratio of secondary to primary voltage, then will be rectified through the other side of bridge. These processes will be repeated at next half switching cycle with this point that the primary applied voltage in next half switching cycle will be negative but will be rectified in the other side of the bridge.

2.2. Buck Mode Operation

According to **Figure 3** that shows the conventional pulse gating, hard switch, for buck mode operation, again there are two main intervals in a half switching cycle, first when diagonal switches turn on, and second one when all switches turn off. When diagonal switches are on, for instance S5 and S8, the power is transferred from high HV side to LV side. In this interval the inductor current increases proportional to the scaled HV side voltage minus output (nominal LV) voltage.

With turning off the switches, next interval starts. Although the existence of leakage inductance prevents the switches go off immediately after applying gate turn off pulses and conduction of switches will continue through parasitic capacitors and diodes, but it is assumed that these subintervals are very short and can be neglected. In off time, the secondary side is only fed by the inductor stored energy, so the inductor current decreases proportional to output voltage. Next half switching cycle is the same, and only applied voltage of HV side is negative that is rectified in LV side.

3. Small Signal Modeling Using Average State Space

Employing average state space method is divided into three phases:

1) With respect to switch conditions, the circuit is divided into different subintervals and state equations are written in the matrix form in each interval. State vectors are defined as inductors currents and capacitors voltages.

2) Averaged equations are formed by taking weighted average of state equations of each interval.

3) Averaged equations are written in differential form then linearization is done by perturbing variables. Employing Laplace transform and omitting additional AC and DC terms (only first order AC terms), needed transfer functions are achieved.

For simplicity of modeling the following assumptions can be employed:

- Switches are ideal, there is no parasitic effect in switches;
- Inductor has no resistance;
- Transformer is ideal and there are no leakage and magnetizing inductances;
- Filter capacitors have low ESR (equivalent series resistance) that can be neglected;
- Load is constant and for modeling of the load change an additional current source has been added at the output;
- Each mode (buck or boost modes) starts with zero initial condition.

State equations will be written in each mode separately and with some mathematical operations one can derive needed transfer functions.

3.1. Boost Mode State Equations

As we saw in Section 2.1 in this mode two main intervals can be assumed. When all four switches conduct the equivalent circuit will be the same as shown in **Figure 4** and the differential equations can be written as follows:

$$v_{IN} = L\frac{\mathrm{d}i_L}{\mathrm{d}t} \Rightarrow \frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{1}{L}v_{IN} \tag{1}$$

$$\frac{v_c}{R} + C\frac{\mathrm{d}v_c}{\mathrm{d}t} = i_z \Rightarrow \frac{\mathrm{d}v_c}{\mathrm{d}t} = \frac{1}{C}i_z - \frac{1}{RC}v_C \tag{2}$$

$$\begin{bmatrix} \frac{\mathrm{d}i_L}{\mathrm{d}t} \\ \frac{\mathrm{d}v_c}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}\begin{bmatrix} v_{IN} \\ i_Z \end{bmatrix} \tag{3}$$

This state lasts for $(d - 0.5)T_s$ where $T_s = 1/f_s$ is period of switching, $d = t_{on}/T_s$ is the effective duty ratio and n is turn ratio of secondary to primary windings. In the next interval when diagonal switches conduct, the equivalent circuit can be sketched as the same in **Figure 5** and the state equations can be written as below:

$$-v_{IN} + L\frac{\mathrm{d}i_L}{\mathrm{d}t} + \frac{v_C}{n} = 0 \Rightarrow \frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{1}{L}v_{IN} - \frac{1}{nL}v_C \tag{4}$$

$$\frac{i_L}{n} + i_Z = \frac{v_C}{R} + c\frac{\mathrm{d}v_C}{\mathrm{d}t} \Rightarrow \frac{\mathrm{d}v_C}{\mathrm{d}t} = \frac{1}{nC}i_L + \frac{1}{C}i_Z - \frac{1}{RC}v_C \tag{5}$$

$$\begin{bmatrix} \frac{\mathrm{d}i_L}{\mathrm{d}t} \\ \frac{\mathrm{d}v_c}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{nL} \\ -\frac{1}{nC} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}\begin{bmatrix} v_{IN} \\ i_Z \end{bmatrix} \tag{6}$$

$$Y = v_C = v_o \Rightarrow Y_c = \begin{bmatrix} 0 & 1 \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix}\begin{bmatrix} v_{IN} \\ i_Z \end{bmatrix} \tag{7}$$

This state lasts for $(1 - d)T_s$. The output state in both intervals is the same as Equation (7). Now averaging the state equations during half switching cycle will result in the equation that has the characteristic of two intervals:

$$A_t = \begin{bmatrix} 0 & \frac{2(d-1)}{nL} \\ \frac{2(1-d)}{nC} & -\frac{1}{RC} \end{bmatrix} \;\&\; B_t = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} \tag{8}$$

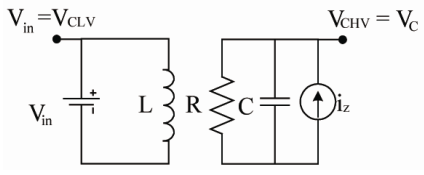

Figure 4. Equivalent circuit of boost mode operation with four LV switches on.

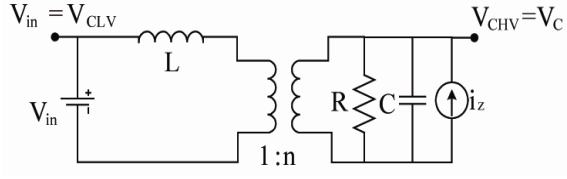

Figure 5. Circuit of boost mode operation with two LV switches on.

$$\dot{X}=\begin{bmatrix}\dot{i}_L\\ \dot{v}_C\end{bmatrix}=\begin{bmatrix}0 & \frac{2(d-1)}{nL}\\ \frac{2(1-d)}{nC} & -\frac{1}{RC}\end{bmatrix}\begin{bmatrix}i_L\\ v_C\end{bmatrix}+\begin{bmatrix}\frac{1}{L} & 0\\ 0 & \frac{1}{C}\end{bmatrix}\begin{bmatrix}v_{IN}\\ i_Z\end{bmatrix} \tag{9}$$

$$Y_c=CX+DU=\begin{bmatrix}0 & 1\end{bmatrix}\begin{bmatrix}i_L\\ v_C\end{bmatrix}+\begin{bmatrix}0 & 0\end{bmatrix}\begin{bmatrix}v_{IN}\\ i_Z\end{bmatrix} \tag{10}$$

Perturbing the state equations around their operating points will result in the equations that can be used for deriving the transfer functions; to do so one just need to write voltages and currents in the following forms:

$$\begin{cases} i_L=I_L+\tilde{i}_L\\ V_c=V_C+\tilde{v}_c\\ v_{IN}=V_{IN}+\tilde{v}_{in}\\ i_Z=\tilde{i}_z\\ d=D+\tilde{d}\end{cases} \tag{11}$$

$$\frac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t}+\frac{\mathrm{d}I_L}{\mathrm{d}t}=\frac{2(D+\tilde{d}-1)}{nL}\left(V_C+\tilde{v}_c\right)+\frac{1}{L}\left(V_{IN}+\tilde{v}_{in}\right) \tag{12}$$

$$\frac{\mathrm{d}\tilde{v}_c}{\mathrm{d}t}+\frac{\mathrm{d}V_C}{\mathrm{d}t}=\frac{2\left(1-D-\tilde{d}\right)}{nC}\left(I_L+\tilde{i}_L\right)-\frac{1}{RC}\left(V_C+\tilde{v}_c\right)+\frac{1}{C}\tilde{i}_z \tag{13}$$

$$\frac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t}=\frac{2\left(D+\tilde{d}-1\right)}{nL}\left(V_C+\tilde{v}_c\right)+\frac{1}{L}\left(V_{IN}+\tilde{v}_{in}\right) \tag{14}$$

$$\frac{\mathrm{d}\tilde{v}_c}{\mathrm{d}t}=\frac{2(1-D-\tilde{d})}{nC}\left(I_L+\tilde{i}_L\right)-\frac{1}{RC}\left(V_C+\tilde{v}_c\right)+\frac{1}{C}\tilde{i}_z \tag{15}$$

For extracting transfer functions additional AC and DC terms can be neglected. With applying Laplace transform to the equations one can achieve the following transfer functions.

$$\frac{\tilde{v}_c}{\tilde{v}_{in}}=\frac{2(1-D)n}{n^2CLS^2+n^2\frac{L}{R}S+4(1-D)^2} \tag{16}$$

$$\frac{\tilde{v}_c}{\tilde{d}}=\frac{-2nLI_LS+8(1-D)V_C-2nV_{IN}}{n^2CLS^2+n^2\frac{L}{R}S+4(1-D)^2} \tag{17}$$

$$\frac{\tilde{i}_L}{\tilde{d}}=\frac{2nCV_CS+8(1-D)I_L}{n^2CLS^2+n^2\frac{L}{R}S+4(1-D)^2} \tag{18}$$

$$\frac{\tilde{v}_c}{\tilde{i}_z}=\frac{n^2SL}{n^2CLS^2+n^2\frac{L}{R}S+4(1-D)^2} \tag{19}$$

3.2. Buck Mode State Equations

The method is the same as mentioned in previous section for the boost mode operation. Two main operating intervals are considered to illustrate circuit conditions. No matter what switching scheme is employed, conventional PWM, phase shift or PWM plus phase shift, there is always an effective duty cycle, D_{eff}. **Figures 6** and **7** depict the main equivalent circuits meanwhile (20) and (21) describe state equations. Note that in writing equations, output voltage (LVS) is mentioned as V_c and the input voltage at HV side is defined as V_{in}.

$$\begin{bmatrix}\frac{\mathrm{d}i_L}{\mathrm{d}t}\\ \frac{\mathrm{d}v_c}{\mathrm{d}t}\end{bmatrix}=\begin{bmatrix}0 & -\frac{1}{L}\\ -\frac{1}{C} & -\frac{1}{RC}\end{bmatrix}\begin{bmatrix}i_L\\ v_C\end{bmatrix}+\begin{bmatrix}\frac{1}{nL} & 0\\ 0 & \frac{1}{C}\end{bmatrix}\begin{bmatrix}v_{IN}\\ i_Z\end{bmatrix} \tag{20}$$

This interval will lasts for dT_s seconds. Following interval will last for the remained half cycle, $(0.5-d)T_s$.

$$\begin{bmatrix}\frac{\mathrm{d}i_L}{\mathrm{d}t}\\ \frac{\mathrm{d}v_c}{\mathrm{d}t}\end{bmatrix}=\begin{bmatrix}0 & -\frac{1}{L}\\ -\frac{1}{C} & -\frac{1}{RC}\end{bmatrix}\begin{bmatrix}i_L\\ v_C\end{bmatrix}+\begin{bmatrix}\frac{1}{L} & 0\\ 0 & \frac{1}{C}\end{bmatrix}\begin{bmatrix}v_{IN}\\ i_Z\end{bmatrix} \tag{21}$$

Averaging in half switching cycle and perturbing the voltage and currents will result the needed transfer functions.

$$\frac{\tilde{v}_C}{\tilde{v}_{in}}=\frac{\left(\frac{2D}{n}\right)}{CLS^2+\frac{L}{R}S+1} \tag{22}$$

$$\frac{\tilde{v}_c}{\tilde{d}}=\frac{\left(\frac{2V_{IN}}{n}\right)}{CLS^2+\frac{L}{R}S+1} \tag{23}$$

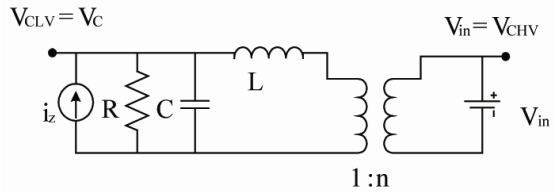

Figure 6. Equivalent circuit of buck mode operation with two HV switches conducting.

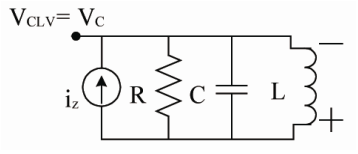

Figure 7. Equivalent circuit of buck mode operation with shorting HV side.

$$\frac{\tilde{i}_L}{\tilde{d}} = \frac{\left(\frac{2CV_{IN}}{n}\right)S + \frac{2V_{IN}}{n}}{CLS^2 + \frac{L}{R}S + 1} \quad (24)$$

$$\frac{\tilde{v}_c}{\tilde{i}_z} = \frac{LS}{CLS^2 + \frac{L}{R}S + +1} \quad (25)$$

4. Model Verification

Having averaged state equation and perturbation one can achieve all transfer functions needed for controller design. In this section verification of the attained averaged model is done by comparing the step responses of transfer functions derived from average state space and simulated circuit in matlab/simulink.

4.1. Boost Mode

Start up process of open loop converter system with input voltage of 24 V is simulated under these conditions: D = 0.6, f_s = 20 kHz, L = 200 μH, C = 50 μF, $V_{out} = V_c$ = 300 V, $P_{in} = P_{out}$ = 1.5 KW, R = 60 Ω.

The simulated start up process of the predicted mathematical model and detailed circuit simulation with fixed duty cycle is depicted in **Figures 8(a)** and **(b)**, respectively. Steady state, peak response, and rise time of output voltage in simulink is the same as obtained by the mathematical model but settling time differs 0.00007 seconds which is acceptable.

In order to check control to output and control to inductor current transfer functions, a small step (0.01) can be applied to duty cycle in the both mathematical models and simulated circuit. **Figure 9** shows the output voltage response to duty cycle change and **Figure 10** represents the current waveforms while **Figure 11** represents the output voltage change due to 1A step change in load current that is modeled by a current source, i_z.

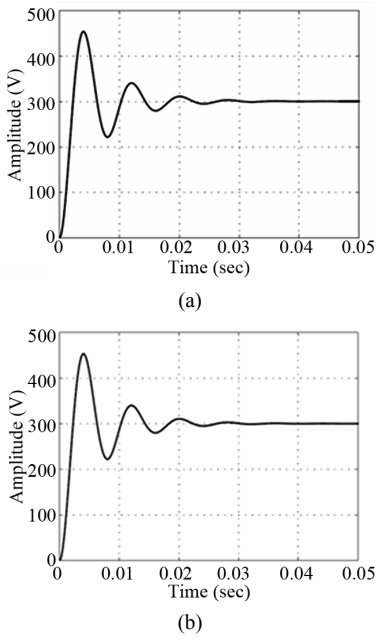

Figure 8. Start-up processes (a) Simulated mathematical averaged; (b) Detailed circuit simulation in matlab/simulink.

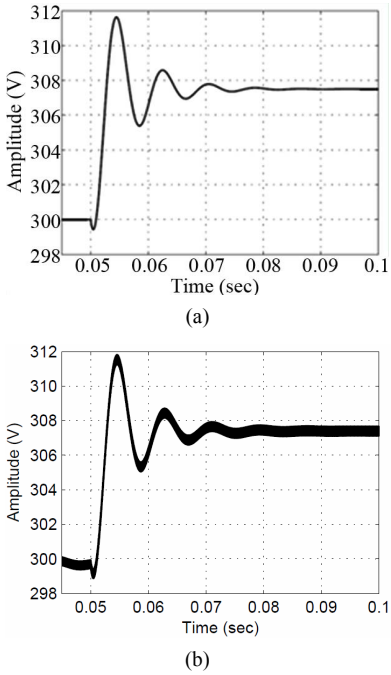

Figure 9. Output voltage in the presence of 0.01 step change in duty cycle. (a) Predicted response by mathematical averaged model; (b) Detailed circuit simulation in matlab/simulink.

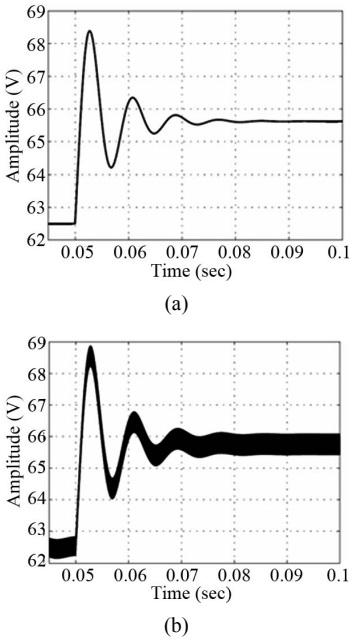

Figure 10. Inductor current in the presence of 0.01 step change in duty cycle. (a) Predicted response by mathematical averaged model; (b) Detailed circuit simulation in matlab/simulink.

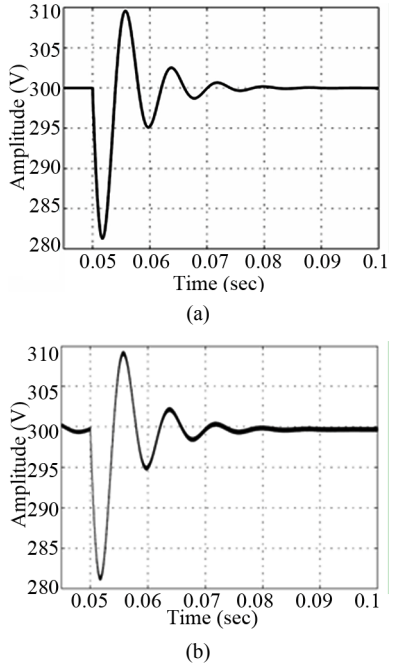

Figure 11. Output voltage in the presence of 1A step change in load current. (a) Predicted response by mathematical averaged model; (b) Detailed circuit simulation in matlab/ simulink.

4.2. Buck Mode

Start up process of open loop converter system with input voltage of 300V is simulated under these conditions: D = 0.4, f_s = 20 kHz, L = 200 μH, C = 50 μF, $V_{out} = V_c$ = 24 V, $P_{in} = P_{out}$ = 1.5 KW, R = 0.384 Ω.

From **Figure 12** it can be seen that the mathematical model has predicted the response of the converter very well. **Figures 13** and **14** represent the behavior of output voltage and inductor current in the presence of 0.02 step change in duty cycle. **Figure 15** shows converter output voltage due to 0.5A step change in load, it is obvious that the mathematical model is in a close agreement with simulated circuit.

5. Controller Design

Switch mode power supplies (SMPS) control methodology can be divided into two main methods consisting of voltage mode control (VMC) and current mode control. Current mode control (CMC) is faster than voltage mode but it suffers from ringing, so merging two methods can cover the shortage of both. Current programmed control (CP) method that is presented in [10,26,27] employs CMC and VMC together. **Figure 16** shows the block diagram of CPC which is mainly divided to peak, valley, and average [28]. Among all of those methods of CPC, the peak current programmed control (PCPC) is one of the most common modes and easiest one to understand.

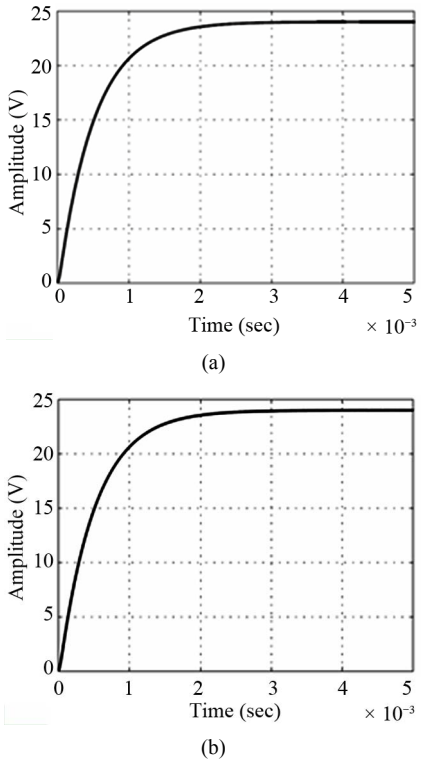

Figure 12. Open loop start up output voltage with fixed duty cycle (a) predicted by mathematical model; (b) Detailed circuit simulation with matlab/simulink.

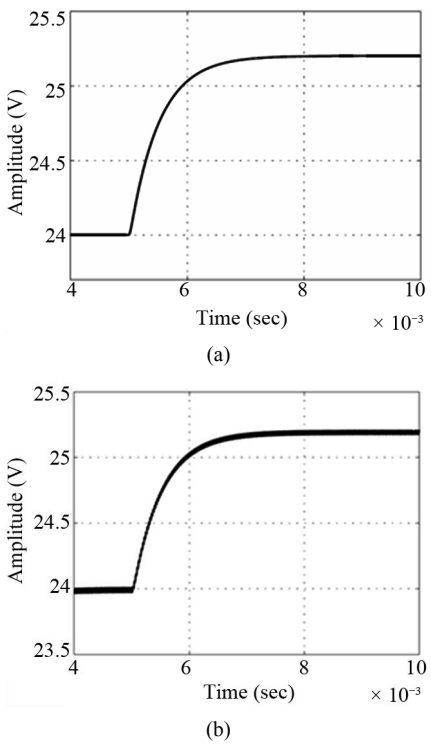

Figure 13. Open loop response of output voltage due to 0.02 step change in duty cycle (a) predicted by mathematical model; (b) Detailed circuit simulation with matlab/simulink.

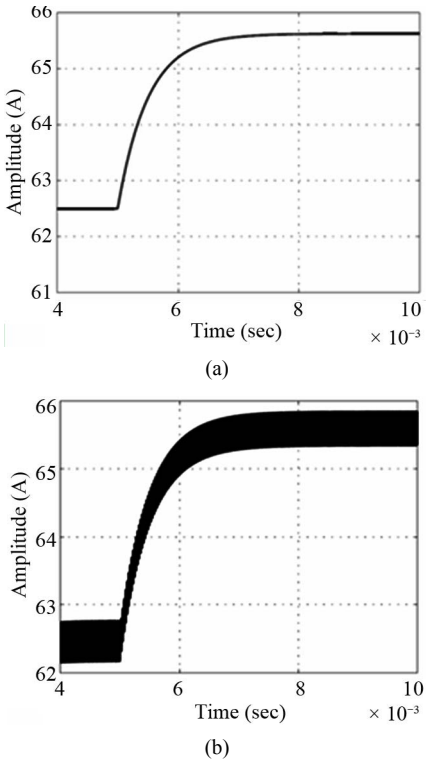

Figure 14. Open loop response of inductor current due to 0.01 step change in duty cycle (a) predicted by mathematical model; (b) Detailed circuit simulation with matlab/simulink.

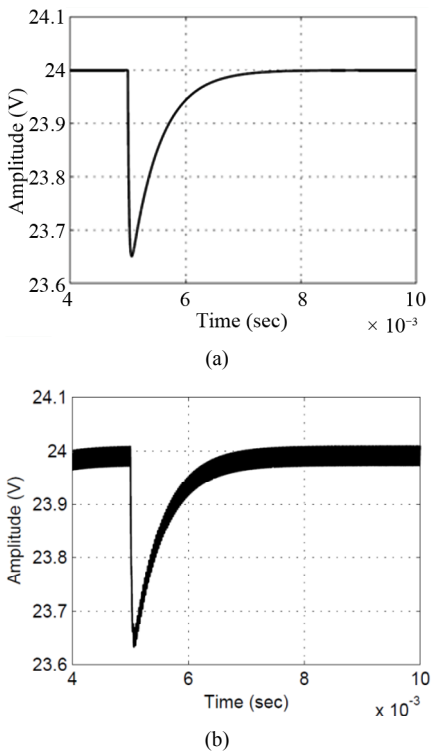

Figure 15. Open loop response of output voltage due to 1A step change load current (a) predicted by mathematical model; (b) Detailed circuit simulation with matlab/simulink.

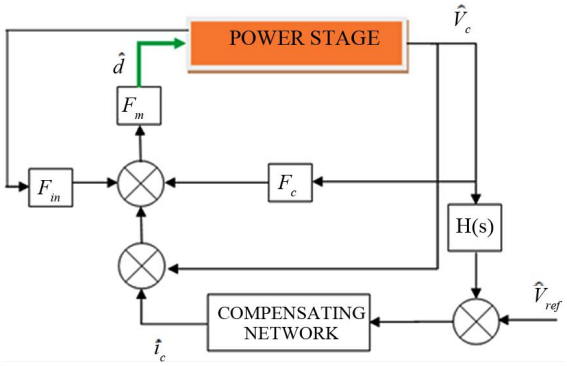

Figure 16. Block diagram of peak current mode control.

The method of PCMC modeling is the same as described in [10], only up and down slopes and their times have been replaced to adapt the formulation with proposed topology. So the model of **Figure 16** can be achieved, where F_m, F_{in} and F_c in boost and buck modes are determined in (26).

$$\tilde{d} = F_m\left[\tilde{i}_c - \tilde{i}_L - F_{in}\tilde{v}_{in} - F_c\tilde{v}_c\right]$$

$$\text{boost mode}\begin{cases} F_m = \dfrac{1}{M_a T_s} \\ F_{in} = \dfrac{(D-3/4)T_s}{L} \\ F_c = \dfrac{(1-D)^2 T_s}{nL} \end{cases} \qquad (26)$$

$$\text{buck mode}\begin{cases} F_m = \dfrac{1}{M_a T_s} \\ F_{in} = \dfrac{D^2 T_s}{nL} \\ F_c = \dfrac{(1/4-D)T_s}{L} \end{cases}$$

Not considering input voltage and load variations, the overall block diagram for both modes of operations can be depicted as **Figure 17** with some algebraic operations; the loop gain transfer function of (27) can be concluded.

$$\text{loop gain} = H(S)G_c(S)\frac{F_m G_{V_c d}}{1+\beta F_m G_{id} + F_m F_c G_{V_c d}} \qquad (27)$$

In order to examine the stability and design the converter's controller, boost and buck mode transfer functions can be replaced to achieve loop gain of each mode. With some algebraic operations one can get to (28) and (29) for boost and buck loop gain respectively. **Figure 18** shows the uncompensated and compensated loop gain of boost mode. Compensating network for boost mode operation is a

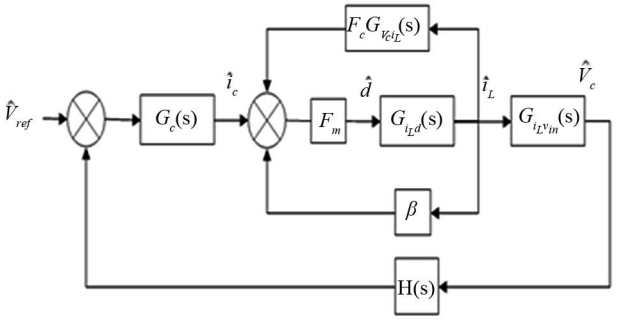

Figure 17. Simplified block diagram of closed loop converter with neglecting the effect of line and load variation.

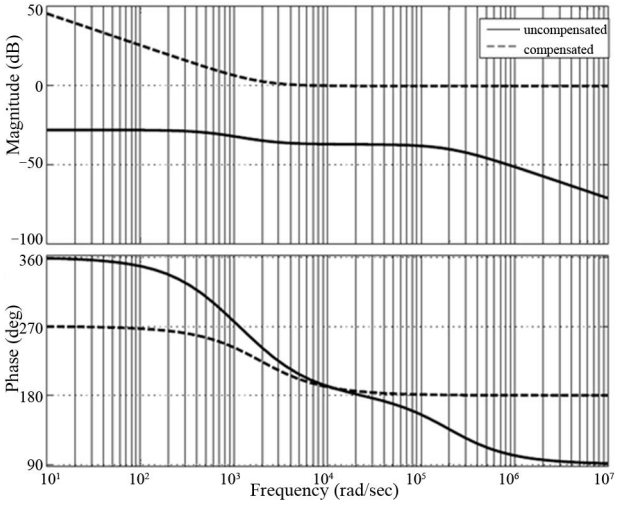

Figure 18. Uncompensated and compensated loop gain of boost mode solid line is uncompensated and dashed line is compensated response.

simple PID which its coefficients have been selected with respect to the method presented by Chien and Fruehauf [29].

$$T_{boost}(S)=\frac{G_c(S)F_mH(S)\left(-2nLI_LS+8(1-D)V_C-2nV_{IN}\right)}{den(S)}$$

$$den(S)=n^2CLS^2+\left(n^2\frac{L}{R}+2nC\beta F_{mV_C}-2nLI_LF_mF_c\right)S+4(1-D)^2+8(1-D)F_m\left[\beta I_L+F_cV_C\right]-2nF_mF_cV_{IN} \quad (28)$$

$$T_{buck}(S)=\frac{G_c(S)F_mH(S)\left[2nV_{IN}\right]}{den(S)}$$

$$den(S)=n^2CLS^2+\left(n^2\frac{L}{R}+2nC\beta F_mV_{IN}\right)S+2nF_m\left[\beta/R+F_c\right]V_{IN} \quad (29)$$

A simple integral controller can meet the requirements of buck mode compensating network. However, the designed controllers are not the optimum ones in terms of robustness. Other advanced control algorithms can be applied to this converter easily with the derived small signal model but that is beyond the scope of this work. **Figure 19** represents uncompensated and compensated loop gain of buck mode.

6. Simulation Results

In order to make sure that the designed controllers are capable of controlling the converter, they should be examined. In control loop additional blocks like duty cycle limiter are employed because at the start up there is no output voltage. This leads to 100% the duty cycle, as a result after some cycles; the circuit is gone to its steady state in which inductor and capacitor experience only a constant source and this is when they go under short and open circuit respectively. The other important block is compensating ramp which can overcome the unstable oscillation problem described in [10,22,30]. **Figures 20** and **21** show that the controllers are successful to control the converter in the presence of 1 A and 10 A step load change for boost and buck mode respectively.

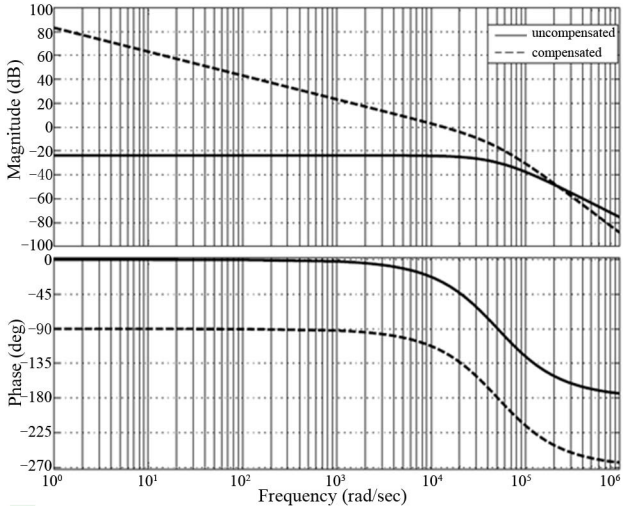

Figure 19. Uncompensated and compensated loop gain of buck mode, slid line is uncompensated and dashed line is compensated response.

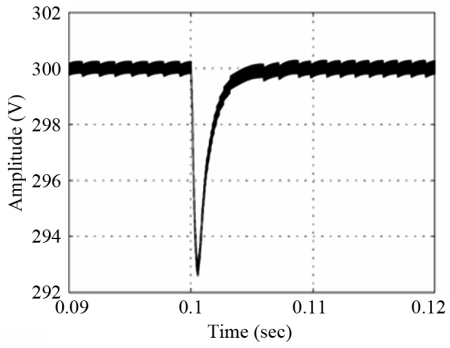

Figure 20. Response of compensated closed loop circuit in boost mode operation in the presence of 1 A step load change.

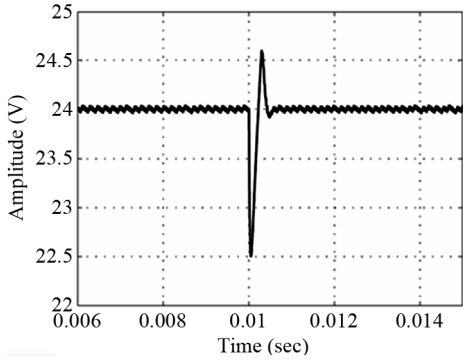

Figure 21. Response of compensated closed loop circuit in buck mode operation in the presence of 5 A step load change.

7. Conclusion

In this paper a bidirectional full bridge DC-DC converter as one of the most applicable industrial converters has been modeled with average state space method. Simulation results are in a close agreement with mathematical model which approve the successfulness of average state space to predict the response. Current programmed controller was designed for each mode. Although compensated network was effective in buck mode but employing modern and robust control algorithms can cope with the zero half plane problems in boost mode to achieve all the requirements such as more bandwidth, phase margin and capability of line and load change rejection.

REFERENCES

[1] T. Mishima, E. Hiraki, T. Tanaka and M. Nakaoka, "A New Soft-Switched Bidirectional DC-DC Converter Topology for Automotive High Voltage DC Bus Architectures," *IEEE Vehicle Power and Propulsion Conference*, Windsor, 6-8 September, 2006, pp. 1-6. doi:10.1109/VPPC.2006.364281

[2] A. E. Navarro, P. Perol, E. J. Dede and F. J. Hurtado, "A New Efficiency Low Mass Bidirectional Battery Discharger-Charger Regulator for Low Voltage Batteries", 27*th Annual IEEE Power Electronics Specialists Conference*, Baveno, 23-27 June 1996, pp. 842-845. doi:10.1109/PESC.1996.548679

[3] E.-S. Kim, K.-Y. Joe, H.-Y. Choi, Y.-H. Kim and Y.-H. Cho, "An Improved Soft Switching Bi-Directional PSPWM FB DC/DC Converter," *Proceedings of the* 24*th Annual Conference of Industrial Electronics Society*, Aachen, 31 August-4 September1998, pp. 740-743. doi:10.1109/IECON.1998.724185

[4] H. L. Chan, K. W. E. Cheng and D. Suatanto, "A Novel Square-Wave Converter with Bidirectional Power Flow," *Proceedings of the International Conference on Power Electronics and Drive Systems*, Hohg Kong, 27-29 July 1999, pp. 966-971. doi:10.1109/PEDS.1999.792839

[5] M. Jain, P. K. Jain and M. Daniele, "Analysis of A Bidirectional DC-DC Converter Topology for Low Power Application," *IEEE Canadian Conference on Electrical and Computer Engineering*, St. Johns, 25-28 May 1997, pp. 548-551. doi:10.1109/CCECE.1997.608283

[6] K. Venkatesan, "Current Mode Controlled Bideirectional Flyback Converter," 20*th Annual IEEE Power Electronics Specialists Conference*, Milwaukee, 26-29 June 1989, pp. 835-842. doi:10.1109/PESC.1989.48567

[7] T. Reimann, S. Szeponik, G. Berger and J. Petzoldt, "A Novel Control Principle of Bidirectional DC-DC Power Conversion," 28*th Annual IEEE Power Electronics Specialists Conference*, St. Louis, 22-27 June 1997, pp. 978-984. doi:10.1109/PESC.1997.616843

[8] M. K. Kazimierczuk, D. Q. Vuong, B. T. Nguyen and J. A. Weimer, "Topologies of Bidirectional PWM DC-DC Power Converter," *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, 24-28 May 1993, pp. 435-441. doi:10.1109/NAECON.1993.290953

[9] N. M. L. Tan, T. Abe and H. Akagi, "Topology and Application of Bidirectional Isolated DC-DC Converters," *IEEE* 8*th International Conference on Power Electronics and ECCE Asia*, Jeju, 30 May-3 June 2011, pp. 1039-1046. doi:10.1109/ICPE.2011.5944690

[10] R. W. Erickson and D. Maksimovic, "Fundamental of Power Electronics," 2nd Edition, Kluwer Academic Publishers, Alphen aan den Rijn, 2001.

[11] T. Mishima, E. Hiraki, T. Tanaka and M. Nakaoka, "High Frequency Link Symmetrical Active Edge Resonant Snubbers-Assisted ZCS-PWM DC-DC Converter," *Electric Power Applications*, Vol. 1, No. 6, 2007, pp. 907-914. doi:10.1049/iet-epa:20060508

[12] C. Zhao, S. D. Round and J. W. Kolar, "Full-Order Averaging Modeling of Zero-Voltage Switching Phase-Shift Bidirectional DC-DC Converters," *Power Electronics*, Vol. 3, No. 3, 2010, pp. 400-410. doi:10.1049/iet-pel.2008.0208

[13] F. Krismer and J. W. Kolar, "Accurate Small-Signal Model for the Digital Control of an Automotive Bidirectional Dual Active Bridge," *IEEE Transactions on Power Electronics*, Vol. 24, No. 12, 2009, pp. 2756-2768. doi:10.1109/TPEL.2009.2027904

[14] P. Jain and J. E. Quaicoe, "Generalized Modeling of Constant Frequency DC/DC Resonant Converter Topologies," 14*th International Telecommunications Energy Conference*, Washington DC, 4-8 October 1992, pp. 180-185. doi:10.1109/INTLEC.1992.268444

[15] L. A. Aguirre, P. F. Donoso-Garcia and R. Santos-Filho, "Use of a Priori Information in the Identification of Global Nonlinear Models—A Case Study Using a Buck Converter," *IEEE Transactions on Circuits and Systems I*: *Fundamental Theory and Applications*, Vol. 47, No. 7, 2000, pp. 1081-1085. doi:10.1109/81.855463

[16] K. T. Chau and C. C. Chan, "Nonlinear Identification of Power Electronics Systems," *Proceedings of International Conference on Power Electronics and Drive Systems*, Singapore, 21-24 February 1995, pp. 329-334. doi:10.1109/PEDS.1995.404900

[17] F. Alonge, F. D'Ippolito, F. M. Raimondi and S. Tumminaro, "Nonlinear Modeling of DC/DC Converters Using the Hammerstein's Approach," *IEEE Transactions on*

Power Electronics, Vol. 22, No. 4, 2007, pp. 1210-1221. doi:10.1109/TPEL.2007.900551

[18] F. Alonge, F. D'Ippolito and T. Cangemi, "Hammerstein Model-Based Robust Control of DC/DC Converters," 7*th International Conference on Power Electronics and Drive Systems*, Bangkok, 27-30 November 2007, pp. 754-762. doi:10.1109/PEDS.2007.4487788

[19] V. Vorperian, R. Tymerski and F. C. Lee, "Equivalent Circuit Model for Resonant and PWM Switches," *IEEE Transactions on Power Electronics*, Vol. 4, No. 2, 1989, pp. 205-214. doi:10.1109/63.24905

[20] V. Vorperian, "Simplified Analysis of PWM Converter Using the Model of the PWM Switch: part I and II," *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 26, No. 3, 1990, pp. 497-505. doi:10.1109/7.106127

[21] R. D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching Converter Power Stages," *International Journal of Electronics*, Vol. 42, No. 6, 1977, pp. 521-550. doi:10.1080/00207217708900678

[22] S.-P. Hsu, A. Brown, L. Rensink and R. D. Middle-Brook, "Modeling and Analysis of Switching DC-to-DC Converters in Constant-Frequency Current Programmed Mode", *Power Electronics Specialists Conference*, San Diego, 18-22 June 1979, pp. 284-301.

[23] S. Cuk, "Modeling, Analysis, and Design of Switching Converters," Ph.D. Thesis, California Institute of Technology, Pasadena, 1976.

[24] L. Zhu, "A Novel Soft-Commutating Isolated Boost Full-Bridge ZVS-PWM DC-DC Converter for Bidirectional High Power Applications," *IEEE Transactions on Power Electronics*, Vol. 21, No. 2, 2004, pp. 422-429. doi:10.1109/TPEL.2005.869730

[25] R. Li , A. Pottharst, N. Frohleke and J. Bocker, "Analysis and Design of Improved Isolated Full-Bridge Bidirectional DC-DC Converter," 35*th Annual Power Electronics Specialists Conference*, Aachen, 20-25 June 2004, pp. 521-526. doi:10.1109/PESC.2004.1355801

[26] R. B. Ridley, "A New, Continuous-Time Model for Current Mode Control," *IEEE Transactions on Power Electronics*, Vol. 6, No. 2, 1991, pp. 271-280. doi:10.1109/63.76813

[27] L. Peng and B. Lehman, "A Design Method for Paralleling Current Mode Controlled DC-DC Converters," *IEEE Transactions on Power Electronics*, Vol. 19, No. 3, 2004, pp 748-756. doi:10.1109/TPEL.2004.826497

[28] R. Sheehan, "Understanding and Applying Current-Mode Control Theory," *Power Electronics Technology Exhibition and Conference*, Dallas, 30 October-1 November,2007, pp. 1-26.

[29] D. E. Seborg, T. F. Edgar and D. A. Millichamp, "Process Dynamics and Control," 2nd Edition, John Wiley and Sons Inc., New York, 2004.

[30] L. Dixon, "Average Current Mode Control of Switching Power Supplies," *Unitrode Application Note*, No. 3, pp. 356-369.

