Scientific Research Publishing

Circuits and Systems, 2018, 9, 117-123
http://www.scirp.org/journal/cs
ISSN Online: 2153-1293
ISSN Print: 2153-1285

New Current Mode Lossy Integrator Employing CDDITA

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How to cite this paper: Panwar, K., Prasad, D., Srivastava, M. and Haseeb, Z. (2018) New Current Mode Lossy Integrator Employing CDDITA. *Circuits and Systems*, **9**, 117-123.
https://doi.org/10.4236/cs.2018.98012

Received: July 8, 2018
Accepted: August 10, 2018
Published: August 13, 2018

Abstract

This work presents a novel current-mode (CM) lossless integrator that uses one current differencing differential input transconductance amplifier (CDDITA) and one grounded capacitor. The configuration based on single active element has several advantages from the aspect of monolithic integration, few are: reduced power consumption, chip miniaturization. Employment of grounded capacitor is also beneficial for monolithic integration. Specifying some of the key features of integrator proposed are: 1) purely resistorless, 2) electronically tunable, 3) current output available at the port having high impedance, and 4) excellent performance under non-ideal conditions. So, a resister-less current mode lossy integrator with electronic control employing single CDDITA has been proposed in this paper. The verification of workability of the proposed current mode integrator is well explained by the help of SPICE simulations using TSMC CMOS 0.18 μm technology node.

Keywords

Current Differencing Differential Input Transconductance Amplifier, Lossy Integrator, Electronic Tunability, Grounded Capacitor

1. Introduction

Active RC Integrator is an extremely versatile circuit element that is employed in development and synthesis of numerous analog signal processing as well as generation circuits that include active filters, quadrature oscillators, waveform generators and many more. Various voltage or current mode integrator circuits based on traditional and modern active components has been proposed in literature. An OP-AMP based integrator was proposed in [1]. Some current conveyor (CCII) based integrator were proposed in [2] [3] [4] [5] [6]. Differential

voltage current conveyor (DVCC) was also proposed in literature [7]. Some integrator circuits employing modern active elements like current differential buffered amplifier (CDBA) [8], multiplication mode current conveyor (MMCC) [9], current controlled current differential buffered amplifier (CCCDBA) [10], differential difference current conveyor (DDCC) [11], current differential transconductance amplifier (CDTA) [12], current follower transconductance amplifier (CFTA) [13], CCCCTA [14] and current feedback operational amplifier (CFOA) [15] have been proposed in the literature available till date.

But the circuit configurations available with us possess few disadvantages like: 1) they uses greater than 1 active element, 2) greater than 1 passive element, 3) floating capacitors are used which increases chip area, 4) no electronic tenability, 5) matching constraint required, 6) poor non ideal performance, 7) exclusive current output at very high impedance terminal is unavailability (in case of CM integrator).

Hence, the goal of this manuscript is to remove disadvantages mentioned above, hence it possess following advantages:

1) Only one CDDITA is used;

2) Just one capacitor is used;

3) Realization is purely free of resistor;

4) Grounded capacitor used, reduces chip area;

5) Gain is electronically tunable;

6) Better performance in non ideal case;

7) Current output signal at high impedance port is available.

CDDITA is new generation ABB and its idea was proposed in [16]. It is an extension of CDTA which has been a popular ABB in last decade. The electrical symbol of CDDITA is shown in **Figure 1**. It has two virtually grounded low input impedance terminals P and N, two high impedance intermediate terminals Z and V and two high impedance output terminals X+ and X−.

The behavioral model of CDDITA is shown in **Figure 2**, which illustrates that input stage is a current differencing unit and the output stage is an OTA.

The voltage current relationships between different ports of CDDITA can be given by following equation set:

$$V_P = V_n = 0 \tag{1}$$

$$I_Z = \left(I_P - I_N\right) \tag{2}$$

$$I_{X+} = g_m\left(V_Z - V_V\right) \tag{3}$$

$$I_{X-} = -g_m\left(V_Z - V_V\right) \tag{4}$$

The CMOS realization of CDDITA has been shown in **Figure 3**.

The applications of CDDITA in analog signal processing/signal generation have been proposed in [17] [18].

2. Proposed Current-Mode Integrator

The circuit of lossy integrator proposed is shown in **Figure 4**.

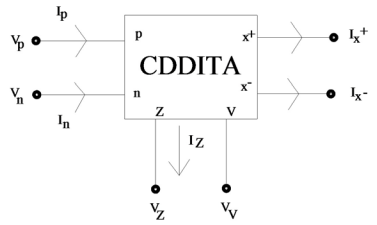

Figure 1. Block diagram of CDDITA.

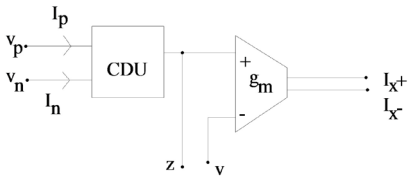

Figure 2. Behavioral model of CDDITA.

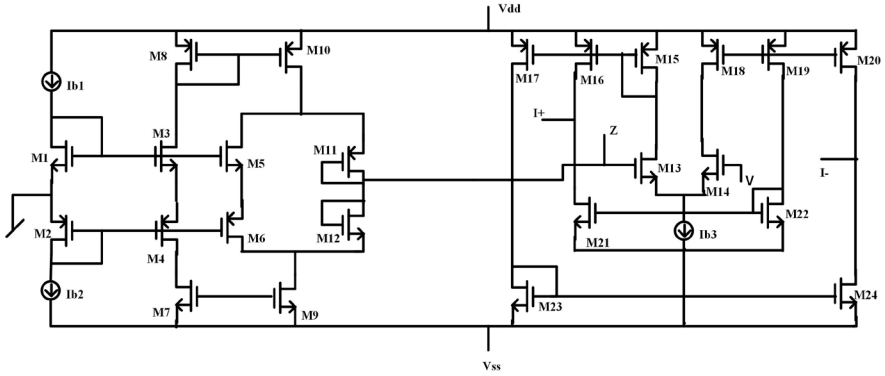

Figure 3. CMOS implementation of CDDITA.

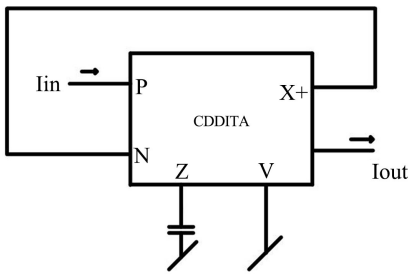

Figure 4. Proposed CM lossy Integrator.

Through proper analysis of circuit following expression is yielded the for output current;

$$\frac{I_{out}}{I_{in}} = \frac{1}{1+\frac{sC}{g_m}} \tag{5}$$

From Equation (5), it becomes clear that the gain of proposed integrator can be tuned electronically by g_{mi}, which is adjusted by bias currents of CDDITA. Output current "I_{out}" is explicitly available at high impedance "X−" port is shown

in Figure 3. Hence, there is no additional need of follower is to use this output.

3. Non-Ideal Analysis and Sensitivity Calculations

Under non-ideal condition the CDDITA is defined by following equations of VDTA modified as

$$I_Z = \left(\alpha_p I_P - \alpha_n I_N\right) \tag{6}$$

$$I_{X+} = \beta_+ g_m \left(V_Z - V_V\right) \tag{7}$$

$$I_{X-} = -\beta_- g_m \left(V_Z - V_V\right) \tag{8}$$

where "β_+" and "β_-" are the trans-conductance error gains and "α_p" and "α_n" are errors in current transfer. These values are just slightly less than that of unity.

The current output transfer function of the presented paper under the influence of ideal conditions is given as

$$\frac{I_{out}}{I_{in}} = \frac{1}{\frac{\alpha_n \beta_+}{\alpha_p \beta_-} + \frac{sC}{g_m \alpha_p \beta_-}} \tag{9}$$

It is clear from Equation (9) that even; the proposed configuration has an ability to simulate an ideal CM integrator under the non-ideal conditions, with adjustable tunable gain. So, the nature of presented circuit remains unaffected in the non-ideal conditions.

4. Simulation Results

The presented circuit is verifying by simulating it by employing CMOS CDDITA (shown in Figure 3) with ±3 V DC supply voltage. All the biasing currents of CDDITA are chosen as 100 μA and the value of capacitor "C" is selected as 0.1 nF. To study the input output relation a rectangular input current signal (shown in Figure 5) of ±0.5 mA is used. The output current (I_{out}) is shown in Figure 6.

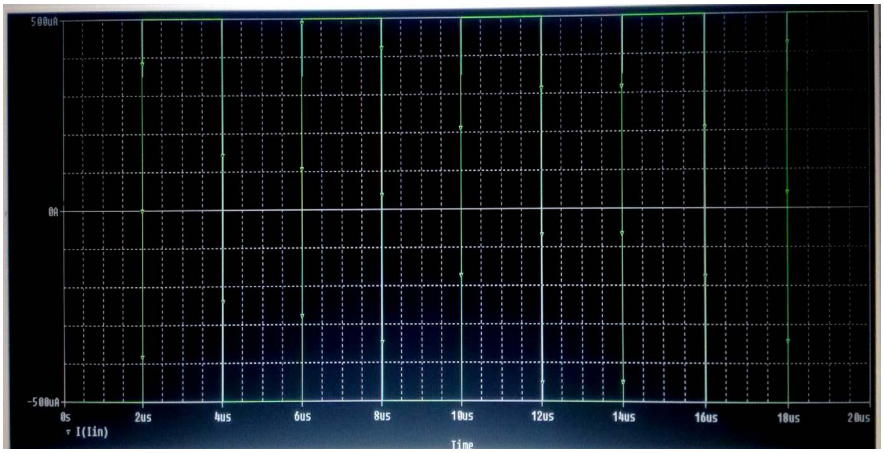

Figure 5. Input rectangular current pulse of amplitude ±0.5 mA and duration 4 μs (Iinput).

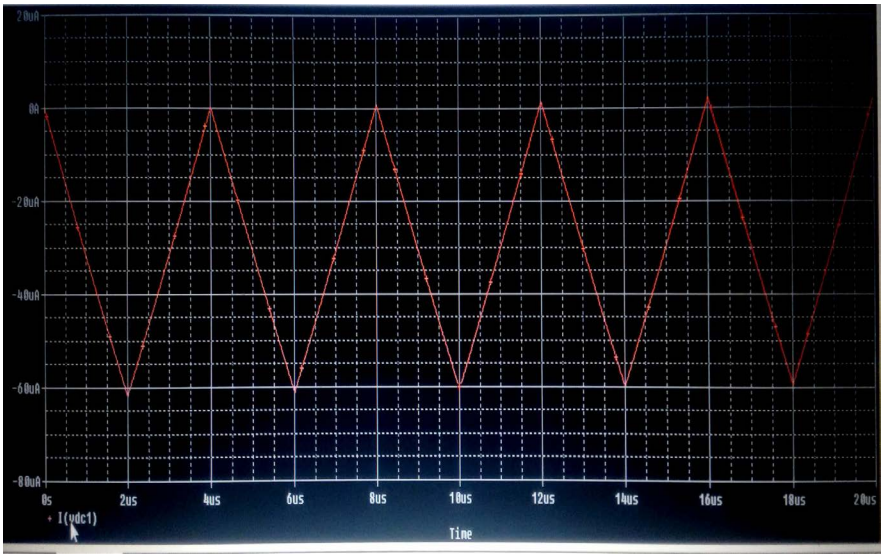

Figure 6. Output triangular current pulse (Ioutput).

5. Conclusion

A CDDITA based current mode lossy integrator circuit that uses single CDDITA and grounded capacitor has been presented in this manuscript. The proposed circuit has following features: no requirement of any resistor, electronically controllable gain and explicit current mode (CM) output at a high impedance port that is suitable for cascading and no requirement of component matching constraint. The designed circuit configuration shows good non-ideal behavior and even in that conditions the circuit can simulate a lossless CM integrator. The analysis has been successfully verified by PSPICE simulation using TSMC CMOS of 0.18 μm process parameters. For simulation purpose CMOS CDDITA has been used with biasing current of 100 μA and supply voltage of ±3 V DC.

Acknowledgements

This research is supported by the "Young Faculty Research Fellowship and Research/Contingency Grant" to Jamia Millia Islamia, under "Visvesvaraya PhD Scheme for Electronics and IT" in 2015-16.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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Nomenclature

V_P: Voltage at "P" terminal
V_N: Voltage at "N" terminal
V_Z: Voltage at "Z" terminal
V_V: Voltage at "V" terminal
I_P: Current at "P" terminal
I_N: Current at "N" terminal
I_Z: Current at "Z" terminal
I_{in}: Input current
I_{out}: Output current
g_m: Transconductance of CDDITA
α, β: Current gain errors