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THD Analysis of Cascaded H-Bridge Inverter with Fuzzy Logic Controller

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Abstract

In recent days, the multilevel inverter technology is widely applied to domestic and industrial applications for medium voltage conversion. But, the power quality issues of the multilevel inverter limit the usage of much sensitive equipment like medical instruments. The lower distortion level of the output voltage and current can generate a quality sinusoidal output voltage in inverters and they can be used for many applications. The harmonics can cause major problems in equipments due to the nonlinear loads connected with the power system. So, it is necessary to minimize the losses to raise its overall efficiency. In this paper, a new topology of seven level asymmetrical cascaded H-bridge multilevel inverter with a Fuzzy logic controller had been implemented to reduce the Total Harmonic Distortion (THD) and to improve the overall performance of the inverter. The proposed model is well suited for use with a solar PV application. In this topology, only six IGBT switches are used with three different voltage ratings of PV modules (1:2:4). The lower number of semiconductor switches leads to minimizing overall di/dt ratings and voltage stress on each switches and switching losses. The gate pulses generated by Sinusoidal Pulse Width Modulation (SPWM) technique with a Fuzzy logic controller are also introduced. A buck-boost converter is used to maintain the constant PV voltage level integrated by an MPPT technique followed by Perturb and Observer algorithm is also implemented. The MPPT is used to harness the maximum power of solar radiations under its various climatic conditions. The new topology is evaluated by a Matlab/Simulink model and compared with a hardware model. The results proved that the THD achieved by this topology is 1.66% and realized that it meets the IEEE harmonic standards.

Keywords

Cascaded H-Bridge Multilevel Inverter, THD, Photo Voltaic Modules, SPWM, Fuzzy Logic Controller, MPPT Technique

1. Introduction

Recently, the multilevel inverters are getting more popular among the industrial and domestic applications. Since, it has many advantages such as low voltage stress on operating switches with high di/dt ratings, and lower harmonic distortion level. For the optimum operation of power system equipments connected with nonlinear loads, it is necessary to keep the inverter output voltage and current waveform as close as possible to the sinusoidal. These inverter topologies can produce a synthesized ac output at any desired level. A stair case waveform with reduced harmonic distortion of an output voltage can be generated by increasing the number of levels in the inverter. But, the number of levels leads to the complexity in control which produces the problem of voltage imbalances. So, they require continuous improvements in their features, such as they could have the higher efficiency, high power density, reduction and control of total harmonic distortion on voltage and current. The conventional inverters have some disadvantages such as high di/dt rating, voltage stress on switches etc. In general, three different topologies of multilevel inverters are suggested: neutral clamped or diode clamped, flying capacitor and cascaded multi cell with different dc link voltage sources [1]. The maintaining of voltage and current at the output of the inverter at its rated rms value and negligible quantity of total harmonics can produce a quality power. Many electronic equipments produce unwanted harmonics and disturbances like voltage sag and swell, Electromagnetic Interference (EMI) at the distribution system. So, in order to overcome these issues, it requires a more sophisticated approach.

A cascaded H-bridge inverter produces stepped AC voltage wave form with reduced harmonics at higher levels by linking different ratings of DC voltage sources. The inverter filter circuit elements required is less when increasing the number of levels in the inverter. Thus, a shaped voltage wave form, reduced switching volume, very low THD and reduced cost of the system is obtained. The voltage sources on the DC side of the converter make multilevel technology as an attractive for photovoltaic applications. In the conventional H-bridge multilevel inverters, the THD is normally high and the resultant output is low while comparing with the proposed inverter topology. In general, it is observed that the THD is reduced by increasing the number of output levels [2].

A solar energy is a most assured renewable power and it is available plenty in nature. Many countries are suffered by the huge power demand due to the rapid development of the technological requirements. Therefore, a modern approach is necessary to meet the energy gap. Also, the conventional power generating methods cause many climatic and environmental problems like global warming, acid raining and abnormal climatic conditions etc. The issues involved in the control of Co2 emission is becoming a huge challenge for many countries. To meet these challenges, many countries concluded that to adopt energy conservation methods and it is necessary to shift over to an alternative energy sources. Therefore, the solar energy is most preferred among the renewable power

sources such as wind, tidal and bio-mass. Solar energy is free from pollution and noiseless, inexhaustible when compared to other conventional energy sources. The Photo Voltaic cells are utilized to convert the solar lights in to electricity. The arrangement PV cells in parallel or series combination can generate a desired power level at the output. The PV solar power system has high reliability and long life span. Hence, in our proposed technology, three different voltage ratings of PV modules are considered to implement the topology.

The solar power conversion system has an issue with the variation of output voltage from the PV modules at different climatic conditions of sun during the day time. So, an MPPT controller is provided for harnessing the maximum solar energy at various solar radiation levels. Perturb and observer algorithm is implemented to get the maximum power through MPPT [3]. The output of the MPPT is given to the Buck-boost converter to keep the constant dc voltage level to the inverter input. In this paper, a proposed model of single-phase asymmetrical cascaded H-bridge multilevel inverter for a PV system is implemented with an MPPT array and a fuzzy logic controller.

2. Cascaded H-Bridge Multi-Level Inverter (CHBMLI)

Construction and Operation

A cascaded multilevel inverter is broadly considered for the PV power conversion system. It is the combination many H-bridge modules with its each output voltage are connected in series. A general structure of an H-bridge module with a separate dc source is shown in Figure 1. It consists of four semiconductor switches such as Sw1, Sw2, Sw3 and Sw4, four diodes with a single dc source.

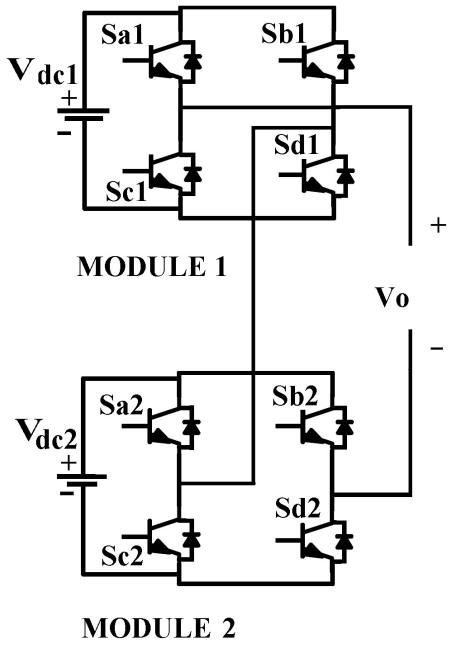

Figure 1. Structure of a H-bridge module with separate dc sources.

Any number of H-bridge modules can be connected to obtain a desired output voltage level of the cascaded inverter. The voltage sources connected with each H-bridge module can be replaced by any dc voltage source such as a battery, PV cells, fuel cells etc., Each H-bridge module can generate three different output voltage levels of +Vdc, 0 and −Vdc.

In order to obtain three levels of output voltages, the switches can be operated in three different sequences [4] [5]. In mode 1; +Vdc is produced with the switches Sa1 and Sd1 are turned on and mode 2; −Vdc is obtained with the switches Sb1, Sc1 are turned on and in mode 3; Sa1, Sd1 and Sb1, Sc1 are turned on to produce zero voltage at the output. The voltage at the output is defined by $M = 2s + 1$ and "s" is denoted by number of dc sources. In this structure, a faulty module can be replaced without affecting the rest of the structure. The each output of the module is connected in series to get the desired voltage level of the multilevel inverter. Series connection provides the resultant output of the inverter. So, the number of switches used for this structure is lowest while comparing with the conventional multilevel inverter. It can generate the waveform almost closer to sinusoidal. The complexity in control circuit, switching losses, size of the module by the least count of the switching components, requirement of gating circuits are also reduced while comparing with the conventional multilevel inverters [6].

Thus, asymmetric cascaded multilevel inverter topology significantly increases the number of levels in output voltage for the same number of control switches. The sequence of operation of each mode of operation is shown in Figure 2.

The output waveform generated 11-level cascaded multilevel inverter by summing up of H-bridge is shown in Figure 3. Each H-bridge topology produces a quasi-square waveform by phase shifting their positive and negative phase legs with a determined switching timing. The output voltage V_o (V_p) is generated

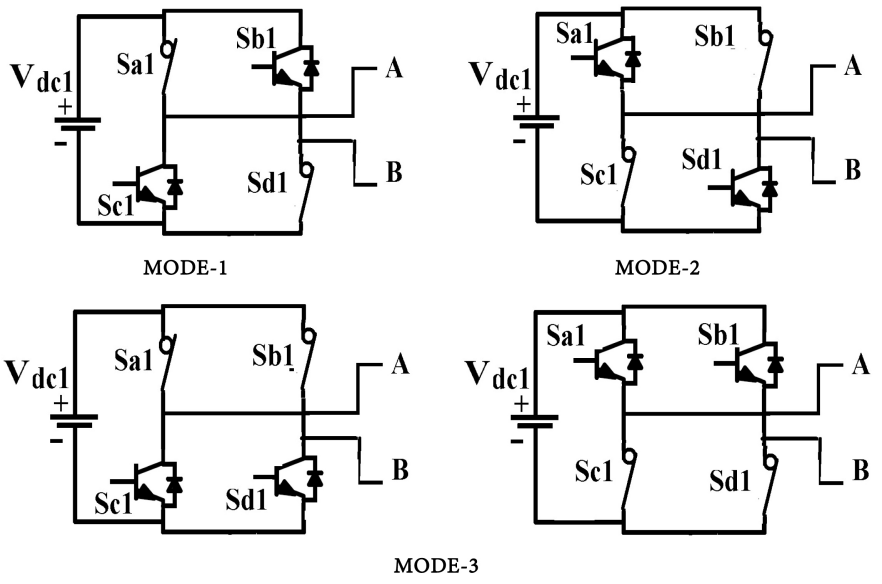

Figure 2. Three modes of operation of CHBMLI.

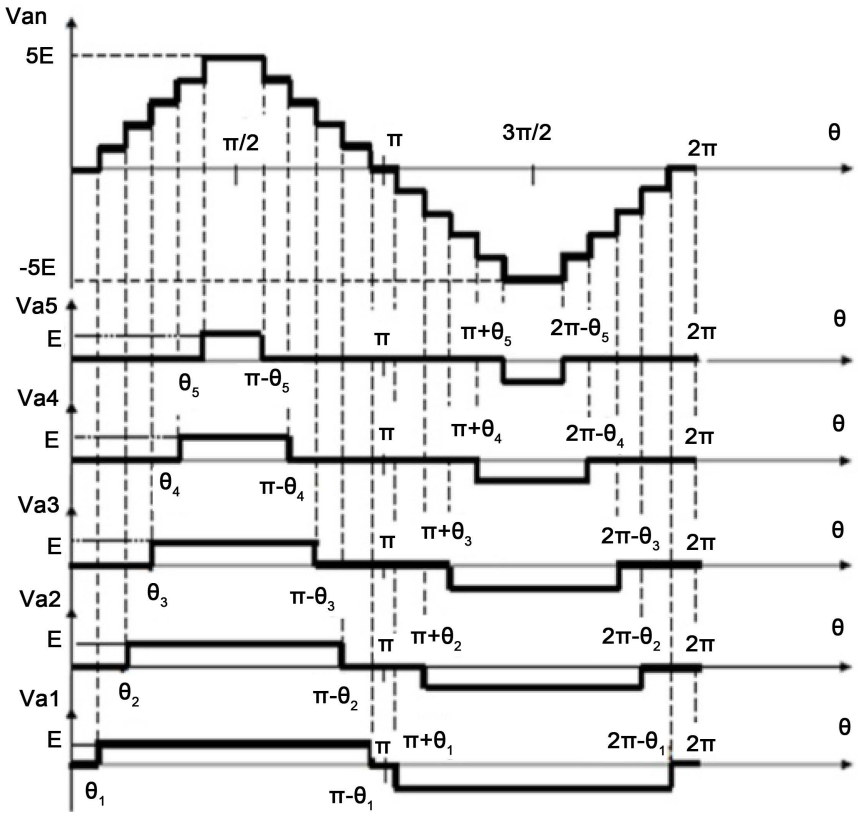

Figure 3. Output waveform generated 11-level cascaded multilevel inverter.

by the summing up of output voltage in each inverter module for various duty cycles. Hence, the voltage of the inverter output is practically sinusoidal. If the number of H-bridge in a single-phase module is greater; then the output voltage Vo would be almost closer to the ac sinusoidal waveform [7]. Thus, the output voltage for an 11-level cascaded H-bridge multilevel inverter is obtained.

3. Modulation Strategies of CHBMLI

A several types of modulation techniques have been implemented for multilevel inverters to synthesize a desired output voltage levels. They are generally classified in to three categories.

1) Space vector modulation (SVPWM) technique

2) Carrier based PWM (sine-triangle PWM or SPWM)

3) Selective harmonic elimination (SHE).

But above the all, only the SVPWM and SPWM are often used. The SVPWM has more complexity in control when the number of level increased is more than five. So the SPWM scheme is almost preferred [8]. Multilevel Carrier based PWM has more than one triangular wave or saw tooth wave form and so on. The modulating or reference signal in carrier based PWM can be sinusoidal or trapezoidal. So, the SPWM scheme is most convenient and is easy to implement.

The principle of SPWM is to provide several triangular carrier signals by keeping only one modulating sinusoidal signal. Equation (2) is given for an

m-level inverter; the $(m-1)$ triangular carriers are required to set the amplitude value and frequency.

The carrier frequency f_c has the same peak-to-peak amplitude A_C. The modulating signals are sinusoidal frequency f_m and amplitude Am. At each instant; each carrier signal is compared with the modulating signal. For all comparisons, the switches are switched "on" if the modulating signal is greater than the triangular carrier designated to that switch. Figure 4 shows the phase opposition and disposition of PWM.

The switching states of the proposed inverter are also given in Table 1.

The main factors of the modulation process are the frequency ratio $k = f_c/f_m$, where, fm is the frequency of the modulating signal and f_c is the carrier frequency. The term Modulation Index (δ) can be realized from the Equation (1) and is given by

$$\delta = A_{ms}/(n * Acs) \tag{1}$$

where, "A_{ms}" denotes the amplitude of the modulating signal and A_c is the peak-to-peak value of carrier signal.

$$n = (n-1)/2 \tag{2}$$

"k" refers the number of levels (odd).

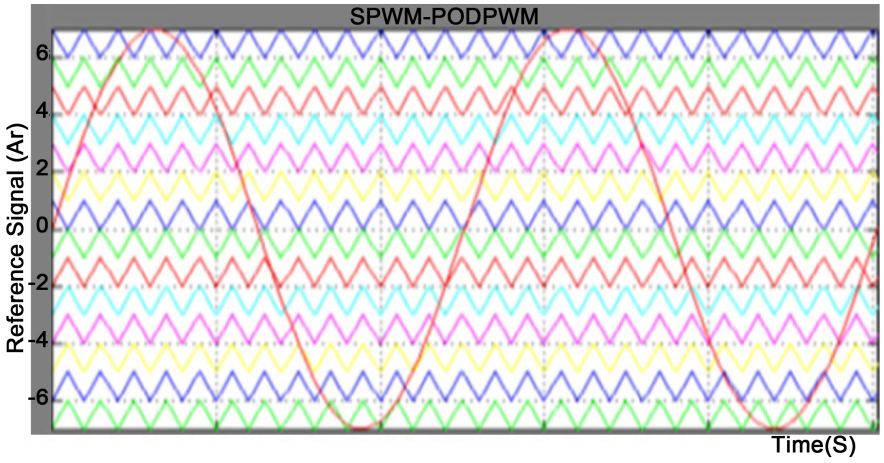

Figure 4. Phase opposition disposition PWM.

Table 1. Switching scheme of the proposed seven level inverter.

S. No	S1	S2	S3	S4	S5	S6	Output voltage
1	0	0	1	0	1	0	+Vdc
2	0	1	0	0	1	0	+2Vdc
3	1	0	0	0	1	0	+3Vdc
4	0	0	0	0	0	1	0
5	1	0	0	1	0	0	−Vdc
6	0	1	0	1	0	0	−2Vdc
7	0	0	1	1	0	0	−3Vdc

3.1. Fuzzy Logic Controller

The Fuzzy logic controller is developed for the proposed model by using non-mathematical solution based algorithms that can be used operator experience. This method is most appropriate for a non-linear system. Figure 5 shows the block diagram for FLC of the proposed inverter. The gate signals are generated by SPWM technique. The seven level cascaded inverter output is fed to the load through LC filter in order to produce sinusoidal voltage (V_o) which is compared with the reference voltage (desired voltage- V_{ref}) to generate error signal (e_n) and so the input to the FL controller is e_n. The subscript n refers sampling instances. The output of the FL controller *i.e.*, the compensating signal (C_s) is included with the reference signal to produce the required modulating signal (m_g) which is used to generate the gate pulses. As a result, a voltage feedback loop is established to obtain the required sinusoidal voltage at the output. Here a number of steps are followed to obtain fuzzy control surface for non-linear, complex dynamic and time varying systems. The inputs to the FLC are the error $e_n = V_{ref} - V_o$ and the change in error $c_e = e_n - (e_n - 1)$. The actual output voltage of the inverter is V_o, the desired output voltage V_{ref} and $e_n - 1$ is the previous error. The compensating signal C_s is inferred by the FLC. The updated modulating signal m_g is obtained by using C_s and fed to SPWM generator which provides a suitable PWM signals.

3.2. Buck-Boost Converter and MPPT Method

The Buck-Boost converter consists of two different states 1) on state, the switch S is closed, the inductor current increases and 2) off state, the switch is open the inductor current flows through the fly back diode D, the capacitor C and load R. This can lead to transfer the energy to the capacitor during the on-state. The circuit diagram of boost converter is shown in Figure 6. The current through the inductor (I_L) never falls to zero when the converter operates in continuous mode. In a few cases, the sum of energy needed for the load is sufficient to be transferred at a time is lesser than the total switching time.

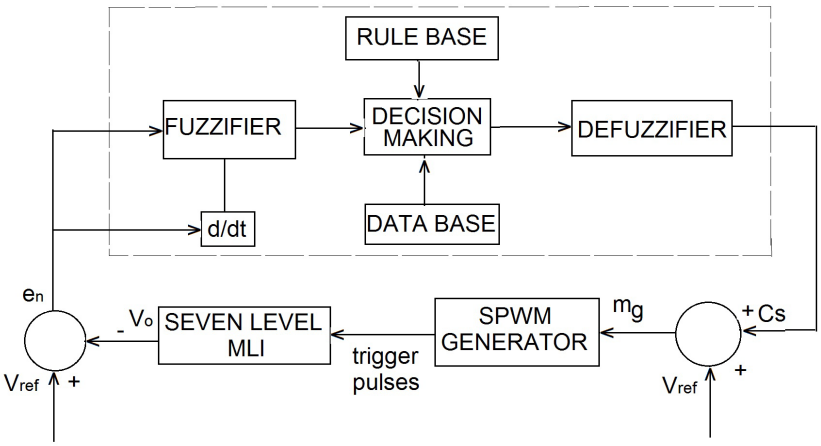

Figure 5. Block diagram of MLI with fuzzy logic controller.

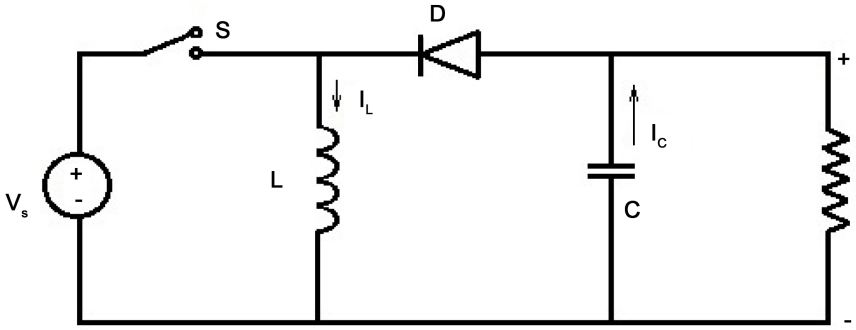

Figure 6. Buck-boost converter.

Here, the current flow through the inductor falls to zero during a part of the period and the converter is assumed to be operated in discontinuous mode. At the end of commutation cycle the inductor is entirely discharged.

The MPPT method can be suitably implemented with the help of an algorithm by means of the voltage-power characteristics of the PV modules. The power is reduced or increased by knowing the right and left of the maximum power point by increasing or decreasing the duty cycle. A change in duty cycle of the converter depends on, a most recent change in power. To perform the Perturb and Observer method, U is the power wanted to be read at a time when the voltage is obtained, then the term (U + I) is the power in time. The MPPT algorithm executed for this scheme is used to arrange the necessary adjustment in the buck-boost converter's duty cycle to obtain the optimum voltage. Hence, it allows the maximum power supplied to the load.

4. Proposed Topology of Seven Level CHBMLI

A new topology of a seven level asymmetric cascaded H-bridge multilevel inverter (ACHMLI) with six switches is proposed here. The low and medium power industrial and domestic gadgets are experiencing many serious power quality issues. The harmonic level of many inverter output are not able to meet the IEEE harmonics standard. By increasing the number of levels in the output of multilevel inverters, the output is also more step levels of staircase waveform, which has a reduced harmonic distortion. If the number of level of output voltage increases, then the number of switches also increased. This phenomenon leads to the complexity in control circuits.

The multilevel inverter is able to produce an output voltage with reduced harmonic distortion and lower electromagnetic interference. Therefore by considering these facts which are affecting the harmonic standards, a new topology of a seven level asymmetric cascaded H-bridge multilevel inverter (ACHMLI) with six switches is proposed here.

The output voltage presents, less harmonic content and produced a sinusoidal voltage. It is realized that the number of power semiconductors required for an inverter is increased then the inverter circuit size is also increased and hence the complexity of control circuit is also increased. The power consumption is also

more and thereby increased in overall system cost [8] [9]. The proposed model is designed by means of one H-bridge and two switches were connected with two flywheel diodes as shown in the Figure 7. Given that the number of switches is minimized for a seven level output of the proposed PV inverter, the gate driver circuit and space required is also reduced.

5. Simulation and Experimental Results

The proposed 7 level ACHBMLI was simulated by using MATLAB/Simulink tool box. The results were compared with a proto type experimental model. A hardware model of the proposed asymmetric inverter topology consists of three different voltage ratings of PV modules, buck-boost converter with an MPPT controller, cascaded H-bridge module and an IGBT driver circuit with a FLC controller. Also, it provides a better output power quality, which is most suitable for the application of PV fed inverter. Figure 8 shows the simulation model of ACHBMLI. The various intensity of sunlight provides uneven input voltage to the buck-boost converter and the dc/dc converter regulates a constant output voltage from the different voltage ratings (1:2:4) of PV modules. The proposed multilevel inverter further converted to AC, which can be used to feed the non-linear loads.

In this setup, there are six IGBT switches used instead of nine and seven

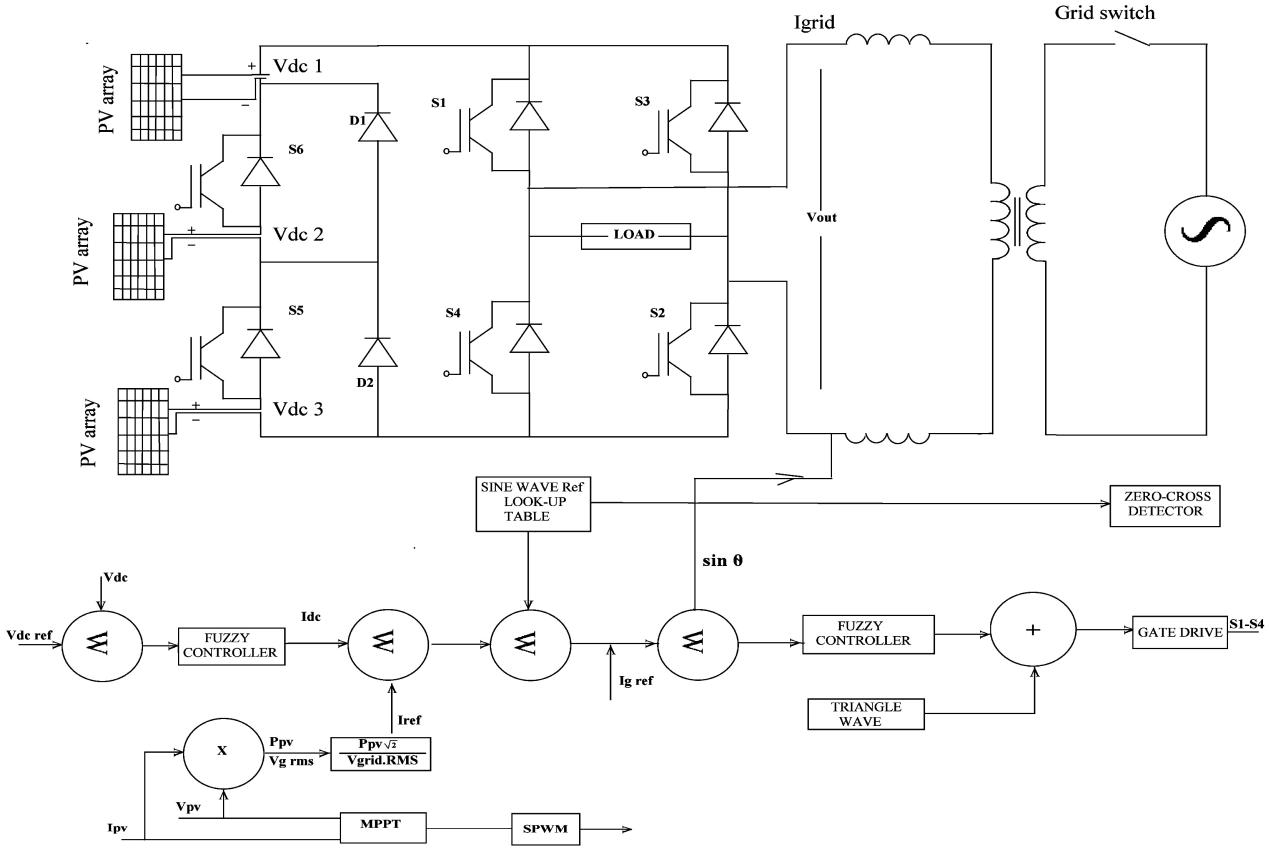

Figure 7. Proposed asymmetrical cascaded multilevel inverter topology.

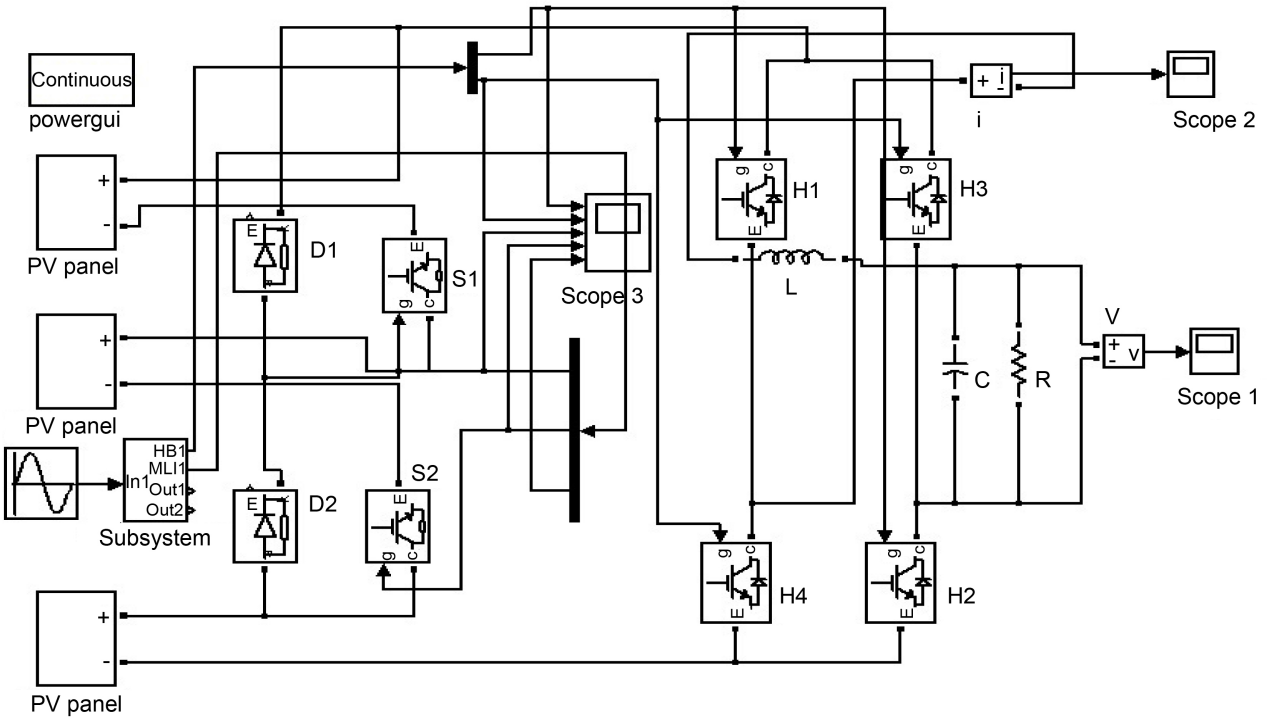

Figure 8. Simulation model of ACHBMLI.

switches in the existing topology for producing the same output voltage level. Pulses are generated by the driver circuit according to the voltage analyzed from the output voltage reference block. The voltage is generated due to the light intensities on the surface of the PV panel. Simulations have been conducted using SPWM method by comparing a reference signal as sine wave and carrier signal as triangular wave with fuzzy logic control. Harmonic analysis also done using FFT window in MATLAB/SIMULINK.

The uniform step output voltage waveforms of seven level inverter obtained by both simulation and from experimental model are shown in **Figure 9** and **Figure 10** respectively. From the results, it shows that the THD of current and voltage harmonics thus obtained by six switches produce 14.38% with R load and 1.66% with RL load which is shown in **Figure 11**.

The different values of the inverter design are also given in **Table 2**.

Hence, the harmonics produced at the output have the lowest THD and it offers good performance of the system. The odd harmonics are found appropriately less and it is almost reduced and satisfies the IEEE 1952-519 standard of harmonics.

6. Conclusion

In this paper a new topology of ACHBMLI is presented with a fuzzy logic controller based SPWM technique and an MPPT controller is implemented for PV on-grid systems with least count of switches. It is realized that the result obtained by the fuzzy logic controller, produced less percentage of THD when

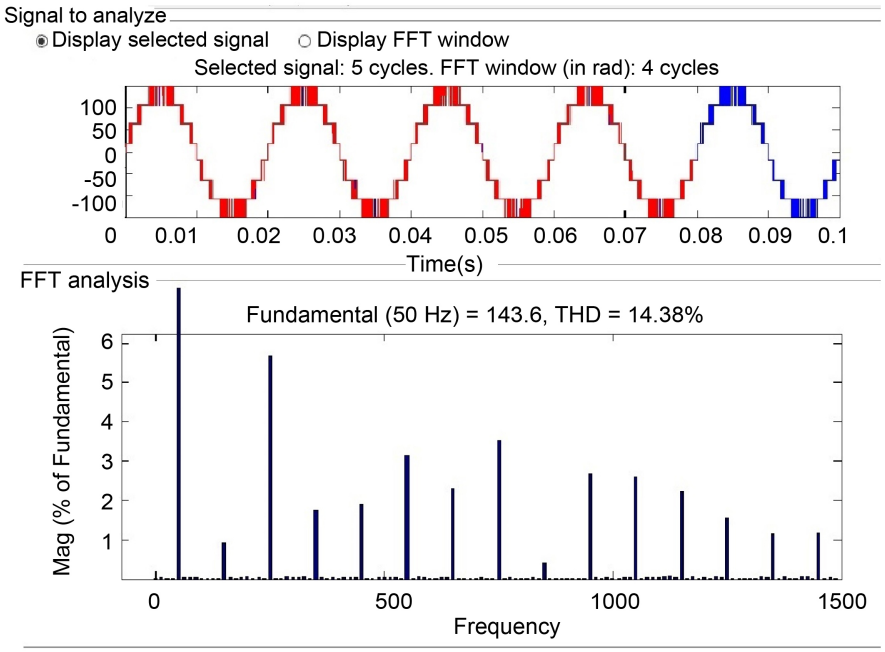

Figure 9. Seven level output voltage waveform of simulation model.

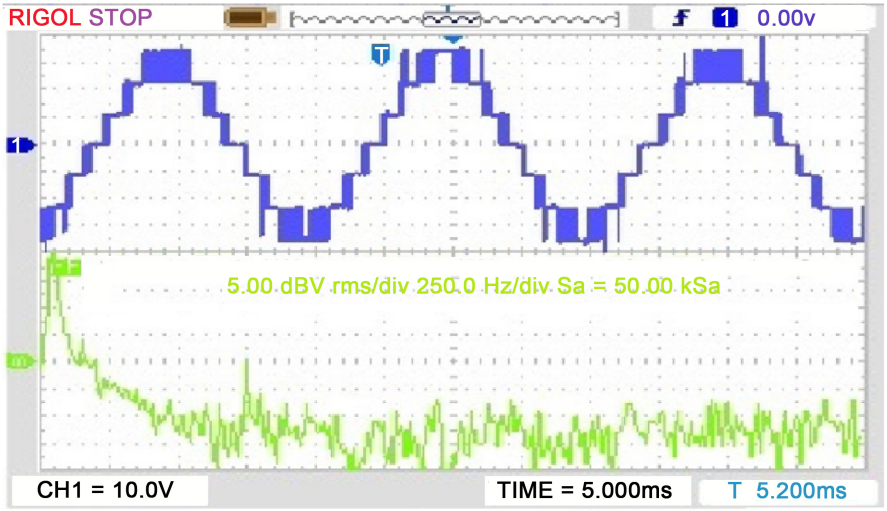

Figure 10. Seven level output of seven level experimental model.

compared with the conventional modulations techniques as revealed in the literatures. So, the proposed topology produced an improved output quality with a THD of 1.66%, which is comparatively low. The current distortion is greatly minimized after the harmonic reduction. The simulation and experimental results proved that the THD obtained is minimum and limited to meet the IEEE 519 - 1992 standard [10] [11] [12]. Thus, the use of different voltage ratings of PV module is recommended for the proposed asymmetric inverter with less number of switches. The overall cost of the proposed model is also reduced. So, the quality of the improved output voltage provides an improved efficiency which is suitable for PV fed inverter. The developed model is widely applicable in PV

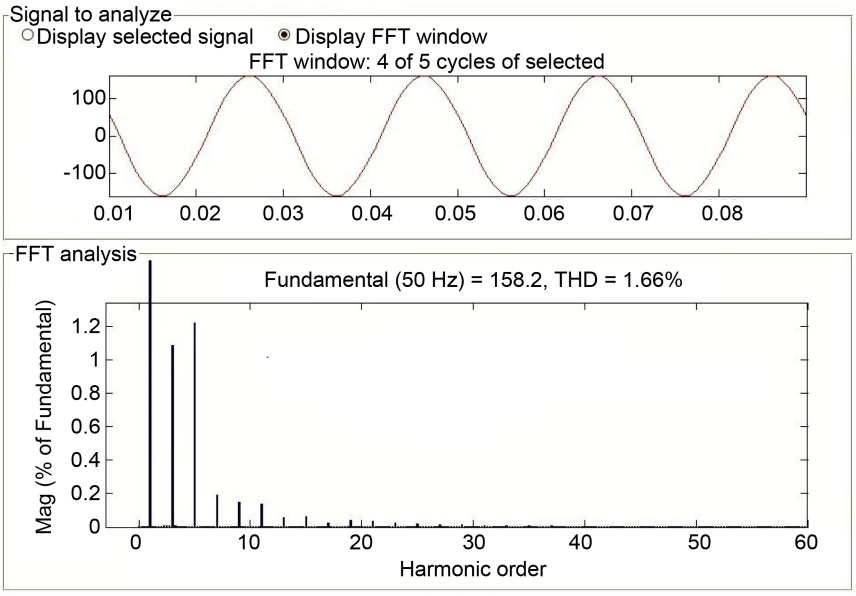

Figure 11. FFT analysis of proposed 7-level inverter with RL load.

Table 2. Specification of the proposed seven level inverter.

S. No	Parameter	Values in units
1.	voltage ratings of PV modules	21 v, 42 v, 84 v
2.	Switching frequency	2 KHz
3.	Output voltage-AC	143.6 V
4.	Output Frequency	50 Hz
5.	Output current	1.5 Amps
6.	Load resistance	100 Ω
7.	Inductor	0.6 mH
8.	Capacitor	10 μF

systems having asymmetric voltage ratings.

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