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FPGA SoC Based Multichannel Data Acquisition System with Network Control Module

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Abstract

Normally, Data acquisition (DAQ) is used to acquire the signals from different devices like sensors, transducers, actuators etc. The data acquisition is also used to analyze the signals, digitizing the signals and acquiring the signals from different inputs. The main drawbacks in data acquisition system are data storage, hardware size and remote monitoring. The System-on-Chip Field Programmable Gate Array (SoC-FPGA) is used in the proposed system in the aim to reduce the hardware and memory size. Further to provide remote monitoring with Ethernet/Wi-Fi, the Network Control Module (NCM) is integrated with Data acquisition and processing module for the communication between the systems. This developed system achieves high resolution with memory reduction, reduced hardware size, fast remote monitoring and control. It is used for real time processing in DAQ and signal processing. For fault tolerance and portability, the full system reconfigurability based FPGA acts as the best solution and the system can be reused with different configurations. The control of data acquisition and the subsequent management of data are coded in LabVIEW. LabVIEW tool is used to design and develop a four-channel Data Acquisition and Processing (DAQP) unit. National Instruments Data Acquisition (NIDAQ) and National Instruments Field Programmable Gate Array (NIFPGA) are used to test and implement the design for real time processing. This is designed to provide high accuracy, storage and portability.

Keywords

DAQ, Real Time Monitoring, SoC FPGA, Multichannel & Data Storage

1. Introduction

The data acquisition and processing system has many applications in measurement and control systems. The main work in data acquisition is to measure an

electrical phenomenon such as voltage, current, temperature, pressure or sound. The DAQ system is the process used to acquire the signals from different inputs, digitize the signals and analyze the signals. The interface can be done between the computer and outside world with the help of the DAQ hardware devices. In this work, a low-cost real-time application based on multi-channel Analog Signal Acquisition and Processing (ASAP) system is presented.

A temperature remote monitoring embedded system platform is designed [1] and the embedded microprocessor AT91SAM7X256 is used as CPU of the system. The system platform can be applied to certain equipment's of the power system, intelligent agriculture remote monitoring, intelligent furniture monitoring [2], intelligent warehouse monitoring and so on. The temperature measurement accuracy is within 0.5˚C. The system is reliable and stable and there are no communication failures. So it has very good social prospects but the data transfer rate does not meet the real time requirements.

System-on-Chip (SoC) [3] is used to increase performance and overcome costs during equipment monitoring. Nowadays industry pays much attention to prevent failures that may interrupt production with severe consequences in cost, product quality, and safety. The work here presented the design and implementation of a low-cost SoC design that utilizes reconfigurable hardware and a customized embedded processor [4] for time-frequency analysis on industrial equipment through short-time Fourier transform and discrete wavelet transform [5]. Analog-to-Digital Converter (ADC) simultaneously converts two channels. The ADC provides optimal combination of low cost, low power and high performance [6]. The presented results indicate and clearly demonstrate the potential of the architecture. However, due to the aforementioned conservative design, layout and verification techniques that were used, significant opportunities for circuit and layout optimization with associated reductions in power and large area exist.

Conventional rigid and general purpose on-chip network occupy significant logic and wire resources in Field Programmable Gate Arrays (FPGAs) [7]. To reduce the area cost, the authors presented a topology customization technique that interconnects the on-demand network which is systematically established in reconfigurable hardware. Experiments with practical applications show that the custom crossbar occupies significantly less area, maintaining higher performance and reduced power consumption, when compared with the general-purpose crossbars. In addition, the authors presented improvement in the configuration performance and cost by reducing the functional area cost in FPGAs. The presented customized NoC is implemented in FPGA and the results indicate that the area is reduced by 66%, when compared to the general-purpose networks.

Several practical applications required high-speed shortest-path computations. In many situations, especially in embedded applications, a FPGA based accelerator for computing the shortest paths can help to achieve high performance at low cost [8]. The proposed architecture is based on the Bellman-Ford algorithm adapted to facilitate early termination of computation. It has been

shown that the implementation on a Xilinx Virtex is more than twice as fast as a software implementation of the algorithm on a high-end general-purpose processor that runs at an order-of-magnitude faster clock. The speed-up offered by the design can be further improved by adopting an interconnection topology that maximizes the data transfer rate among the Processing Elements (PEs).

SEA (Scalable Encryption Algorithm) targeted for small embedded applications. It was initially designed for software implementations in controllers, smart cards, or processors. Here it investigates the performances in recent FPGA devices [9]. Beyond its low cost performances, a significant advantage of the proposed architecture is its full flexibility for any parameter of the scalable encryption algorithm, taking advantage of generic VHDL coding. It also carefully describes the implementation details allowing us to keep small area requirements [10] but it consumes more power.

State of the art FPGA designs methodologies with a focus on industrial control system applications [11]. Speed performance of new components and flexibility inherent of all programmable solutions give many opportunities in the field of digital implementation [12] for industrial control systems. It starts with an overview of FPGA technology [13] development followed by a presentation of design methodologies, development tools and relevant CAD environments. It also includes the usage of portable hardware description languages and system level programming/design tools. Finally, two complete and timely case studies are presented to illustrate the benefits of an FPGA implementation when using the proposed system modeling and design methodology. Thus the result shows minimized the response time, and maximized operational performance in order to achieve low efficiency and low power.

Real-time digital signal processing applications like digital communication systems require high-speed, low-power logarithm operators with low or moderate accuracy [14]. Many methods have been proposed to calculate the logarithm with high accuracy. These methods require complex hardware or have long latencies, so they are not suitable for high-speed, low-power applications. The simplest method to approximate the logarithm was proposed by Mitchell. The drawback of the Mitchell method is its poor maximum approximation error is about 0.08639, which is only 3.53 bits accuracy. A low cost, high-speed architecture for the computation of the binary logarithm was proposed. This architecture was implemented in an FPGA device and the results were compared with other low cost architectures [6]. It requires less area and achieving high-speed but the power required is very high.

Reference [15] shows the traditional data collection terminals mainly utilized by the method of wire, but it is very difficult to wire on the occasion of scattered collection points and also on the scene complex environment. Based on wireless sensor network technology [16], data collection terminal with a core processor was proposed. It replaced the traditional actual wiring with wireless sensor network and sends the collected data to control centre or upper PC in wireless multi-hop way. It makes use of the characteristics of self-organization, self-manag-

ing of wireless sensor network, avoiding the wiring difficulties and make equipment installation, maintenance, replacement more quick and convenient.

Multi-channel data acquisition system is in order to monitor industrial [17] [18] parameters such as the temperature, pressure and humidity more intuitively. In the system, AT89S52 is used to control the LCD that displays different parameters with different colors. The software is designed with digital filter shared by the input channels, so as to reduce the cost and simplify the hardware development. The data acquisition system has some features like small size, low cost and high reliability [19] but the speed of the acquired data is yet to be improved. It is widely used in industrial field.

In response to the complexity of the cable, the occurrence of accidents and completing the task without cables in industrial field, an embedded bluetooth device is used to reduce the cable connection [20]. An embedded Bluetooth data acquisition system [21] is combined with Bluetooth wireless-networking communication which is based on LPC2142 and Bluetooth chip. The rate of data acquisition is up to 150 kHz, as well as 460 kbps for data transmission. The major difference with other data collector is that it has achieved wireless data transmission after the A/D conversion. It's also simpler in circuit design, stronger in integration anti-interference, mobility and practicality; it can be widely used in the complex environment of the industrial field and can substitute traditional wired cable.

The CAN-Ethernet communication module based on ARM processor which is used to convert protocol, however, with less spread and without talking about the technology of self-identification, self-descriptive and interoperability [22]. It focused on the Ethernet interface methods [23], CAN/Ethernet protocol conversion methods and the construction of the network database [24]. Test results showed that the system meets the requirements of automation equipment maintenance, real-time monitoring and reliability. It constituted a network of interconnected system on-site intelligent equipment's, smart on-site equipment and control room devices, which adapts the control system to the intelligent, network-based and decentralized development but the performance and speed of the device is low.

The Run-time assignment of communication tasks onto the communication and computation resources of such a multiprocessor platform is a challenging task [25]. Instead of executing a dedicated hardware task, the fine-grain reconfigurable hardware fabric hosts a programmable soft core block that, in turn, executes the task functionality. It explained a run-time task assignment heuristic that performs fast and efficient task assignment in a multiprocessor system-on-chip but it totally reduces the performance of the processor. In addition, it is capable of managing a configuration hierarchy which improves the task assignment performance (*i.e.*, success rate and assignment quality). In several cases, adding a configuration hierarchy improves the assignment success rate of the assignment heuristic by 20%.

The data acquisition system based on the single-chip is not only limited in

processing capacity, but also the problem of poor real-time and reliability [26]. With the rapid development on the field of industrial process control and the fast popularization of embedded processor, it has been a trend that processor can substitute the single-chip to realize data acquisition and control. The system has the dual redundant network and long-distance communication function, which can ensure the disturbance rejection capability and reliability of the communication network. The reliability of the system is low and it gives poor performance.

Now-a-days the biomedical field needs continuous monitoring for the patients affected by chronic a disease which is very tedious one, so that the recent technology introduces the multichannel signal processing using an On-chip data acquisition process. The advanced technology in DAQ using FPGA allows the multiple components to integrate on a single chip and it has processing, storage and input/output capabilities that are used by the DAQ system. The FPGA [6] for limited purposes for some other DAQs and FPGA works as a coprocessor for fixed-architecture based processor. This has advantages of low-cost, compact-size and the design is integrated in a high-capacity FPGA. Some research teams also utilize the FPGA (fully or partially), but are able to acquire data only a single input channel.

The ASAP system is divided into five steps. First the multichannel analog signal acquisition system is used to acquire multichannel real time analog signals, second the Archiving system stores the acquired data into a Flash memory or SDRAM and third the Digital Signal Processing Unit performs the digital signal processing. The fourth and fifth performs the Frequency Deviation Monitoring (FREDM) system and the Heterogeneous Maximal Service (HMS) Scheduler which is presented to be integrated with FREDM system. The proposed ASAP allows for the sampling of up to 32 heterogeneous signals with a single high speed ADC.

In the proposed design, single high-speed ADC is used along with a multiplexer (MUX) instead of using multiple ADCs to perform quasi-simultaneous DAQ. For fault tolerance and portability, the full system reconfigurability based on FPGA is the best solution and the system can be reused with different configurations. Next, hardware real-time adaptive sampling is only available in the proposed system. It provides the design security in terms of reversing the engineering and secures the design in hardware design.

This system hardware can be realized up to eight data acquisition modules that can be combined and connected to the host PC. The system's software performs the control of data acquisition and the subsequent management of data is coded in LabVIEW. The hardware real-time adaptive sampling is the best way to optimize the ADC sampling rate in case of input signals with different bandwidths and also reduces the overall sampling rate.

2. On-Chip Data Acquisition

The On-Chip data acquisition system brings the large system into a small single chip in order to reduce the cost, size and improving the performance. The mul-

tichannel data processing which when designed by an FPGA network control module, will reduce the hardware size and increase in reconfigurability. It is used to meet the need of many medical and industrial real world applications. This on-Chip Data Acquisition and Processing (DAQP) is capable of simultaneously acquiring multiple heterogeneous signals for networking and processing them in real time. It is a technical challenge to design database classification components that integrates the required functions of the database management layer on the target FPGA chip. The On-Chip DAQP consists of input system such as multi-channel signals, host interface module, and Data processing unit.

In order to make the system reconfigurable and efficient the system should have the following capabilities.

Capability 1: To accept various input signals with different amplitudes and frequencies. It is desired to accept analog input voltage signals of amplitude with a range from mill volts to volts. Furthermore, it is desired to accept input signals in the frequency range from hertz to megahertz. This will allow the system to accommodate a variety of sensors at the same time (e.g., low-frequency electric pulses, acoustic, ultrasounds, etc.).

Capability 2: To perform automatic signal conditioning such as bias addition and removal, adaptive signal scaling, and filtering. Only the information about the signal type will be needed. A library that contains the parameters of filters and amplifiers will be built.

Capability 3: To store the acquired signals without the need for an external computer. A detachable Flash memory write module is needed. A network control module will be needed to securely transmit the acquired signals to authenticated destinations via the Internet.

Capability 4: To have the built-in capability to perform digital signal processing such as FFT and DCT for a 1-D digital signal.

Capability 5: To perform adaptive scheduling for the ADC multiplexed interface for a variable number of channels. If all channels have the same characteristics, then it will be equivalent to a round-robin sampling technique (*i.e.*, uniform sampling, one sample per channel per cycle).

3. Multichannel Data Acquisition and Processing (DAQP) Module

The sensors or transducers are used to measure the non-electrical signals as electrical signals. Generally in industrial applications the sensors are used in various types to measure heterogenic parameters such as velocity, viscosity, pressure, temperature, friction level and vibrations etc,. In medical applications the electrical signals produced by the human body which are measured by ECG, EEG,EMG etc. are analog in nature and should be converted into digital. These signals are typically wave forms of sinewave or sawtooth wave or cosine wave. In existing methodology a signal generator is used to generate the 1-4-8-10 kHz of sine waves for four channel inputs. The n channel inputs can be used and it is multiplexed as n:1 using an multiplexer.

3.1. Host Interface Module

The host interface module consists of different sub modules like analog MUX of n:1, analog to digital converter, and multichannel data buffer as shown in Figure 1.

3.1.1. Multiplexer

A multiplexer (or mix) is a device that selects one of the several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select the input line to send the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. The analog MUX merges the n number of input channel into a single output using a multiplexer. Each and every channel has different sine wave signals with different kHz frequencies. Also here audio signals can also be used for different channels with varying frequency range.

3.1.2. A/D Converter and Multichannel Data Buffer

Using a multiplexer, which force the input to the ADC. The analog to digital converter converts the multiplexed analog input signals into a digital output. The multi channel data buffer is a temporary storage which collects the signal output produced by ADC for continuous time variation. Let n channels be simultaneously acquired by the proposed instrument design. Each channel is assigned a different number of time slots of the MUX time schedule. A flow chart (Figure 2) shows the working of ADC and Data storage.

The acquired samples from the first channel are stored in a buffer. If the buffer is not full the buffer index is incremented, and the channel-assigned time slot

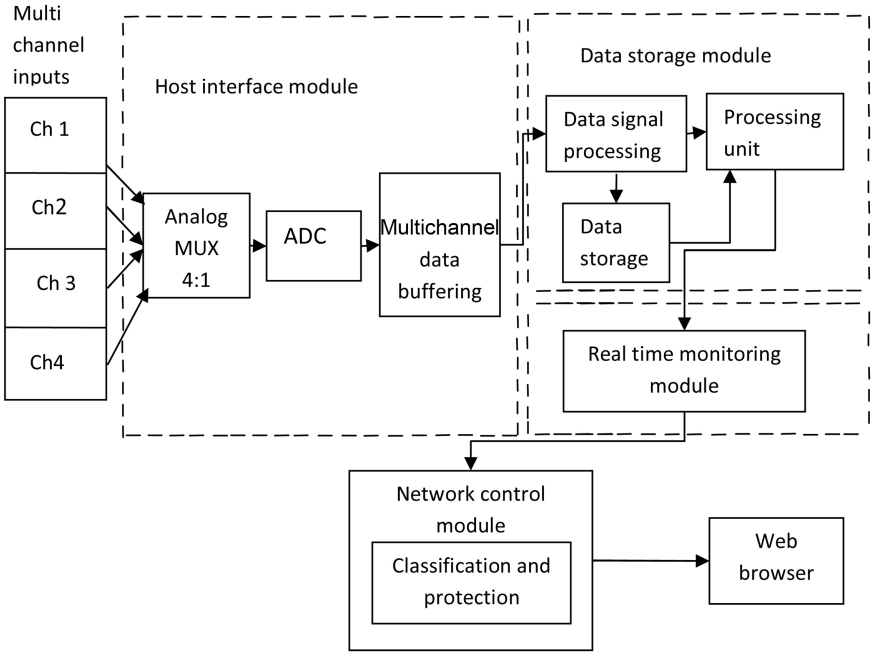

Figure 1. Multichannel DAQP module with network control module.

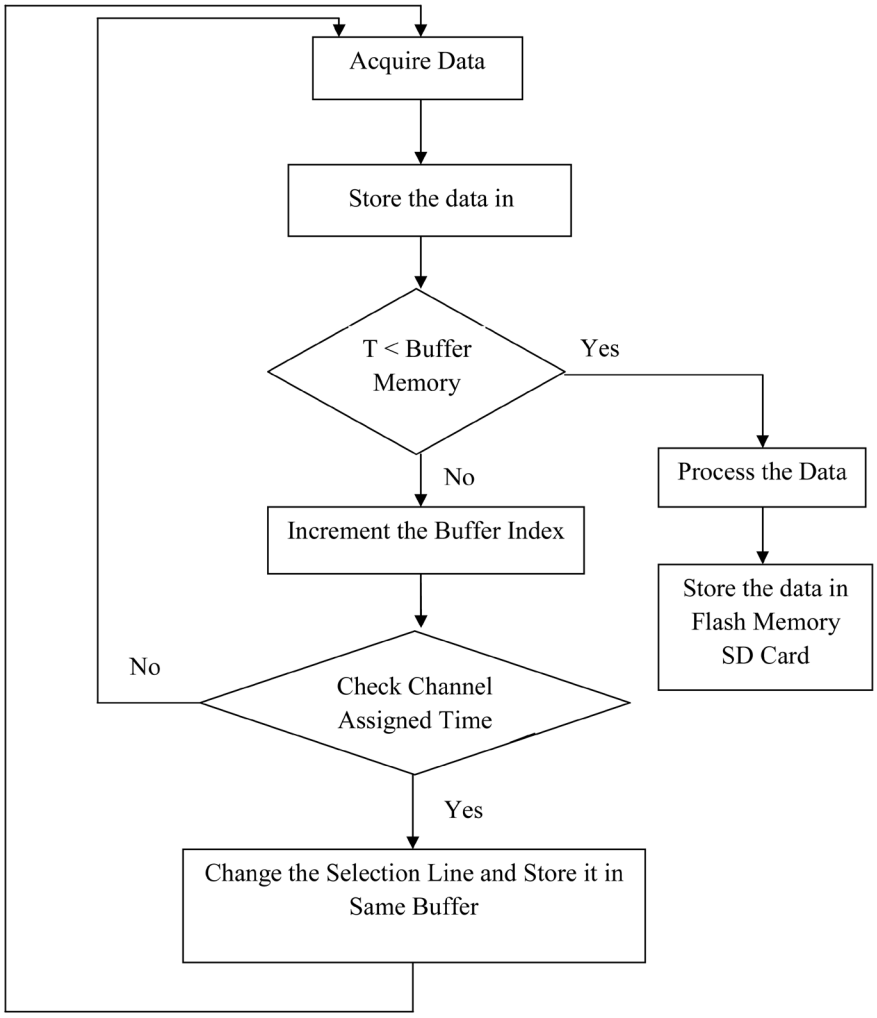

Figure 2. ADC interface design.

is checked. If this channel has more time slots, ADC will acquire more data from this channel. If not, the selection lines (sel) are changed. This change provides collecting data from another channel and storing them into the same buffer to optimize the utilization of the ADC. This utilization is achieved by reducing the time consumed between two consecutive samples.

3.2. Data Storage and Processing Unit

In the data storage and processing unit the digital data which is obtained from ADC through the multichannel input signals are stored in a data storage unit which may be a flash memory. Data storage plays an increasingly essential role in data monitoring, control, and safety protection. Analog data storage is subject to deformation with time and poor privacy protection. On the other hand, digital instrumentation technologies are known for high processing capabilities, which allow them to perform intelligent onboard computing that supports functionality such as universal data storage. In addition, they also provide improved accuracy, flexibility, and easier data protection. This is because the conversion from various analog signal types to a digital format simplifies universal data arc-

hiving and unifies data protection and communication schemes.

3.3. On-Chip RAM

The on-chip real-time archiving is designed to copy the collected data that are temporarily stored in the FPGA internal buffers to nonvolatile memory. This module is designed and embedded in the FPGA to directly write data into the Flash memory card with a minimal interface. In traditional systems, Flash memories are written by the host PC through a permanent interface (*i.e.*, soldered chips on circuit boards). Such use of Flash memory devices is common in embedded systems to store configuration information. Detachable Flash Memory Devices is the only design choice made in the proposed system. Sampled data must be written into the Flash memory device to allow further remote analysis and interpretation and also introduces technical design challenges. In particular, Flash memory must be written by customized hardware and not a PC. Hence, the proposed Flash memory controller addressed the following design requirements.

3.3.1. Synchronization

A detachable Flash memory must have a small and robust physical interface. In interface, it limits the maximum number of data and control pins. It affects the writing speed consequently as a serial data communication that must be employed. Timing and clock signals between the Flash memory controller and the DAQ units must be properly matched. A phase-locked loop and clock dividers are used to achieve this matching.

3.3.2. Integrity

Since a Flash memory is detachable, it needs to be detected before the beginning of writing operations. Hence, the Flash memory must be initialized before the storing process. The storing process cannot be done unless the Flash memory is attached. In order to ensure the data that are passed to the flash memory, Continuous monitoring of the Flash memory during both the reading process and the writing processes are done. A continuous error check code is used to check the valid arrival and storage of the data into the Flash device to avoid error due to disconnection while writing. The writing process is limited by the access time of the Flash memory device. For data integrity, error checking is continuously performed to write properly ordered blocks (*i.e.*, no incomplete or out-of-order blocks). There is no need to store data that are incomplete or out of order. One solution that can be used is an internal buffer. Here it is assumed that there is no data compression and a fixed data arrival rate is available.

3.3.3. Writing Rate

For real-time operation, the processing rate must be faster than the arrival rate. It is advantageous to use the FPGA internal memory cells for buffering because their access time is much smaller than that of external memories. In order to ensure the integrity of the stored data, the Flash memory controller will follow

an error detection algorithm in the data writing process. The FPGA will record acquired data after filling its internal storage buffers. To optimize the acquire-and-write processes, the Flash memory controller can use single- or multiple-block-writing mechanisms. Single block writing can be done to ensure data integrity by using an integrity check value (cyclic redundancy check) at the end of each block. However, if multiple blocks are to be sequentially written into the Flash memory, the total write time can significantly be reduced by the use of a more sophisticated write mechanism. In the multiple-block-writing mechanism, the total write time decreases. This improves the overall performance of the acquire-and-write cycles.

3.4. Real Time Monitoring Module (Display Unit)

The virtual monitoring refers to the monitoring of virtual machines such as virtual desktops and virtual servers. Virtual monitoring recognizes that virtual machines are subject to the same variations in performance as physical machines. An administrator can act to ensure that virtual machines continue to perform optimally with the proper information. A virtual instrumentation user interface module is designed for display of raw data and waveforms. Using LabVIEW platform, it has controls and indicators for controlling and monitoring was developed. For further use, the data log module is designed to record measured data into data files.

3.5. Networking

A computer network connects a collection of computers to allow communication and data exchange between systems, software applications, and users which is also said to be telecommunication network. The computers originate, route and terminate the data that are called nodes which involved in the network. The interconnection of computers is accomplished with a combination of cables or wireless media and networking hardware. When a process in one device is able to exchange information with a process in another device is said to be networking. Networks may be classified by various characteristics, such as the media used to transmit signals and the communication protocols are used to organize network traffic, network scale, network topology and organizational scope.

Internet is the best known computer network. For exchanging information in a computer network, Communication protocols define the rules and data formats. Well-known communication protocols include Ethernet, a hardware and link layer standard that is widely used for local area networks, and the Internet protocol suite (TCP/IP). This defines a set of protocols for communication between multiple networks, for host-to-host data transfer, and for application specific data transmission formats.

A widely-adopted family of communication media is used in Local Area Network (LAN) technology which is collectively known as Ethernet. The media and protocol standards enable the communication between networked devices over Ethernet which is defined by IEEE 802.11. Ethernet embraces both wired and

wireless LAN technologies. Wired LAN devices use cable media as a transmission medium and Wireless LAN devices transmit using radio waves or infrared signals.

3.6. Network Control Module

The need for remote monitoring is vital to measure some acquired signals. Any mobile system should consist of three main modules, these are: non-invasive technique which is used to measure biological signals without doctor interfere, wireless system for transmitting data captured, and a user interface software to enable data acquisition. The multiple components integrate on a single chip and it has processing, storage and input/output capabilities that are used by the DAQ system using FPGA. The data acquisition is implemented with the help of Network Control Module (NCM). It acquires the data with reduced hardware complexity. It further improves the speed and performance of the multichannel data acquisition system.

For runtime monitoring and control, the network control module will securely transmit the acquired runtime signal and store the data into the internet web server. The classification of various signals and protection of data from unauthorized access is carried using NCM as shown in Figure 3.

The proposed DAQ using NCM is designed and implemented using LabVIEW. Data acquisition and processing module which is also called as sensor interface module directly interface with the system for remote monitoring. This base system acquires the signal by the DAQ module and monitors through the real time monitoring module. The monitored information is gathered and analyzed by transmitting it to the remote network management station for online monitoring. The web publishing tools is used to publish on a web page using real time monitoring front panel.

In LabVIEW direct URL locator design, the Ethernet/Wi-Fi modem is used for transmitting the HTML page through internet. Then the client system monitors and controls the DAQP to publish through Ethernet.

4. Hardware Module

The experimental setup of this system was designed under LabVIEW and National

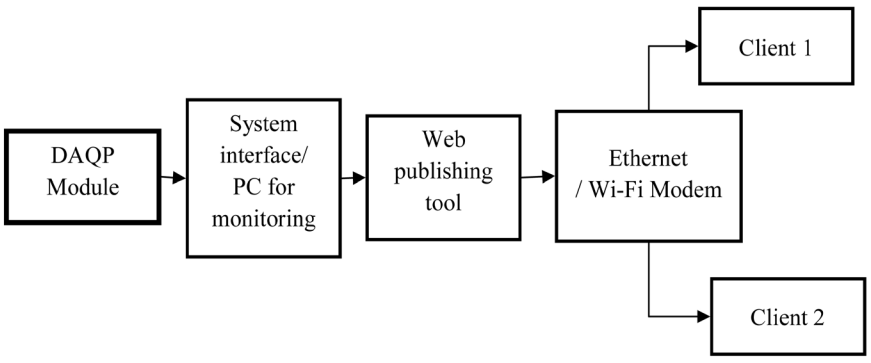

Figure 3. Network control module.

instruments (NI) DAQ board. The design consists of NI ELVIS II board which act as the DAQ card for interfacing the sensors, a NI cRIO (compact reconfigurable input and output) is used for design of the biomedical sensors which is used for acquiring the signals and NI SD memory storage module is used for storing purpose as shown in Figure 4.

4.1. NI ELVIS II

The NI Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) is a hands-on design and prototyping platform that integrates 12 of the most commonly used instruments including the oscilloscope, Function generator, DMM and Bode analyzer into a compact form factor ideal for the hardware lab or classroom. The NI ELVIS II+ is available in the range of 100 MS/s oscilloscope option. This NI ELVIS II has analog input channels of 8 differential or 16 single ended ADC of 16 bit resolution and input frequency up to 50 to 60 Hz.

4.2. Compact RIO (cRIO)

Compact RIO (cRIO) is a reconfigurable embedded control and acquisition system. The Compact RIO system's rugged hardware architecture includes I/O

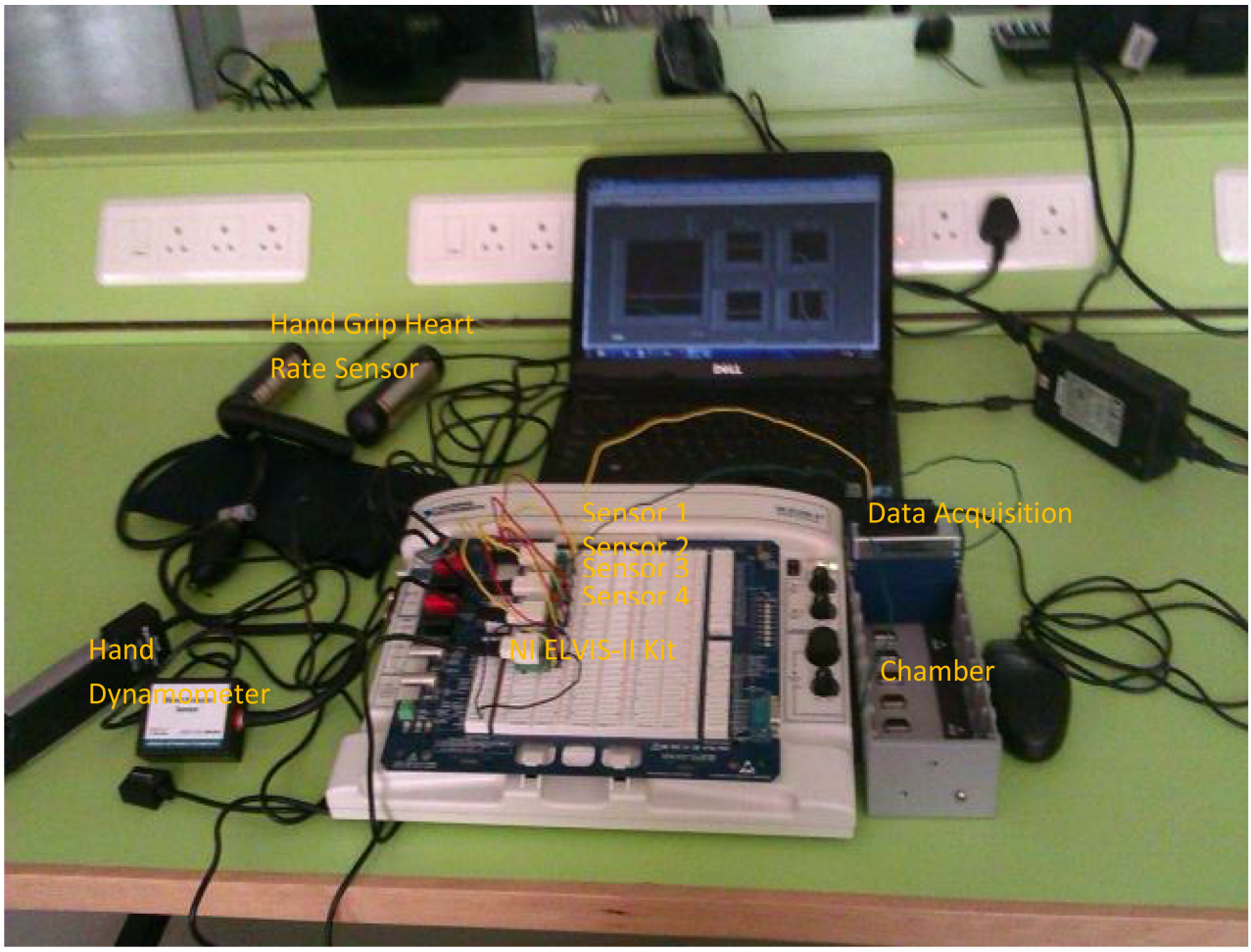

Figure 4. Experimental setup of multichannel DAQP.

modules, a reconfigurable Field Programmable Gate Array (FPGA) chassis and an embedded controller. It is programmed with NI LabVIEW graphical programming tools and can be used in a variety of embedded control and monitoring applications. The cRIO has the processor performance of up to 400 MHz, FPGA performance up to 43,661 logic cells up to 58 multipliers and run under real-time OS. NI 9802 is a secure digital removable storage module which is connected with compact RIO, which it holds the capability of Maximum storage of up to 4 GB per module and sustained data write/read speeds of 2 MB/s.

4.3. NI DAQ

The NI 9225 C Series analog input module has a full measurement range of 300 Vrms for high-voltage measurement applications such as power metering, power quality monitoring, motor test, battery stack testing and fuel cell tests. The NI 9227 C Series current input module is designed to measure 5 A nominal and up to 14 A peaks on each channel with channel-to channel isolation. When the NI 9225 high-voltage module is used, then the NI 9227 current module can measure power and energy consumption for applications such as appliance and electronic device test.

4.4. Surface Temperature Sensor

The Surface Temperature Sensor consists of an exposed thermistor. A thermistor is a special kind of resistor where the resistance value varies significantly with temperature. Thermistors are manufactured from semiconductor material and its resistivity depends exponentially on ambient temperature. Specifically, this sensor uses the 20 kΩ NTC Thermistor whose resistance decreases nonlinearly with increasing temperature. You can rearrange the voltage divider equation to calculate the thermistor resistance from the input voltage measured by the NI ELVIS II Series. The rearranged voltage divider Equation (1.1) is as follows:

$$R = R_1 * V_T / \left(V_s - V_T\right) \tag{1.1}$$

where R = thermistor resistance, R_1 = reference resistance (20 kΩ in this case), V_T = measured voltage, and V_s = supply voltage.

This process uses a LabVIEW program to calculate the thermistor resistance from the above equation and to convert the resistance into temperature Equation (1.2) using the Steinhart-Hart equation for the 20 kΩ NTC Thermistor

$$T = \left[1.02119^{-3} + 2.2246^{-4}\left(\ln R\right) + 1.33342^{-7}\left(\ln R\right)^3\right]^{-1} \tag{1.2}$$

where R = thermistor resistance in ohms.

4.5. NI Modem

IEEE 802.11 wireless or Ethernet communication combines with National Instruments Wi-Fi DAQ devices to produce direct sensor connectivity, and the flexibility of NI LabVIEW software for remote monitoring and control of electrical, physical, mechanical, and acoustical signals. NI Wi-Fi DAQ devices

stream data in real time with the help of built-in signal conditioning and highest commercially available network security for easy-to-use, high-performance remote wireless sensor measurements.

NI Ethernet data acquisition (DAQ) devices outspread the reach of PC-based data acquisition for remote sensor and electrical measurements through the process around the world. NI Ethernet DAQ devices deliver high-speed data and ease of use in a single, small package by combining more than 50 C Series I/O modules with NI Compact DAQ Ethernet chassis and single module Ethernet carriers. In addition, with NI-DAQmx driver software, you can log data for simple experiments or develop a complete test system in NI LabVIEW, ANSI C/C++, Visual Basic.NET, and other programming environments.

5. Frontend Design Module

The entire data acquisition and processing module is designed and simulated using LabVIEW graphical programming language. The block diagram window grasps the graphical source code of LabVIEW. Using this window, the icons and connectors are got from the VI control pallet. The real-time multichannel Data acquisition module block diagram is as shown in Figure 5 using LabVIEW G code. The user interacts with the program using the front panel window. When the VI has to run the front panel of the program it must be opened so that the execution of the program can be monitored.

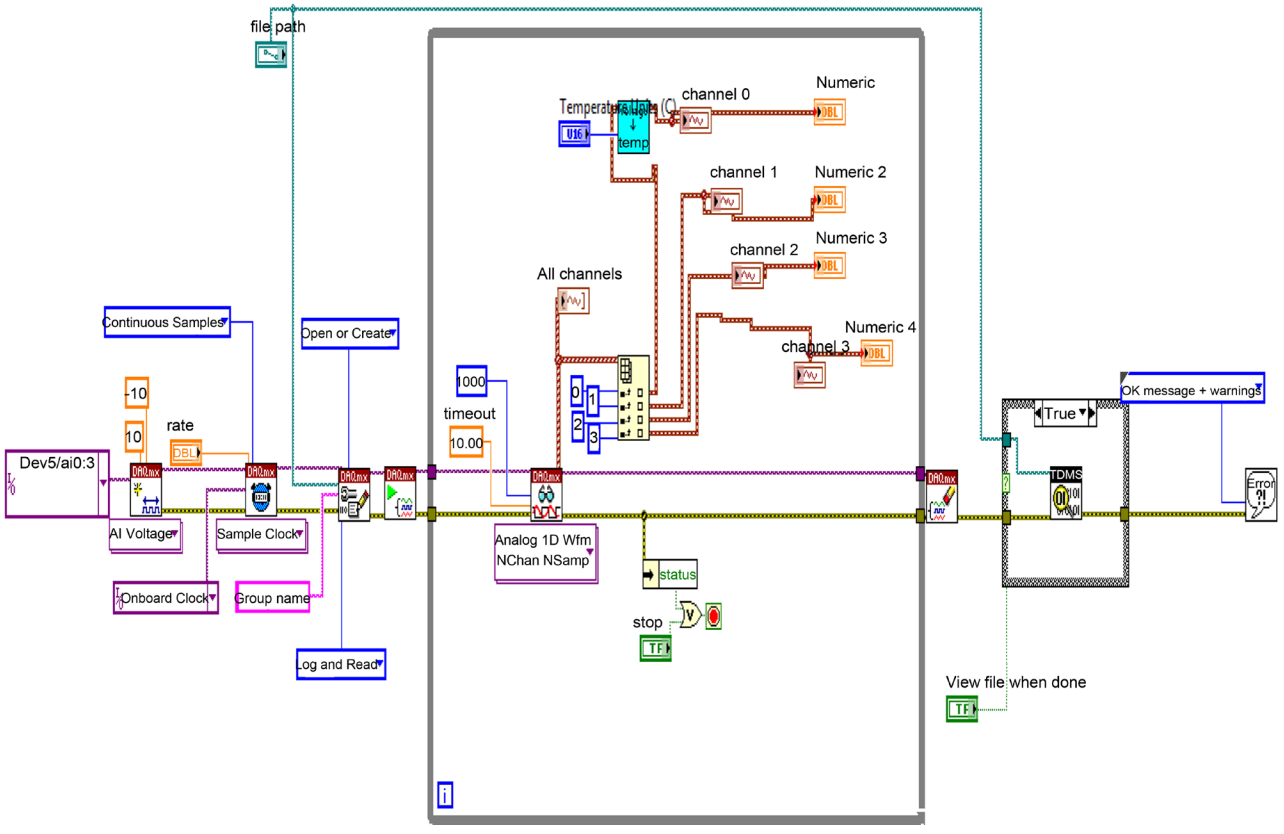

Figure 5. Multichannel DAQP using LabVIEW G code.

5.1. Signal Acquire and Signal Storage Design Using G Code

The front panel is a combination of controls and indicators. Controls simulate typical input objects such as knobs, switches and Indicators shown in **Figure 6**. The virtual window shows the acquired signals from the sensors. The waveform chart shows the combined or mixed signal which are acquired simultaneously at instant of time continuously. The residual waveform charts showing the separated individual sensor signal waveform.

TDMS files establish data in a three-level hierarchy of objects. The top level is encompassed of a single object that holds file-specific information like author or title. Each file can contain an unlimited number of groups and each group can contain an unlimited number of channels.

In general the analog signals from some measuring devices are stored in .wav file format which is machine readable. The TDMS file viewer (**Figure 7**) shows the acquired signals in terms of *.xml* file format which will be both human and machine readable.

5.2. Web Publishing

Web Publishing Tools are the applications that are used to design and build websites for Internet or Intranet. They range from simple text editors that can generate web application code to highly sophisticated and feature-rich web authoring packages. Some of the Web Publishing Tools must be installed on a

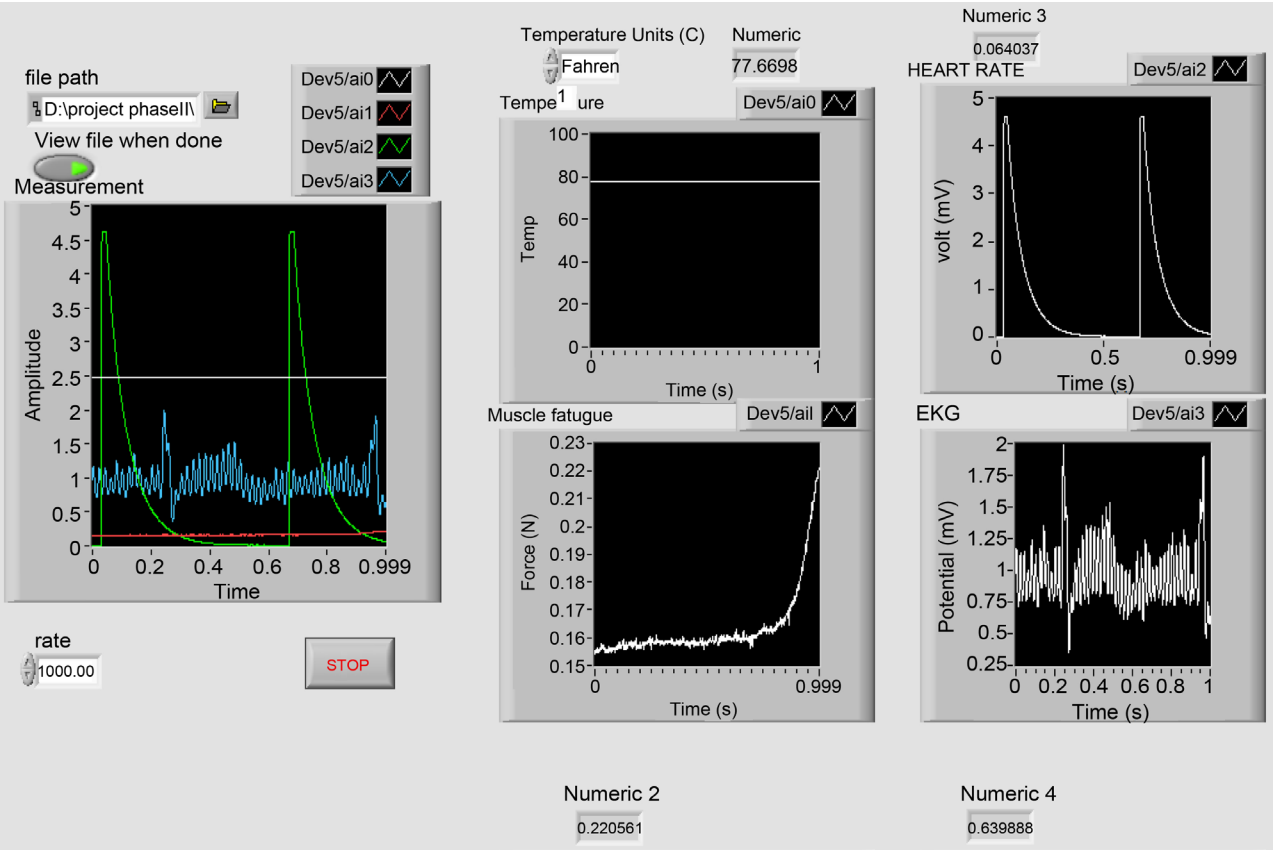

Figure 6. Front panel window of multichannel DAQP module.

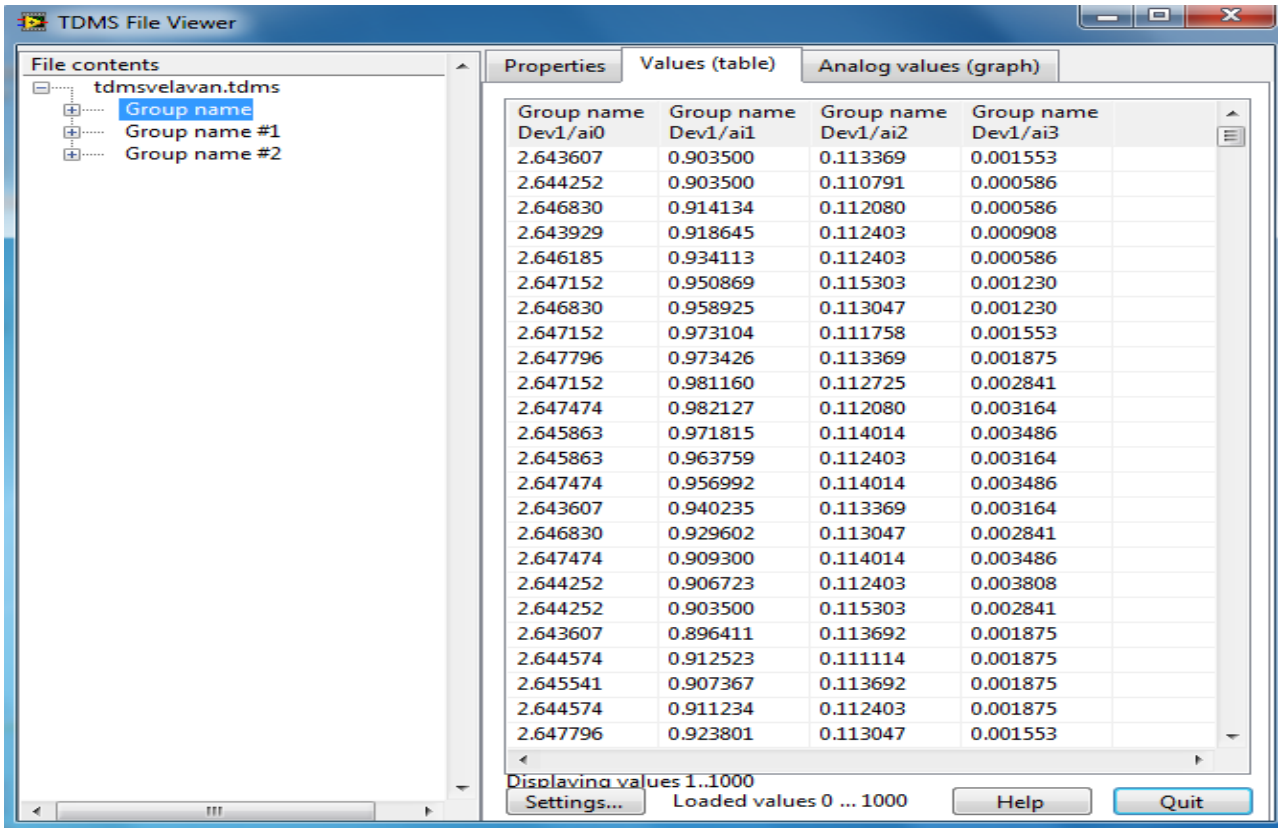

Figure 7. TDMS file viewer for data storage.

workstation and others are server-based and accessed via a web-interface. Web Publishing Tools are also said to be Web Authoring Tools. Figure 8 shows the LabVIEW G code design for immediate URL locator for publishing the designed and stored web page in the server system. The Lab VIEW provides a supportive method for web publishing application.

The front panel window published in webpage of Multichannel DAQP module. The real time monitoring and online control of Multichannel DAQP system is done through internet for continuous monitoring. The use of TCP/IP or UDP mode of web publishing can be applicable for this real time monitoring. The Ethernet data transmission and receiving can be accessed in high speed and accuracy.

5.3. FPGA Implementation

The FPGA is Field Programmable Gate Array, The NI LabVIEW FPGA Module extends the LabVIEW graphical development platform to target FPGAs on NI reconfigurable I/O (RIO) hardware. LabVIEW is well-matched for FPGA programming because it clearly represents parallelism and data flow.

The multichannel data acquisition and processing module is implemented in NI cRIO standalone device which is designed with inbuilt FPGA. The FPGA implementation design must be done using project explorer window. The FPGA target.vi and Host.vi is created and the hardware used for the project implementation is configured before implementation.

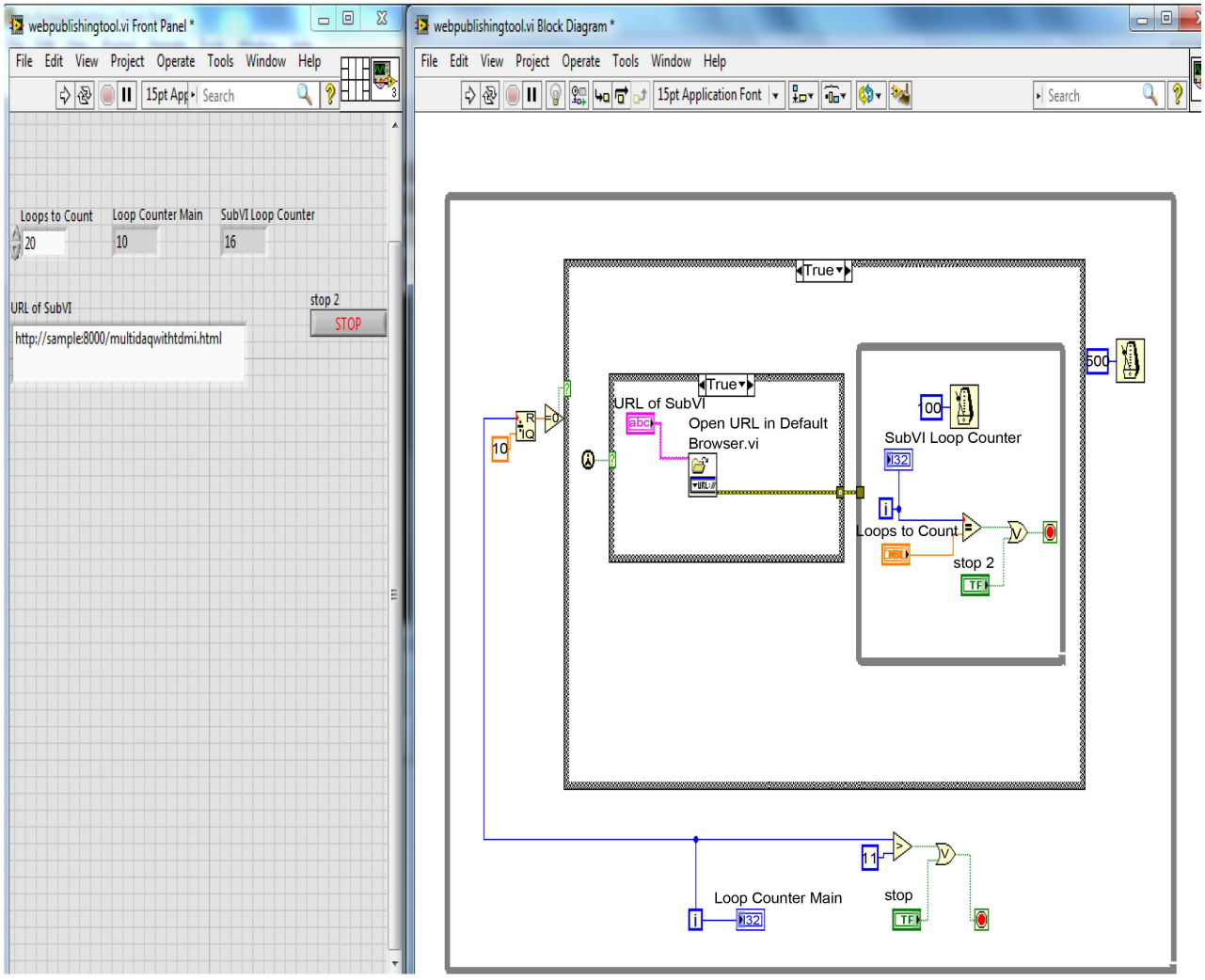

Figure 8. LabVIEW G-code designs for Web publishing URL locator.

5.3.1. Target VI

LabVIEW Real-Time Module users run programs with a RT target.vi that runs in the Real-Time operating system and a host computer VI that runs in Windows as shown in **Figure 9**.

The VIs does not consume space in the memory of the RT target while they are not running. Also, there is no need for a startup executable when using this technique. In some cases, this may be more flexible than using a more static startup executable.

The target.vi is a FPGA target for accessing the number of inputs needed and selecting the input port of the module. It selects the data types, memory size and data read write operations. It is compiled for generating the bitfiles in order to load it into the Host.vi.

5.3.2. Host VI

To transfer data between an FPGA VI and a Windows-based host.vi programmatically, either programmatic front panel communication or Direct Memory Access (DMA) is used. These methods have a user-defined timing model, to

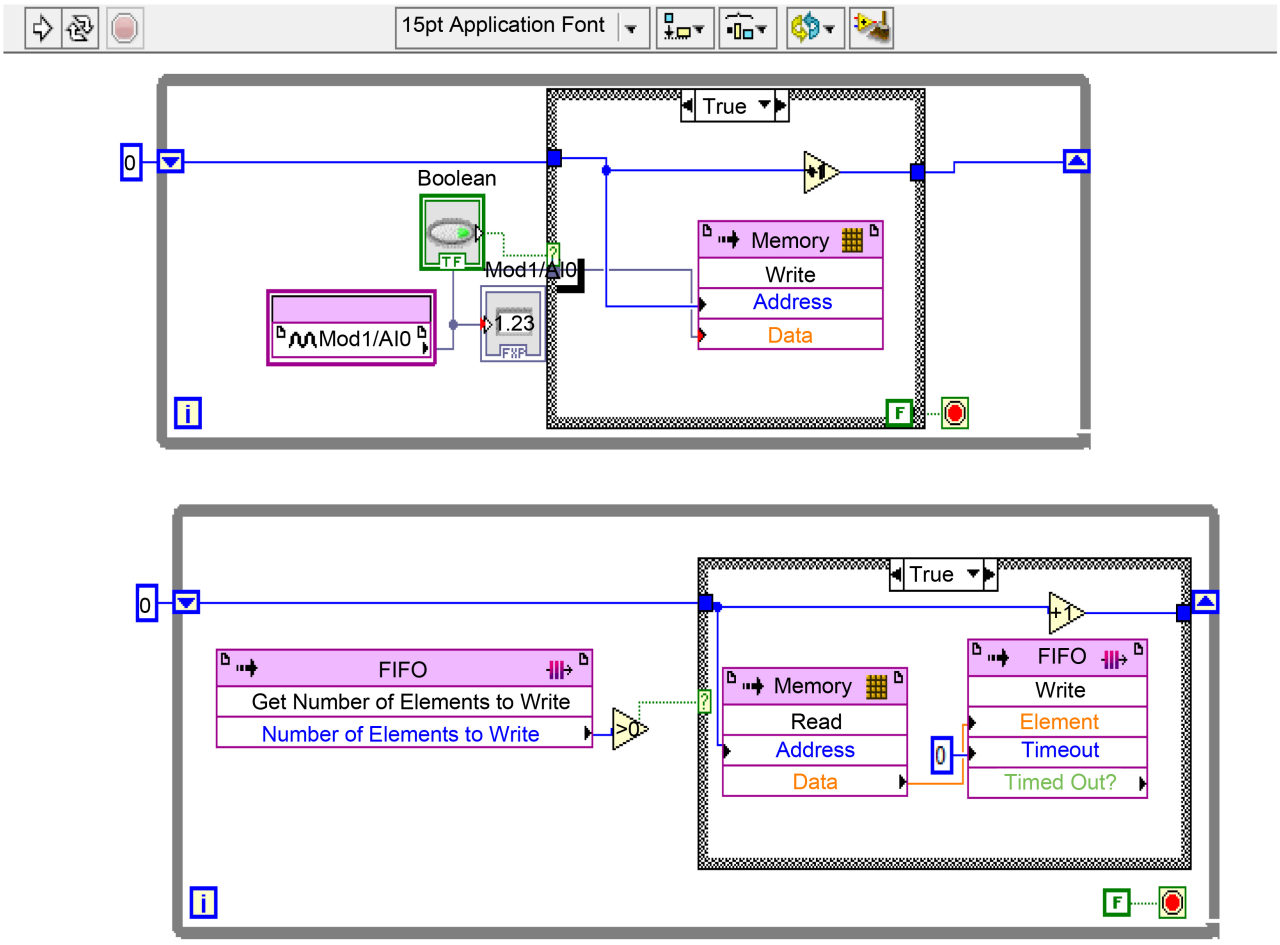

Figure 9. Design of FPGA target.vi for multichannel DAQP using LabVIEW G-code.

create block diagram code that synchronizes the FPGA.vi along with host.vi.

The host vi is a FPGA vi where the signals or the data is to be deployed into the FPGA device. By using the reference VI function the bitfiles of the target.vi is configured for the deployment. It is designed for virtual monitoring of the acquired signal data from the sensor module, only after the successful deployment of the host.vi. The FPGA will process the application. The host.vi is as shown in Figure 10.

The window is the deployment status of the FPGA implementation of Multichannel DAQP module. The module is successfully implemented in FPGA with zero errors.

The deployment of FPGA host.vi for Data acquisition of temperature sensor is successfully done using the stand alone device NI cRIO 9073. The waveform chart showing the result of the FPGA implemented application of temperature sensor is shown in Figure 11. It clearly depicts the accuracy of the measurement result and the speed of acquisition response in minimum time.

6. Result Analysis

The proposed Multichannel DAQP system can be used to acquire human body

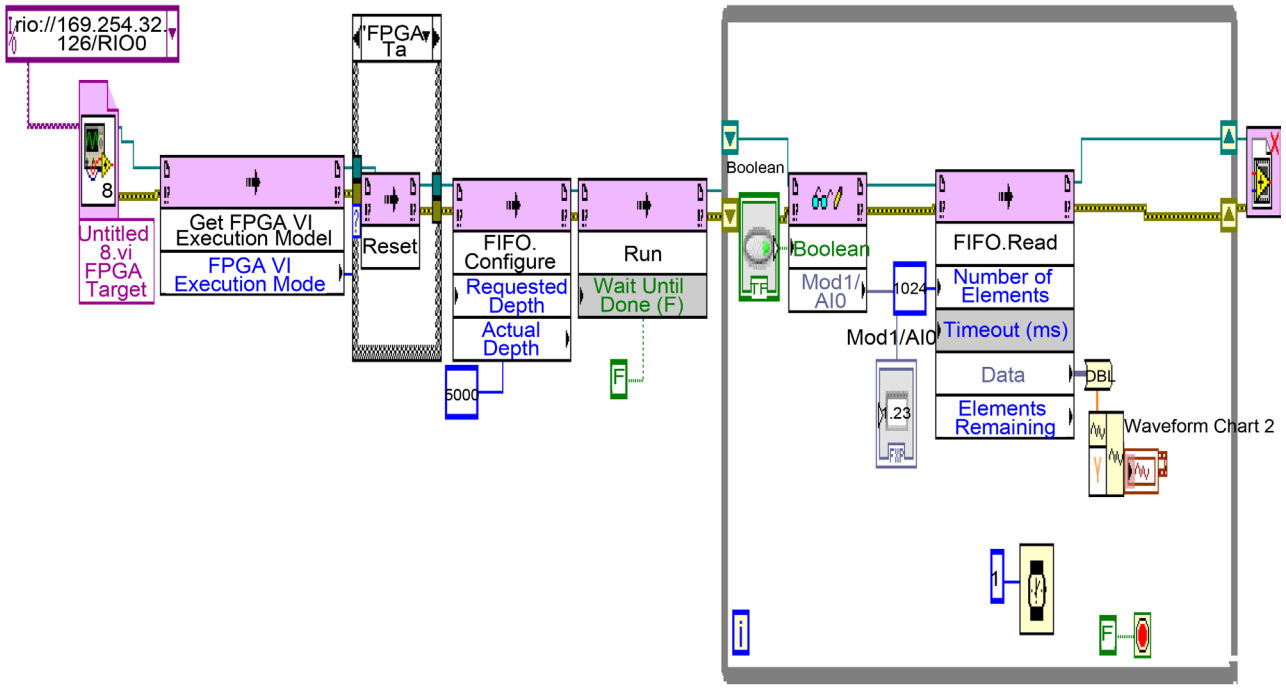

Figure 10. LabVIEW G-code for FPGA host.vi.

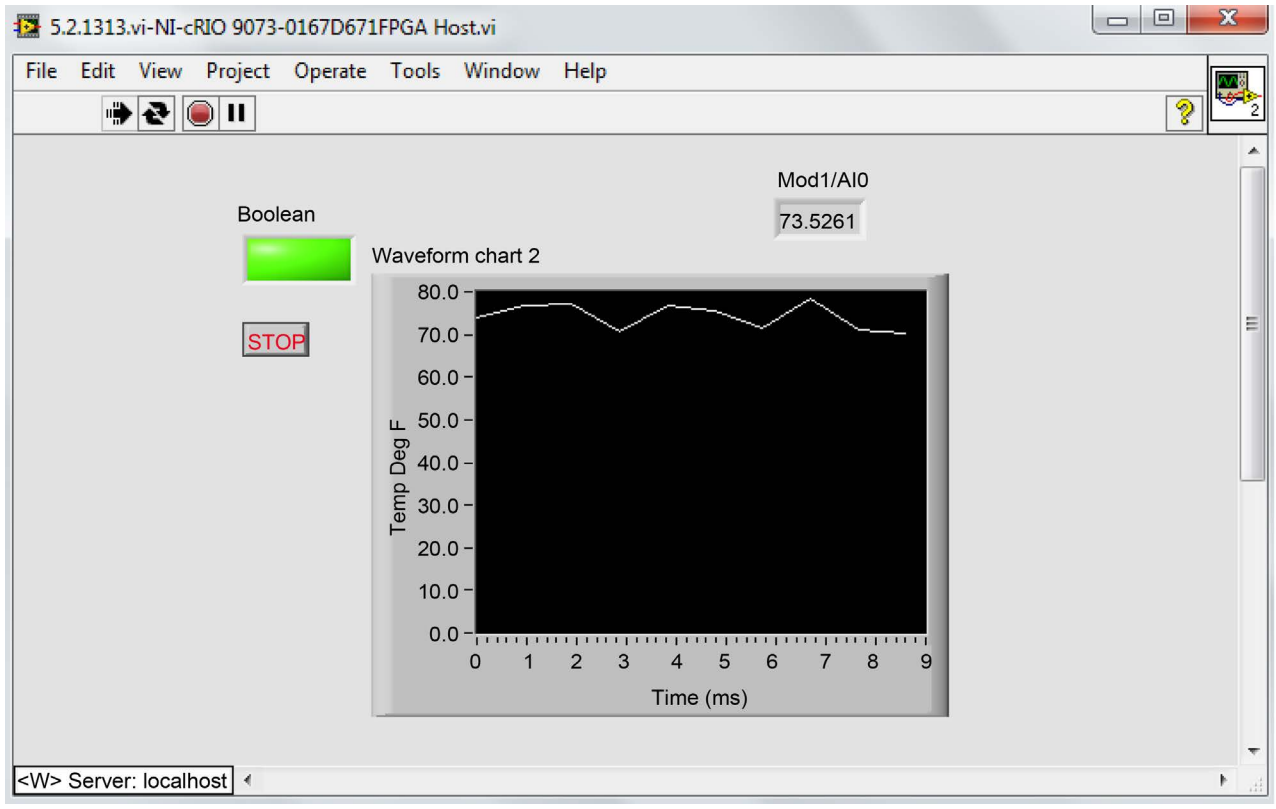

Figure 11. FPGA output result for temperature measurement.

signals such as the heartbeat, pressure and the lung sound. The varying sampling rate per channel is the optimal solution in terms of scalability, power consumption and memory requirements. This leads to reduction in the circuit size, low

power consumption, and low storage requirements as shown in Figure 12.

In addition, the proposed DAQ is used without the need to computing systems such as a PC. The reconfigurability brings the system to work with advanced and recent updating software or hardware. The remote monitoring technique brings the need of online monitoring and control or diagnosis application and the technology makes secure and easiest way of data transmission and receiving. The entire system was tested using the LabVIEW tool with National Instruments hardware tool kits for the real time testing and FPGA implementation. Table 1 shows the comparison in the performance of the proposed methods.

7. Conclusion

Field Programmable Gate Array (FPGA) is one of the ultimate operative reconfigurable devices. The System-on-Chip Field Programmable Gate Array (SoC-FPGA) is used in the proposed system to reduce the hardware and memory size. The results prove reduction in the circuit size, cost and power consumption by the proposed DAQ. This developed system achieves high resolution with memory reduction, reduced hardware size, fast remote monitoring and control. Later, it can be improved using web camera servers at the device or process to provide the visual image of the device reaction for better systems performance

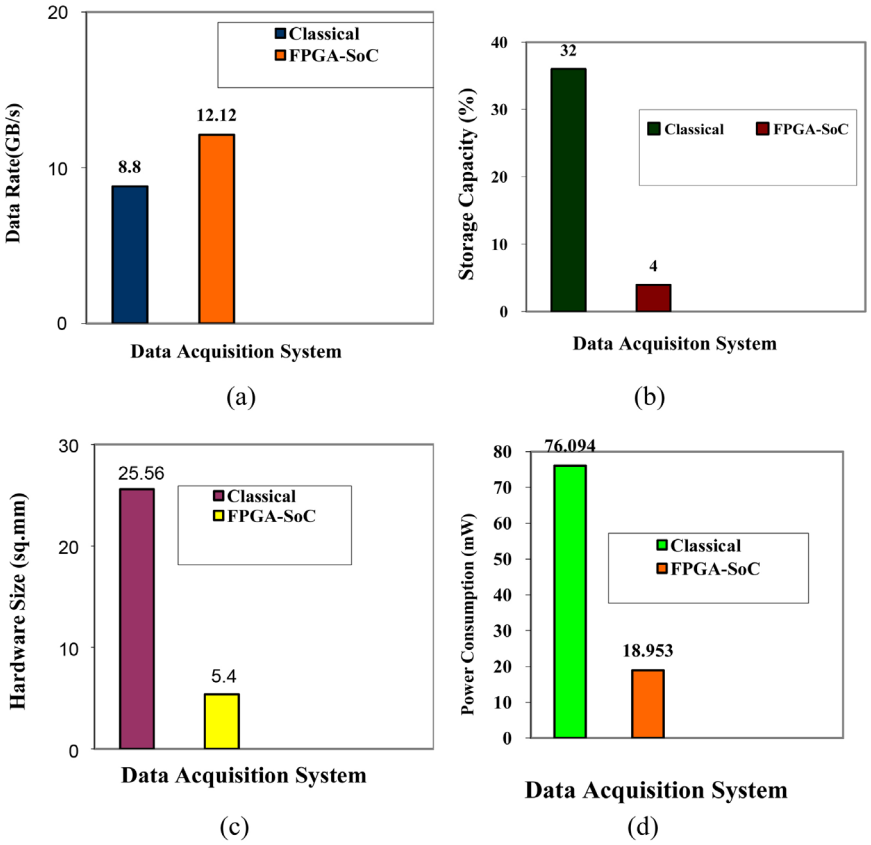

Figure 12. Performance analysis of proposed FPGA-SoC based DAQ system (a) Data rate speed (b) Storage capacity (c) Hardware size (d) Power consumption.

Table 1. Comparison in the performance of the proposed methods.

Data Acquisition system	Data rate speed (GB/s)	Storage Capacity	Hardware Size (mm^2)	Power Consumption (mW)
Classical	8.80	32% (32 × 16384)	25.56	76.094
FPGA SoC	12.12	4% (8 × 16384)	5.40	18.953

evaluation. In future data acquisition can be applied for agriculture to acquire the data with more security even in remote areas.

References

[1] Zhu, Q., Zhu, D. and Su, X. (2010) Distributed Remote Temperature Monitoring and Acquisition System Based on CAN Bus. *Proceedings of IEEE International Conference on Prognostics and System Health Management*, Macao, 12-14 January 2010, 1-4. https://doi.org/10.1109/phm.2010.5413439

[2] Gori, L., Tommasini, R., Cautero, G., Giuressi, D., Barnaba, M., Accardo, A., Carrato, S. and Pauolucci, G. (1999) An Embedded Control and Acquisition System for Multichannel Detectors. *Nuclear Instruments and Methods in Physics Research*, **431**, 338-346. https://doi.org/10.1016/S0168-9002(99)00286-7

[3] Cabal-Yepez, E., Garcia-Ramirez, A.G., Romero-Troncoso, R.J., Garcia-Perez, A. and Osornio-Rios, R.A. (2013) Reconfigurable Monitoring System for Time-Frequency Analysis on Industrial Equipment through STFT and DWT. *IEEE Transactions on Industrial Informatics*, **9**, 760-771. https://doi.org/10.1109/TII.2012.2221131

[4] Malinowski, A. and Hao, Y. (2011) Comparison of Embedded System Design for Industrial Applications. *IEEE Transactions on Industrial Informatics*, **7**, 244-254. https://doi.org/10.1109/TII.2011.2124466

[5] Garrity, D., LoCascio, D., Cavanagh, C., Kabir, N.M. and Guenther, C. (2008) A Single Analog-to-Digital Converter That Converts Two Separate Channels (I and Q) in a Broadband Radio Receiver. *IEEE Journals of Solid State Circuits*, **43**, 1458-1469. https://doi.org/10.1109/JSSC.2008.922718

[6] Abdallah, M. and Elkeelany, O. (2011) InTech. http://www.intechopen.com/books/applied-biomedicalengineering/towards-affordable-home-health-care-devices-using-reconfigurable-system-on-chip-technology

[7] Hur, H.Y., Stefanov, T., Wong, S. and Goossens, K. (2011) Customisation of On-Chip Network Interconnects and Experiments in Field Programmable Gate Arrays. *IET Computer Digital Techniques*, **6**, 59-68. https://doi.org/10.1049/iet-cdt.2010.0105

[8] Jagadeesh, G.R., Srikanthan, T. and Lim, C.M. (2010) Field Programmable Gate Array-Based Acceleration of Shortest Path Computation. *IET Computers and Digital Techniques*, **4**, 231-237.

[9] Mace, F., Standaert, F.X. and Quisquater, J.J. (2008) FPGA Implementation of a Scalable Encryption Algorithm. *IEEE Transactions on VLSI*, **16**, 212-216. https://doi.org/10.1109/TVLSI.2007.904139

[10] Angarita, F., Marin-Roig, J., Almenar, V. and Vallas, A. (2012) Low Complexity Low Density Parity Check Decoding Algorithm for High Speed Very Large Scale Integration Implementation. *IET Computers and Digital Techniques*, **6**, 2575-2581.

[11] Scrofano, R., Gokhale, M.B., Trouw, F., Monmasson, V.K.E. and Cirstea, M.N.

(2007) FPGA Design Methodology for Industrial Control Systems—A Review. *IEEE Transactions on Industrial Electronics*, **54**, 1824-1842. https://doi.org/10.1109/TIE.2007.898281

[12] Pimentel, B.S., de Avila Valgas Filho, J.H. and Campos, R.L. (2001) A FPGA Implementation of a DCT-Based Digital Electrocardiographic Signal Compression Device. *Proceedings of* 14*th Symposium on Integrated Circuits and System Design*, Pirenopolis, 15 September 2001, 44-49. https://doi.org/10.1109/SBCCI.2001.953002

[13] Yanez, J., Quintana, D., Quintáns, C., Fariña, J. and Rodríguez-Andina, J. (2005) FPGA-Based System for the Education in Data Acquisition and Signal Generation. *Proceedings of Annual IEEE Conference on Industrial Electronics Society*, Raleigh, 6-10 November 2005, 2168-2173. https://doi.org/10.1109/iecon.2005.1569240

[14] Gutierrez, R. and Vallas, J. (2011) Low Cost Hardware Implementation of Logarithm Approximation. *IEEE Transactions on VLSI*, **19**, 2326-2330. https://doi.org/10.1109/TVLSI.2010.2081387

[15] Gao, M., Zhang, F. and Tian, J. (2008) Design and Implementation of Wireless Sensor Network Data Collection Terminal Based on ARM9. *International Colloquium on Computing, Communication, Control and Management*, Guangzhou, 3-4 August 2008, 587-590. https://doi.org/10.1109/cccm.2008.335

[16] Guo, H., Low, K.S. and Nguyen, H.A. (2011) Optimizing the Localization of a Wireless Sensor Network in Real Time Based on a Low-Cost Microcontroller. *IEEE Transactions on Industrial Electronics*, **58**, 741-749. https://doi.org/10.1109/TIE.2009.2022073

[17] Sun, R., Tian, Y. and Dong, Y. (2009) Design and Implementation of Industrial Multi-Parameter Data Acquisition System Based on AT89S52. *International Symposium on Intelligent Information Technology Application Workshops*, Nanchang, 21-22 November 2009, 169-172.

[18] Salvadori, F., Campos, M., de Camargo, R.F., Gehrke, C., Rech, C., Sausen, P.S., Spohn, M.A. and Oliveira, A. (2007) Monitoring and Diagnosis in Industrial Systems Using Wireless Sensor Networks. *Proceedings of IEEE Conference on Wireless Internet Service Provider*, Alcala de Henares, 3-5 October 2007, 1-6. https://doi.org/10.1109/wisp.2007.4447498

[19] Barone, U. (2013) Design of a Portable, Intrinsically Safe Multichannel Acquisition System for High-Resolution, Real-Time Processing HD-sEMG. *IEEE Transactions on Biomedical Engineering*, **60**, 2242-2252. https://doi.org/10.1109/TBME.2013.2252346

[20] Sun, H. and Jiang, M. (2009) Bluetooth Data Acquisition System Based on ARM. *International Workshop on Education Technology and Computer Science*, Wuhan, 7-8 March 2009, 872-875. https://doi.org/10.1109/etcs.2009.197

[21] Anitha, K., Srinivasa, R.M. and Murthy, C.R.S. (2011) Embedded Bluetooth Data Acquisition System based on ARM for Unmanned Underwater Vehicle (UUV). *International Journal of Computer Science and Network Security*, **11**, 136-140.

[22] Zhao, X., Su, H., Ren, M., Cao, Y., Chen, L. and Wang, F. (2009) Remote Equipment Monitoring System Based on ARM9 and CAN Bus. *Proceedings of the IEEE Global Congress on Intelligent Systems*, Xiamen, 19-21 May 2009, 298-302.

[23] Li, D., Zhong, C., Yuan, X. and Zhang, L. (2006) Study on Embedded Equipment Web Monitoring and Control Based on Industrial Ethernet. *Proceedings of* 6*th World Congress on Intelligent Control and Automation*, Dalian, 21-23 June 2006, 4600-4603. https://doi.org/10.1109/WCICA.2006.1713252

[24] Orekhov, D.I., Chepurnov, A.S., Sabel'nikov, A.A. and Maimistov, D.I. (2007) A Distributed Data Acquisition and Analysis System Based on a CAN Bus. *Interna-*

tional Journal on Instruments and Experimental Techniques, **50**, 65-72.

[25] Nolet, V., Avasare, P., Eeckhaut, H., Verkest, D. and Corporaal, H. (2008) Run-Time Management of a MPSoC Containing FPGA Fabric Tiles. *IEEE Transactions on VLSI Systems*, **16**, 24-33. https://doi.org/10.1109/TVLSI.2007.912097

[26] Peng, D., Zhang, H., Zhang, K., Li, H. and Xia, F. (2009) Research and Development of the Remote I/O Data Acquisition System Based on Embedded ARM Platform. *Proceedings of IEEE International Conference on Electronic Computer Technology*, Macau, 20-22 February 2009, 341-344.