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Minimization of Switching Devices and Driver Circuits in Multilevel Inverter

S. Jawahar[1], P. Ramamoorthy[2]

[1]HOD/Electrical, VSVN Polytechnic College, Virudhunagar, India
[2]ECE, Adhitya Institute of Technology, Coimbatore, India
Email: sjeeevsvn@gmail.com

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Abstract

The various configurations of multilevel inverter involve the use of more numbers of switching devices, energy storage devices and/or unidirectional devices. Each switching unit necessitates the add-on driver circuit for proper functionality. Cascaded H-Bridge Multilevel Inverter requires overlapped switching pulses for the switching devices in positive and negative arms of the bridge which may lead to short circuit during the device failure. This work addresses the problems in different configurations of multilevel inverter by using reduced number of switching and energy storage devices and driver circuits. In the present approach Single Switch is used for each stair case positive output and single H-Bridge for phase reversal. Driver circuits are reduced by using the property of body diode of the MOSFET. Switching pulses are generated by Arduino Development Board. The circuit is simulated using Matlab. More so, through experimental means, it is physically tested and results are analyzed for the 5-step inverter and thereby simulation is fully validated. Consequently, cycloconverter operation of the circuit is simulated using Matlab. Moreover, half bridge configuration of the multilevel inverter is also analyzed for high frequency induction heating applications.

Keywords

H-Bridge Multilevel Inverter, Single Switch Multilevel Inverter, Body Diode, Switching Angle, THD, Cycloconverter, Half Bridge Multilevel Inverter

1. Introduction

Multilevel inverters find applications in domestic and industrial power system. These inverters basically convert DC power from stand alone units like solar cell, fuel cell and battery into AC power. For this power conversion,

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multilevel inverter uses an array of power switches, DC sources and in some cases diodes/capacitors. The concept of multilevel inverter is first introduced by Baker Richard H and Bannister Lawrence H, in their work titled **Electric Power Converter**. They designed a system that employed a number of stages connected in cascade. Each stage includes an electrical energy source or an electrical energy storage unit and switch means adapted to bypass the energy source or storage unit, to interconnect the source or storage unit with other electrical energy sources or storage units across a load in a programmed fashion, and to reverse the direction of current flow in the load to apply, for example, a quasi-sinusoidal voltage across the load [1].

Figure 1 shows the basic arrangement of multilevel inverter. It includes an array of switches and voltage sources, the output of which generates voltages with stepped waveforms. The commutation of the switches permits the addition of the voltages sources, which reaches high voltage at the output.

It allows low staircase switching frequency and also high PWM frequency [2]. The cascaded multilevel inverters are formed by connecting H-Bridge Modules in series. Each module is connected with its own DC source and by proper switching sequence of series connected H-Bridge module; stepped sine waveform is produced. This inverter is applicable to high voltage, high power applications such as flexible AC transmission systems (FACTS) including static VAR generation (SVG), power line conditioning, series compensation, phase shifting and voltage balancing and fuel cell and photovoltaic utility interface systems [3]. Single phase full bridge inverter with a DC source can produce 3-level waveform. A cascaded H-bridge multilevel inverter can produce a maximum of (2S + 1) distinct level of voltage, where S is the number of DC sources. Each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

Figure 2 represents five-step cascaded H-bridge inverter circuit. Five-step cascaded H-Bridge inverter circuit requires 20 switching devices. Moreover, the bottom switches in each arm are of high side switching type. It requires 10 driver circuits.

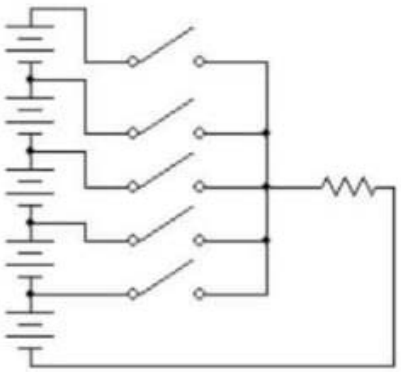

Figure 1. Basic arrangement of cascaded multilevel inverter.

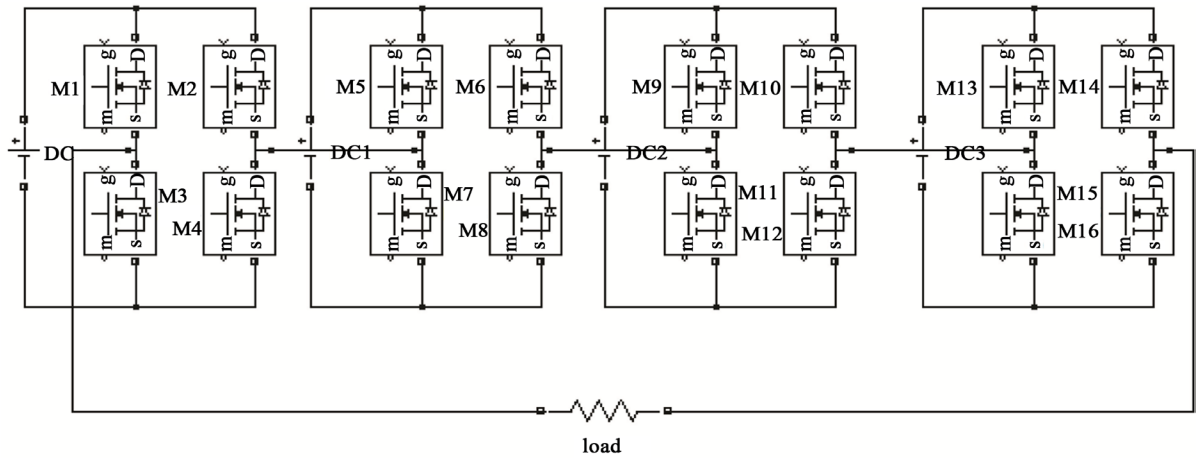

Figure 2. Five step cascaded H-bridge inverter.

In this paper, single switch for each step of staircase waveform generation is presented. With this arrangement S + 4 switches can produce S + 1 steps of voltages. For five steps, the proposed circuit needs only 9 switches. Driver circuits' need for this arrangement is two. To reduce the number of driver circuits, stepped voltage is shifted to drain of the switching MOSFET. By changing the switching angle of the load bridge, cycloconvertor operation is obtained. Half-bridge single-phase inverter is analyzed for three levels in [4]. Cascaded multilevel inverter (MLI) based on Secondary Multilevel Constituent (SMC) consisting of a series of stacked half bridge cells and an H-bridge inverter is proposed in [5]. This MLI outputs higher voltage levels with the same number of switching devices. Problem arises when using half-bridge for multilevel. This work addresses the problem in implementing half-bridge multilevel inverter.

2. Single Switch Multilevel Inverters

2.1. Single Switch Multilevel Inverter Operation

Figure 3 represents single switch multilevel inverter circuit. In this circuit only one switch is provided for each level and an H bridge is used only in the output stage. The individual dc sources are connected to load through the switches at timed intervals of sinusoidal steps. At the source terminal of the first MOSFET switch dc sources are accumulated by the holding capacitor and directed to its source terminal. Diode in series with the switching device prevents the accumulated voltage from returning to the dc source.

One of the main advantages of the multilevel inverter (MLI) is that it is able to produce low total harmonic distortion (THD) voltage waveforms. This is because the MLI is characterized by a large number of voltage vectors [6]. Total Harmonic Distortion is reduced in multilevel inverter by increasing the number of levels. A lot of algorithms are tried by various researchers to reduce the THD of the multilevel inverter. In this work, a simple approach is proposed. Each stage of inverter is switched at an angle, by taking into account the % of voltage of the current stage to the peak voltage *i.e.* % of number of steps. **Table 1** shows the switching angle for each level of 11 step multilevel inverter.

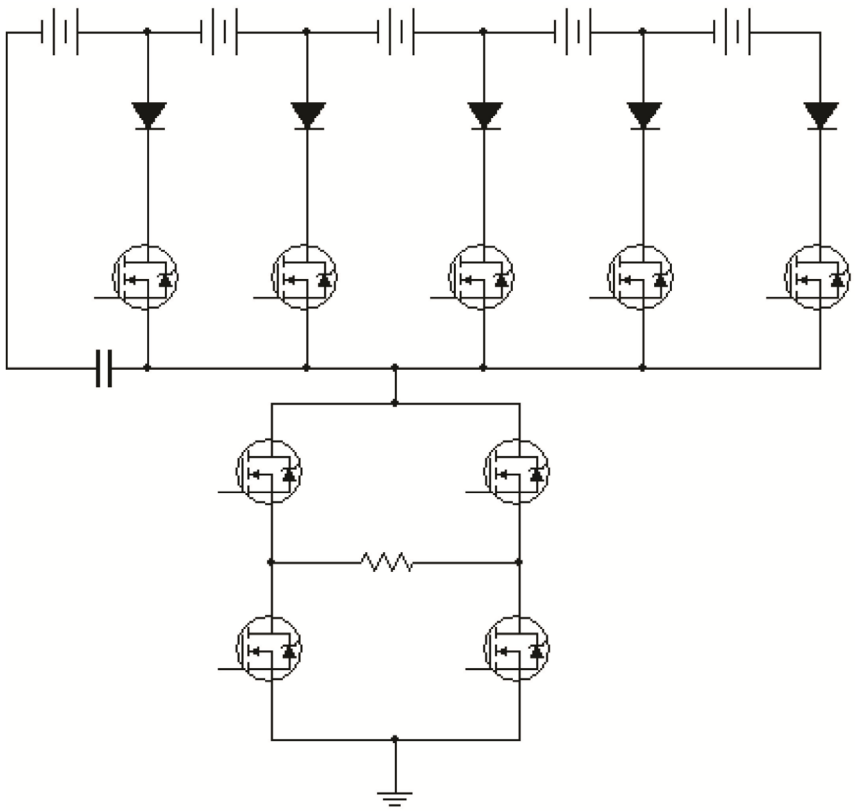

Figure 3. Five steps multilevel inverter.

Table 1. Switching angle for 11-step inverter circuit.

Level	Normalized Value of Voltage referring to peak	Switching angle
0	0	0
1	0.1	5.739
2	0.2	11.54
3	0.3	17.457
4	0.4	23.57
5	0.5	30
6	0.6	36.87
7	0.7	44.43
8	0.8	53.13
9	0.9	64.158
10	0.999	87.44

Figure 4 shows the Matlab simulation result for the 11-step inverter circuit. Voltage at the drain of the first MOSFET is in the upper side and voltage at the load point is in the lower side of the figure.

The rms value of the output voltage is given by

$$V_{rms} = \sqrt{\frac{1}{T}\int_{t_1}^{t_2} v^2 \mathrm{d}t + \int_{t_2}^{t_3} 2v^2 \mathrm{d}t + \cdots + \int_{t_{m-2}}^{t_{m-1}} mv^2 \mathrm{d}t} \quad (1)$$

where m = number of levels; v = voltage of the individual cell; T = time taken to reach peak value.

For the frequency of 50 Hz and switching angle given in **Table 1** the rms voltage value of output waveform is

$$V_{rms} = 180.7 \text{ Volts} \quad \text{for } V_{dc} = 264 \text{ Volts}$$

Figure 5 and **Figure 6** represent the voltage and current total harmonic distortion curve for the 11-step multi level inverter with resistive inductive load. Fifth harmonics is predominant for the selected switching angle and third harmonics predominate when the load is resistive in the current THD.

Fundamental frequency = 50 Hz; Fundamental voltage = 255.3 Volts; Total Harmonic Distortion = 4.96.

When the load is inductive, total harmonic distortion slightly increases (5.68) due to the fact that the induced voltage in the inductor with time varying stepped input varies.

Fundamental frequency = 50 Hz; Fundamental current = 2.241 Amps; THD = 5.68.

The main disadvantage of cascaded H-Bridge topology is that large number of driver circuits require for gating the switches. High side switching (load connected to the source side) requires gate to source voltage greater than threshold voltage. In order to turn on the N channel MOSFET in high side switching, the gate voltage, V_g, should be greater than threshold and output.

$$V_g > V_{out} + V_{th}$$

For this purpose, high side switching requires driver circuit for each switching device. To solve this issue, voltage shifting from source to load through body diode is proposed in this paper. In n channel enhancement MOSFET, P-type body is shorted to the source terminal resulting in an intrinsic diode with anode at the source and cathode at the drain. While the MOSFET is turning off, the diode cannot conduct until it is forward biased. As the voltage across the MOSFET increases from near zero to the full input voltage V_{in}, it conducts the full output current. Once the diode is forward biased the current starts transferring from the MOSFET to the diode. During the reverse transition, first current is transferred from the diode to the MOSFET, and then the voltage across the MOSFET reduces from V_{in} to the conduction voltage drop. **Figure 7** shows the circuit arrangement for the proposed 5 step multilevel inverter. In this arrangement, Positive Staircase Voltage is obtained from the point where all the sources of MOSFETs are short circuited. Bridge circuit at the output stage provide positive

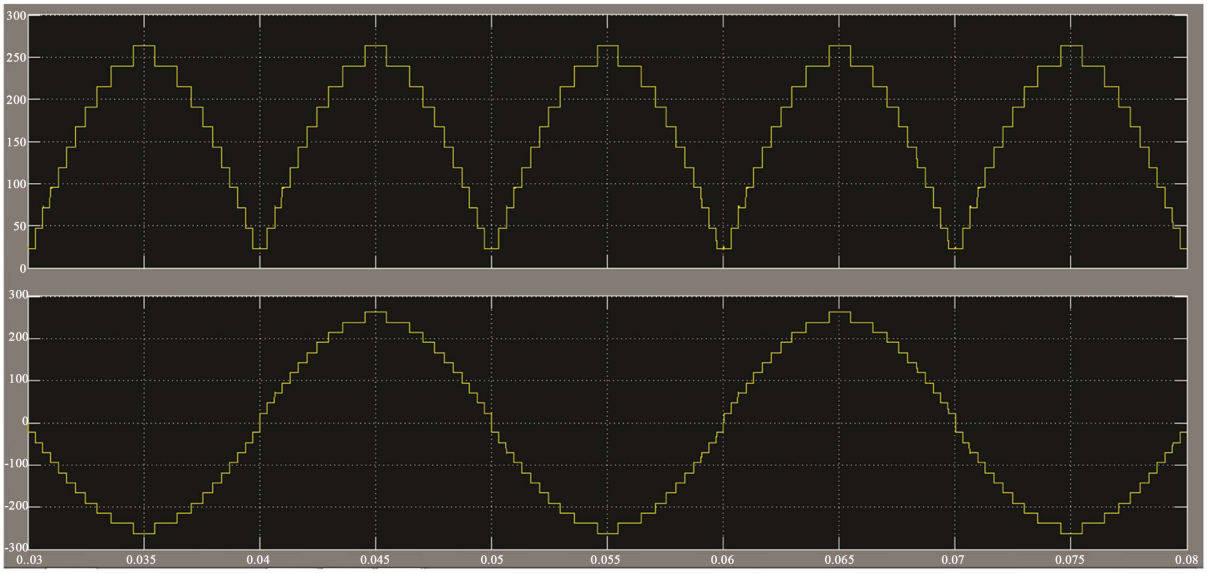

Figure 4. 11-step multilevel inverter.

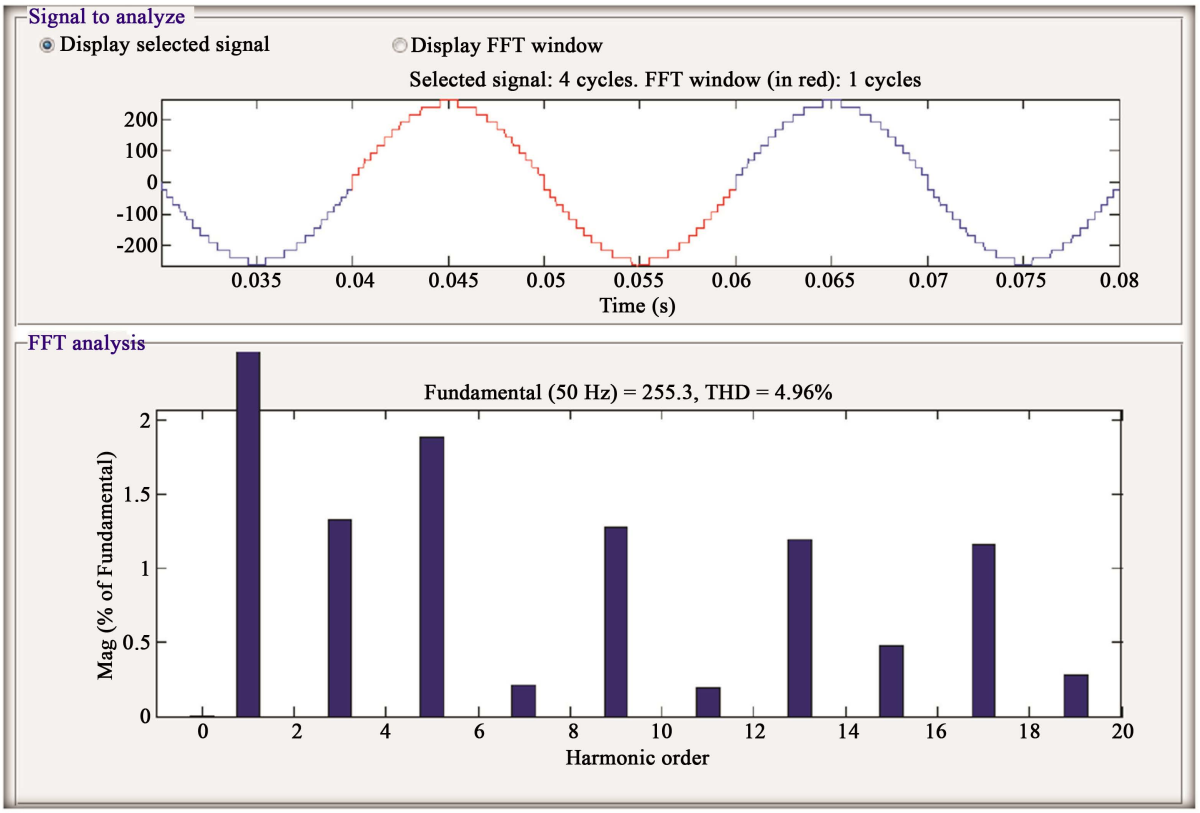

Figure 5. Voltage THD of 11-step multilevel inverter.

and negative half cycles to the load. Since the load is connected to the source side, there is a need of driver circuits. The drain of the first MOSFET in the array holds all the staircase values due to the effect of the body diode. Hence bridge circuit is fed from drain of the first MOSFET. To avoid power loss and ensure holding of positive side staircase voltage for the period of switching, a capacitor is connected between source point and ground. Proper selection of capacitor value is necessary to ensure non distorted waveform.

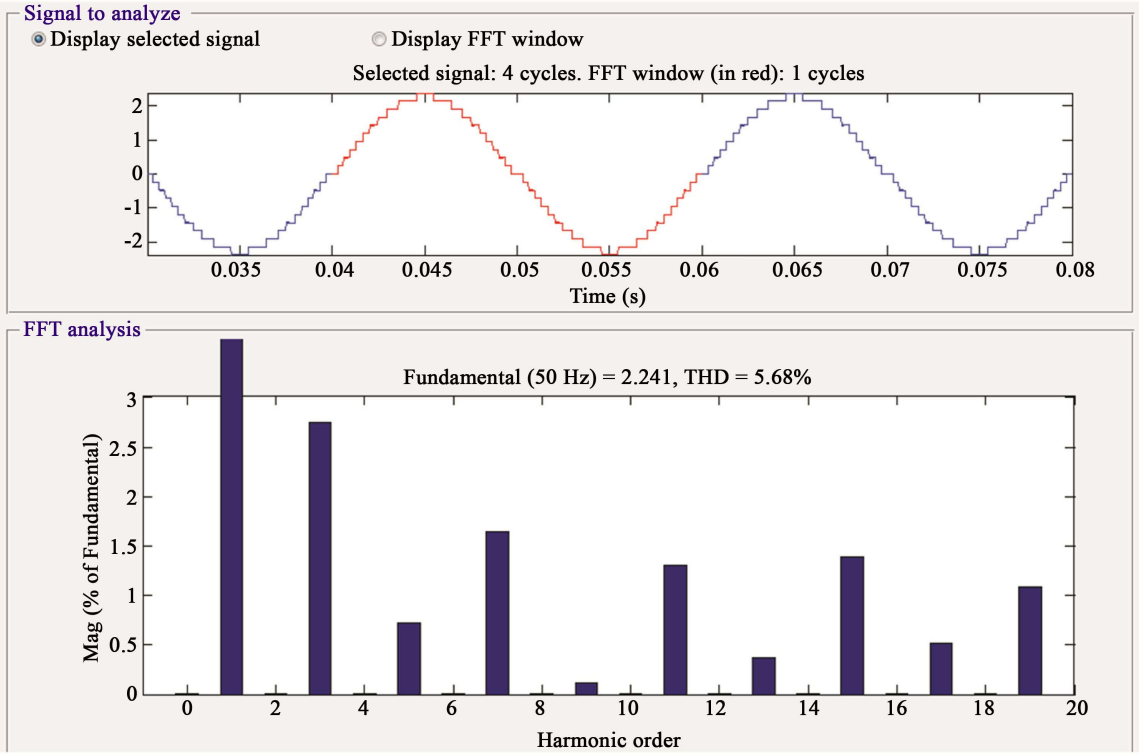

Figure 6. THD of 11-step multilevel inverter with inductive load.

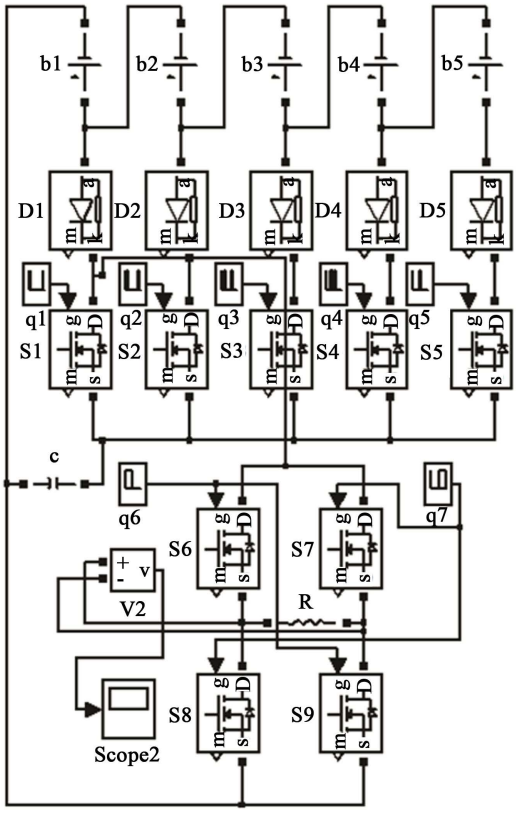

Figure 7. Simulation circuit arrangement of proposed 5-step multilevel inverter.

Figure 8 and **Figure 9** show the simulated output waveform and voltage at the drain of the first MOSFET and voltage THD.

Fundamental frequency = 50 Hz; Fundamental voltage = 104 Volts; Total Harmonic Distortion = 12.36.

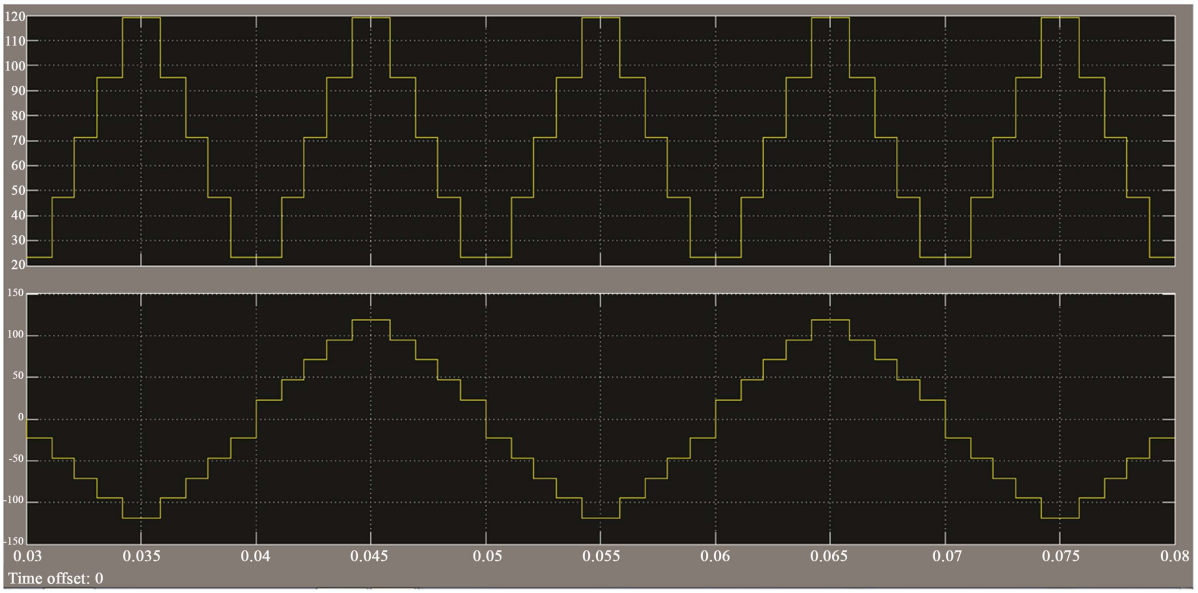

Figure 8. Output waveform-bridge and drain of first MOSFET.

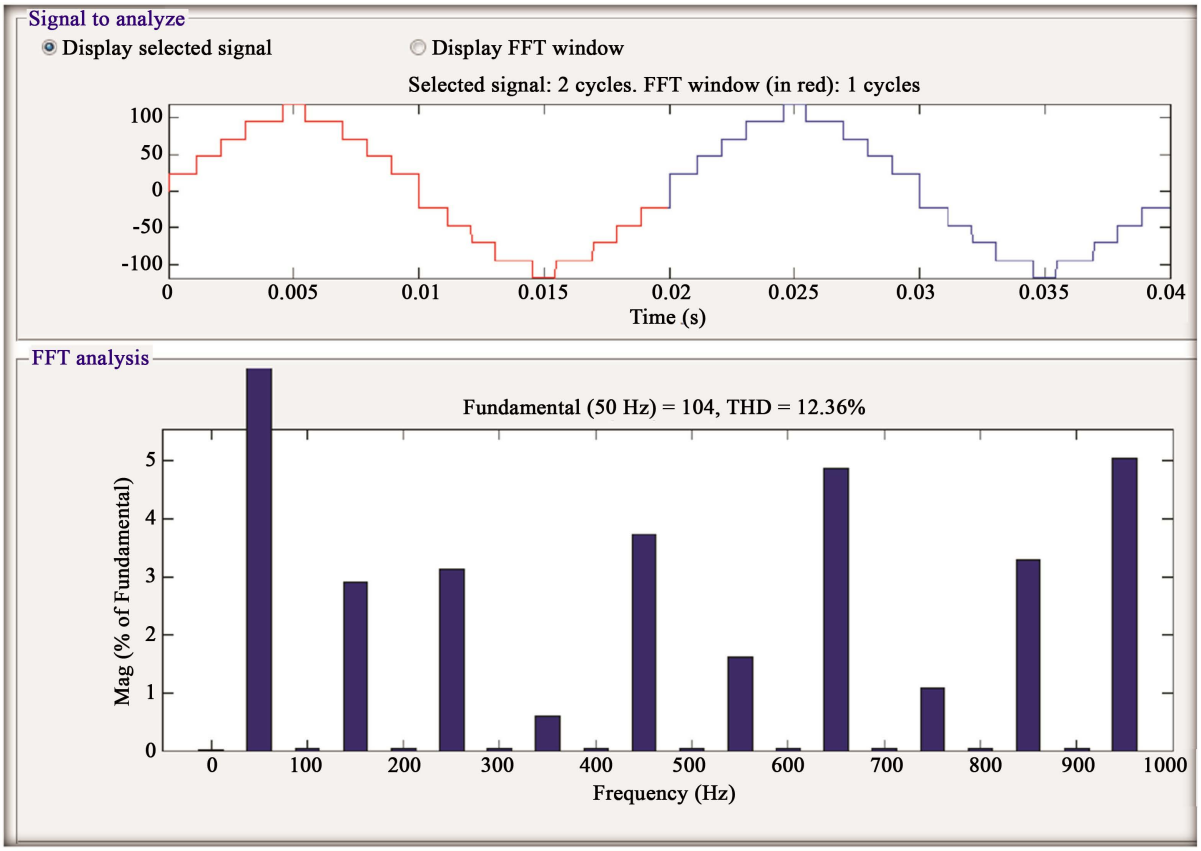

Figure 9. THD of 5-level multilevel inverter.

In the Sample (also commonly known as Track) mode, the voltage on the hold capacitor (C_H) follows the input signa-with a certain delay and bandwidth limitation. In the Hold mode, the capacitor is disconnected from the input signal and it is supposed to hold the voltage present before it was disconnected. In this circuit, holding capacitor operates in sample mode when switching devices ON and hold mode when switching devices OFF. The capacitor in the circuit is to hold the previous step voltage during the switching interval between the consecutive switching devices. Considering the switch off time of the MOSFET 1 msec interval is given from Arduino board.

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = \frac{i_c}{c} \tag{2}$$

To minimize or zero the capacitor current, the value of rate of change of voltage/msec multiplied by C value should approaches zero. The value of capacitance may ranges from 0.01 μF to 0.01μF.

Figure 10 represents the current through each switching devices in the proposed multilevel inverter. Current through the first switching device is the negative sum of the current flows through the switching devices. This is due to the fact that the current through each switching devices is accumulated in the source of the first switching device and delivered to the load through drain of the first device. **Figure 11** represents the current through capacitor (upper) connected in the source and load current (lower). The capacitor current, one which is not useful current, is less than 3% of the useful current. The required rating of switching devices is given in **Table 2**.

2.2. Experimental Setup for the Proposed Multilevel Inverter and Results

Figures 12-16 show the experimental setup for the proposed five step multilevel inverter, voltage at drain of the first MOSFET with high resistance and capacitance at the source while load is connected at the drain of the first MOSFET.

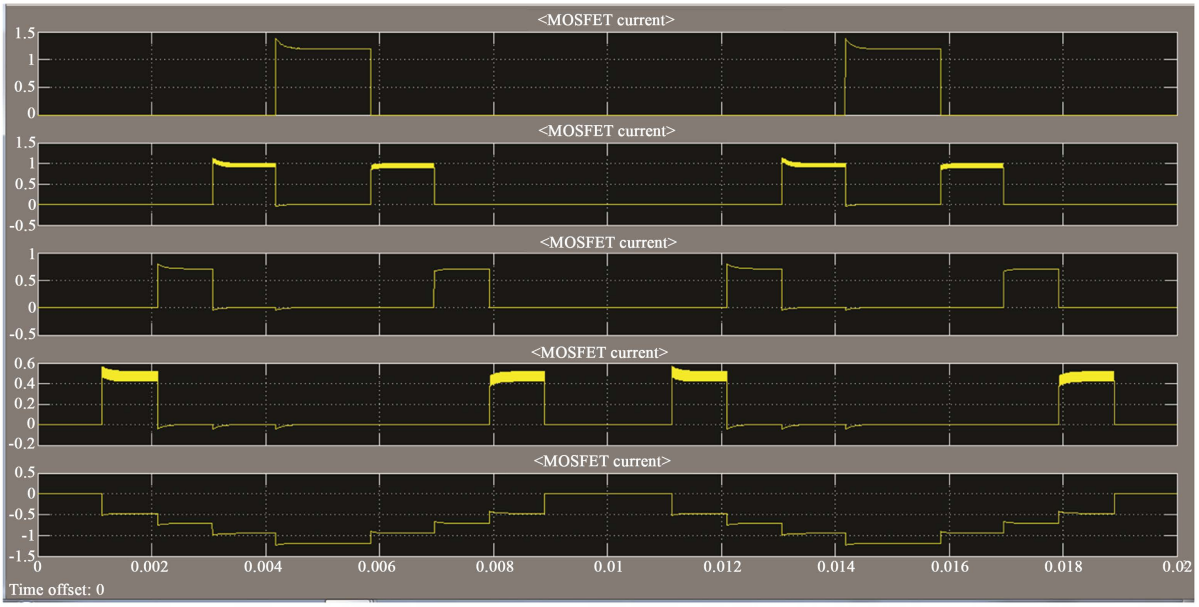

Figure 10. Current through switching devices and load.

Table 2. Switching devices and required current rating.

Switching Device	Current rating
Devices in the bridge circuit	Load current
Devices in the first and last levels	Load current
Devices in the mid levels	Less than load current

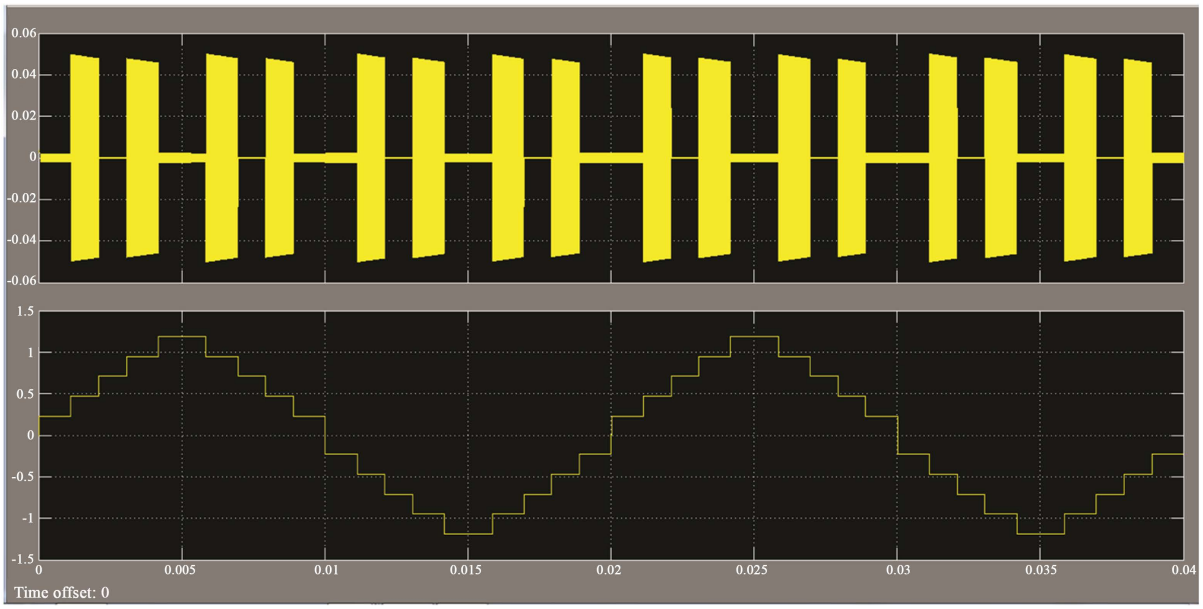

Figure 11. Current through capacitor and load.

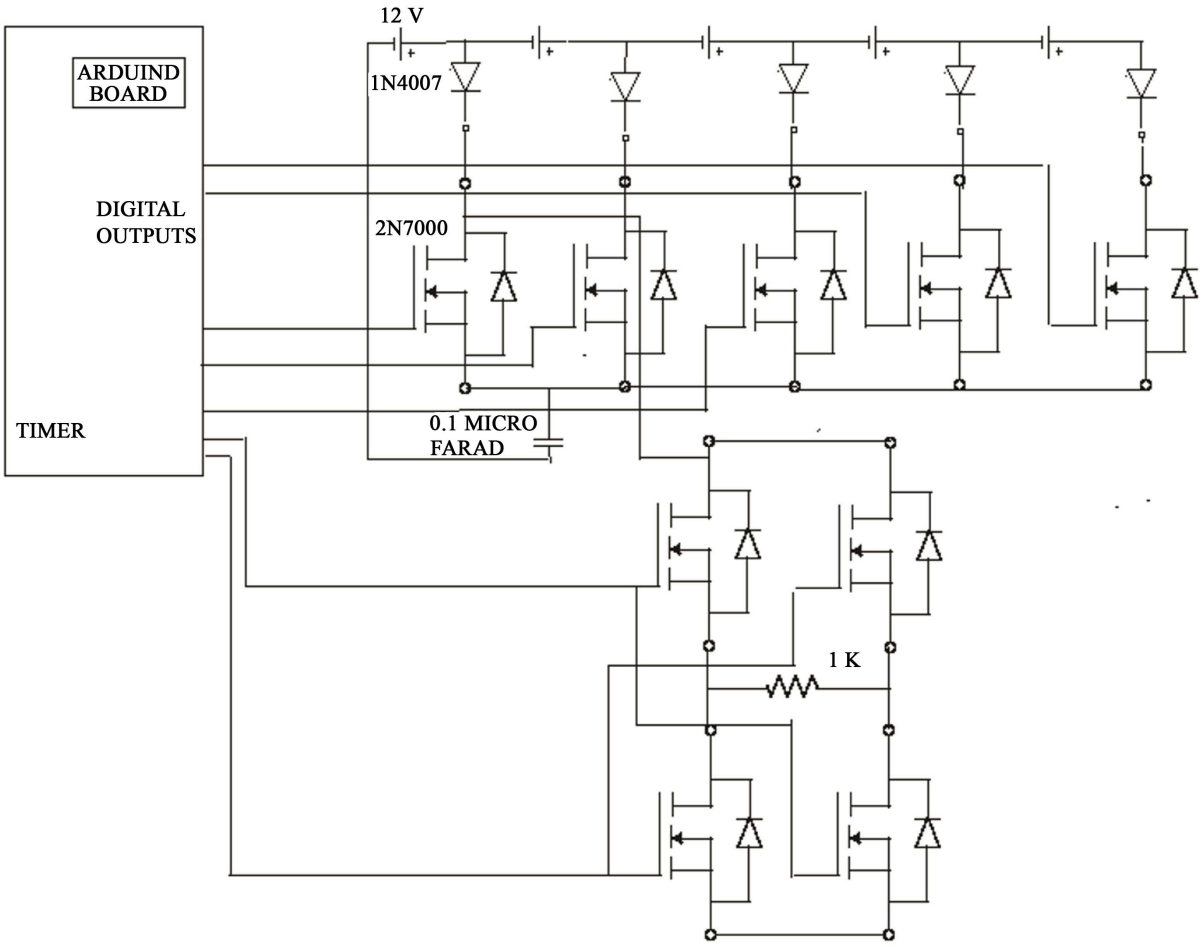

Figure 12. Circuit diagram of the proposed 5-step multilevel inverter.

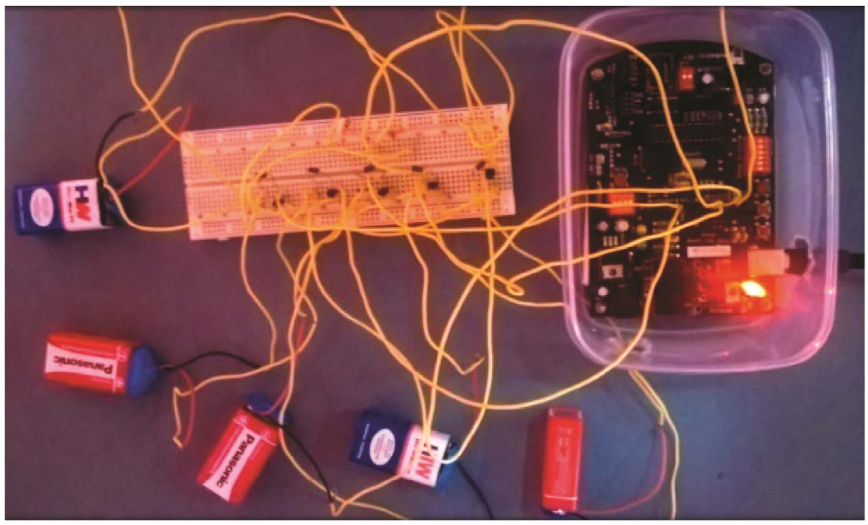

Figure 13. Experimental setup for five-level multilevel inverter.

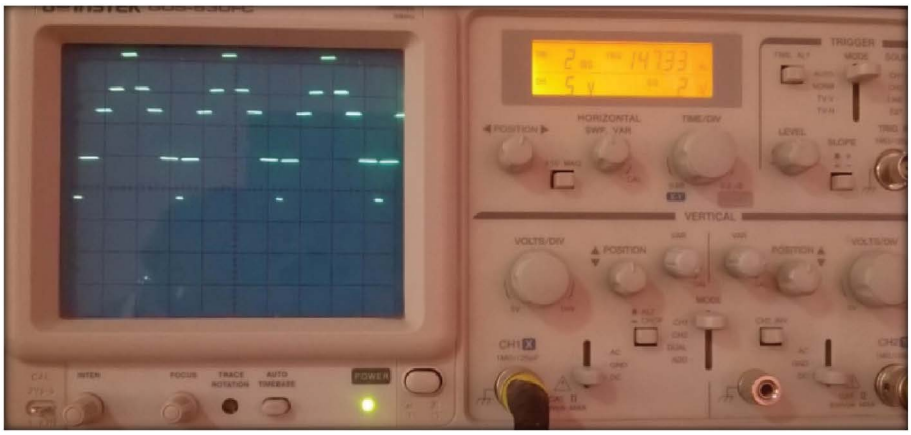

Figure 14. Voltage at the drain of the first MOSFET with resistance at source.

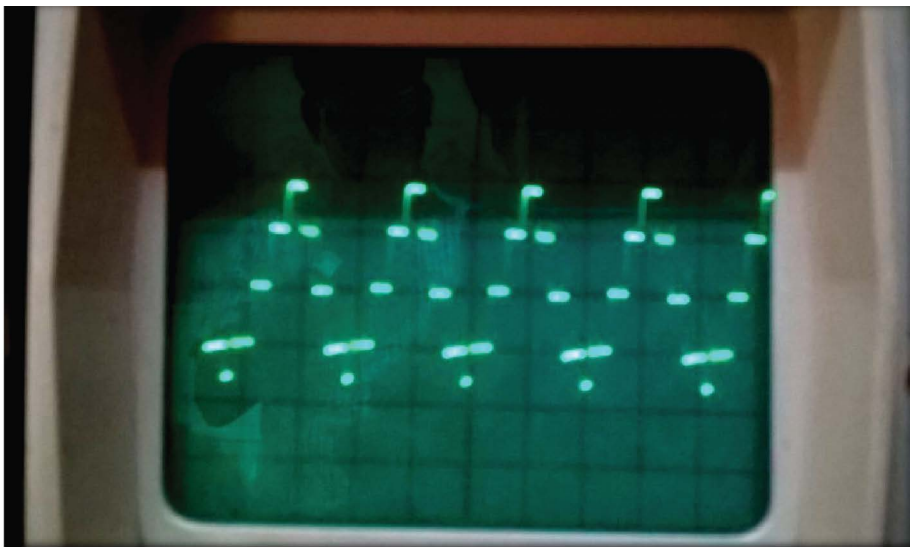

Figure 15. Voltage at the drain of the first MOSFET with capacitance at source.

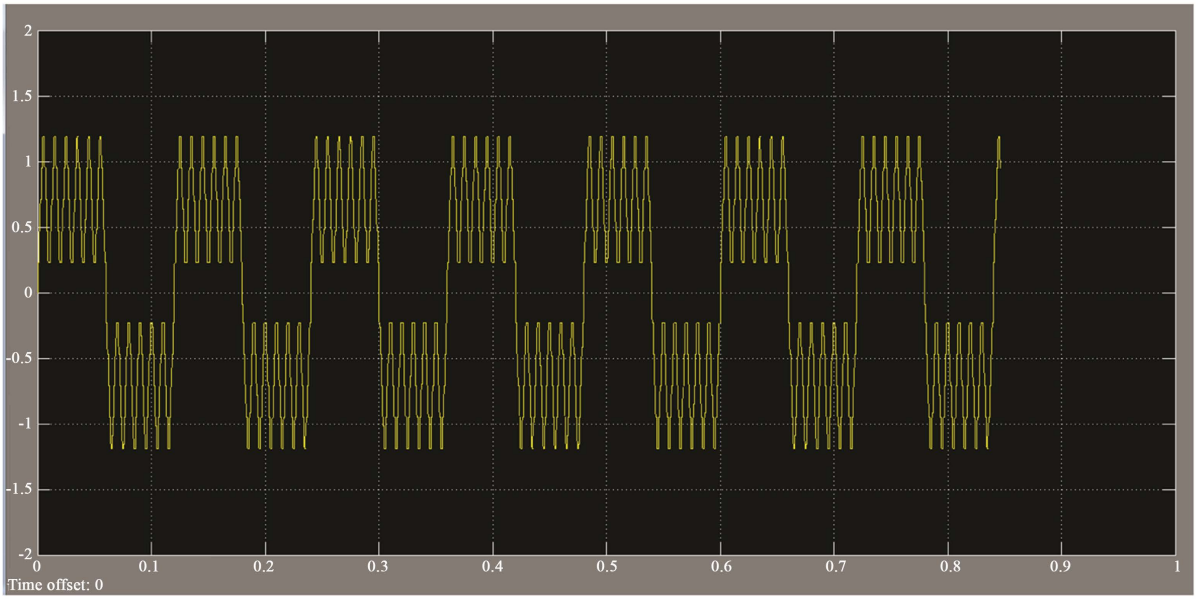

Figure 16. Submultiple frequency current waveform.

Circuit Components:

N Channel MOSFET 2N7000 (0.2A, 60 Volts); Capacitor 0.1 µF/100 Volts; Arduino Board for gate pulse input; 9 Volt Batter 5-No.

When resistor is connected between sources and ground, power loss occurs in it and the stepped voltage is discontinuous. When capacitor is connected, the power loss is very much less (less than 3%) and rising edge of the stepped voltage is continuous.

2.3. Cycloconverter Operation

Cycloconverter converts ac power frequency into submultiples of power frequency by ac-ac conversion without an intermediate link. In the proposed multilevel inverter, only positive stepped sine waveform is available at the drain of the first MOSFET of the multilevel inverter. At the bridge stage, the sub multiple frequency of the base frequency generated by the single switch multilevel inverter stage could be obtained. **Figure 15** represents cycloconverter simulated using the proposed multilevel inverter for the submultiple frequency of 6, *i.e.* 50/6.

3. Half Bridge Multilevel Inverter for High Frequency Induction Heating

The induction heating power supply adopting cascaded multilevel inverter with improved quality of output voltage in induction heating power supply inverter, a harmonics control mean of output voltage by selecting switching angles were presented in [7]. Single switch multilevel inverter is not suitable for this application. In this paper Half bridge multilevel inverter is suggested for this high frequency application. Figure shows the simulation circuit based on half bridge multilevel inverter. The half bridge multilevel inverter consists of half bridge and centre tapped stand alone dc sources for each level and a common half bridge and centre tapped stand alone dc source with voltage of $n*V_{dc}$ where n is the number of steps and V_{dc} is the voltage of each dc source. **Figures 17-19** represents the high frequency half bridge inverter simulation circuit, current waveform and voltage THD.

Simulation Parameters:

Frequency 50 KHz; Inductor $2.733e^{-6}$ Henry; Coil resistance 0.1165 Ohm; Capacitor $3.7\ e^{-6}$ Farad Smoothing inductor 10 mH.

4. Conclusion

This work proposes a multilevel inverter with reduced number of switches and driver circuits by using single

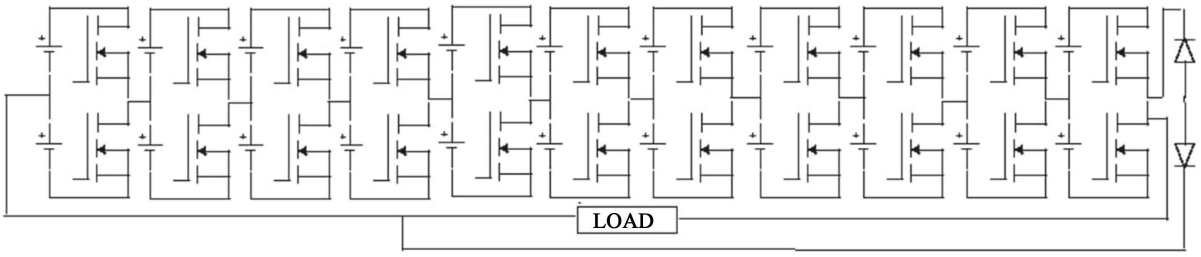

Figure 17. 10-step half bridge inverter for induction heating.

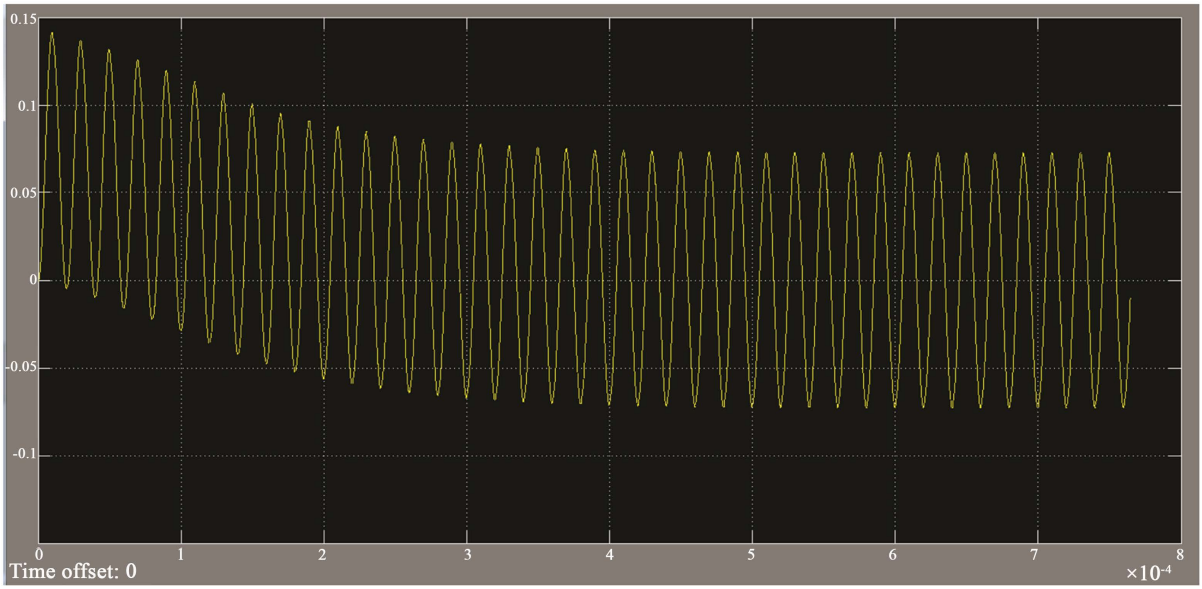

Figure 18. Current waveform of half bridge inverter.

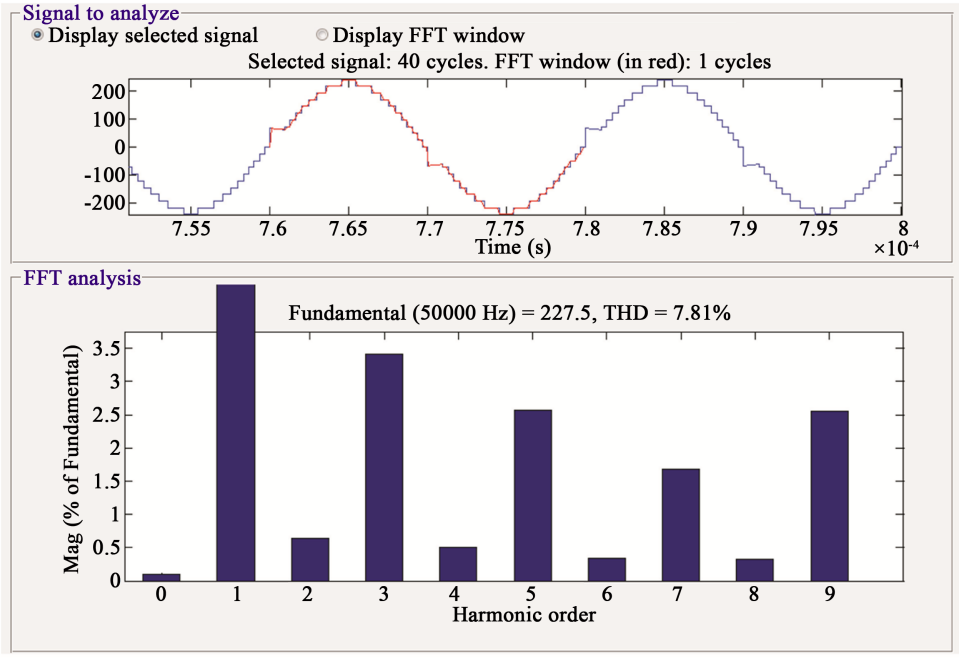

Figure 19. Voltage THD of half bridge inverter.

switch for each step and the effect of body diode in the MOSFET. The circuit is simulated and verified by experimental setup. Total harmonic distortion of voltage and current is within the limit of IEEE standard. Submultiple frequency at the H-bridge stage is obtained by simulation. A half-bridge multilevel inverter is simulated for high frequency applications.

5. Future Work

The multilevel inverter used in ups system is based on multi-winding transformer with one primary and several output coils, thus producing several partial AC square waveforms. The inverter output stage combines these partial voltages in order to produce the sinusoidal output voltage. The multilevel inverter proposed in this work is suitable to design a multilevel inverter for ups without using multi-winding transformer and is to be tested.

Solar based single phase motor drive application using the proposed multilevel inverter is to be tested.

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