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Improved PLL Tuning of Shunt Active Power Filter for Grid Connected Photo Voltaic Energy System

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Abstract

This research work brings out the unique predictive current control method for attaining an efficient grid connected Photo Voltaic (PV) system by Shunt Active Power Filter (SAPF) as grid connected converter. The major objective of the research work is to address the presence of Direct Current (DC) component, frequency improvement, quicker theta response, voltage magnitude estimation in the input signal of the Phase Locked Loop (PLL) which is challenging. This work focuses on tuning the PLL block (K_p, K_i, K_v and K_o) through Artificial Bee Colony (ABC) optimization algorithm. The proposed ABC based modified three-phase PLL method is based on adding a new loop inside the PLL structure. In power converters, ABC algorithm is used to select the optimal switching states. The voltage vector which minimizes a cost optimization function is selected. Simulation is carried out for both balanced and unbalanced system and the results validate that the performance of the proposed approach is better in terms of harmonic compensation as per the IEEE standards within ±5%, power factor improvement of the system, quicker theta tracking and suppression of frequency jump with the interconnection of PV system.

Keywords

Shunt Active Filter, Phase Locked Loop, Artificial Bee Colony, Current Control Method, PV System

1. Introduction

In recent years, power quality at end user's terminal is affected greatly and it has become a great concern in

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many industrial applications. Therefore, it is very essential to identify novel and efficient system that would mitigate the disturbances in the electrical systems, improving their power quality [1]. Normal filters such as LC, LCL, etc., are used to eliminate specified frequency range and thus, it can be only used for predetermined loads. Thus, Active Power Filter (APF) has been used for these types of harmonic mitigation concerns in transmission lines [2].

Shunt active power filter has the growing popularity than series active power filter since most of the industrial applications require the compensation towards current harmonics. It has the ability to keep the current in the source as balanced and sinusoidal after compensation, irrespective of whether the load is nonlinear, balanced or unbalanced [3]-[5]. The utilization of SAPF provides significant advantages to the power system. Thus, developing new methodologies have become an active area of research to improve the performance of these SAPFs [6].

In recent decades, interconnection of Renewable Energy Sources (RES) with SAPF has become one of the attractive research topics. But, there is a certain level of influence and impact that renewable generation has on power quality on account of its nonlinearity, especially as both solar generation plants as well as wind power generators have to be connected as such with the grid using high power static Pulse Width Modulated (PWM) converters [7]. Power generation in non uniform nature has a direct effect on the voltage that is regulated therein and thus leads to voltage distortion in power systems. This paper focuses on contributing an efficient compensation technique to deal with the problem of power quality disturbances in the power distribution systems due to the RES interconnection.

Many types of active power filter configurations have been proposed in the last two decades to achieve the required harmonic compensation level. The main techniques in the active filter are to generate the reference current and the control method applied to inject the required compensation current into the line, which decides the performance of an active filter. There are several methods for reference current generation for the shunt active power filters. In 1984, H. Akagi stated instantaneous active and reactive power theory control method that was quite efficient method for three phase loads in the balanced system, being later worked by Watanabe and Aredes for three phase four wire systems; later F.Z. Peng proposed zero sequence currents. Synchronous Reference Frame (SRF) concept is simple algorithm having good dynamic responses. The SRF could compensate the harmonics in the current and reactive power component from the distorted load currents.

In 1995, Bhattacharya proposed dq component's calculations of the instantaneous three phase currents and created synchronous reference frame concept. A dq based current reference generator scheme is used to obtain the reference current signal of the active power filter. This scheme presents a fast and accurate signal tracking capability, which avoids voltage fluctuations that deteriorate the current reference signal affecting compensation performance [8]. So, in this work, dq based current reference generator scheme is preferred.

To implement the dq based current reference generator, some kind of synchronizing system should be used. PLL has been widely used for the synchronization purpose. SRF-PLL has been widely used in power system applications due to its simplicity and considerable performance. But it suffers from double frequency error when the input signal is unbalanced. Moreover, it also has drawbacks due to the presence of DC components. The DC component can be an intrinsic component of a signal (e.g., the DC link voltage in a single phase rectifier that has a DC and a second order harmonic), and can be generated by measurement devices (e.g., due to the saturation phenomenon in a current transformer [9]), conversion processes (e.g., the A/D conversion for fixed point DSP applications [10]), or when a fault occurs [11]. Therefore, it is necessary to remove any error that such a component may cause. But, complete removal of DC component in the PLL systems has not been addressed in the literature so far [12].

In this paper the author proposed a method to address the DC component in the input signal of the PLL and notch filter algorithms for filtering and synchronization applications. This paper takes the motivation of the abovementioned work and focuses on improving the performance of the overall system through the utilization of swarm intelligence optimization algorithm.

Traditional PI controllers are widely used in the control loop of the voltage source converters to produce the switching states of the converters because of its simplicity in control design. Perfect tuning of the controller is needed to have the satisfactory operation of the converters and several traditional tuning rules, such as Ziegler and Nichols, Astrom and Hagglud, Sain and Ozgen cohen and coon etc. are adopted for this purpose. Though they are enough for the first order system, they produce large overshoot and required repeated design process for any variations in the system model. But in general the power system has many disturbances, parameter varia-

tions and has many nonlinear loads which lead to the degradation of the quality of the power. Hence the continuous tuning algorithm is needed to have satisfactory operation in its dynamic nature [13]-[16]. Hence this paper brings out the unique optimized self tuning of the controller for the PLL structure in the current control loop of the VSCs, which is obtained by ABC algorithm.

The main contribution of this paper is to tune the PLL block parameters such as proportional gain (K_p), integral gain (K_i), change in the instantaneous frequency (K_o) and voltage magnitude gain (K_v). The settling time and the steady state response of the frequency are tuned by K_i and K_p gain values. Similarly, elimination of DC component and identification of the voltage magnitude are tuned through K_o and K_v gain values through the ABC optimization approach. Moreover, the control loop of Voltage Source Inverter (VSI) is proposed with the predictive current control approach. This method predicts the future load current values for the voltage vectors generated by the inverter. The voltage vector which minimizes a cost optimization function is selected. The cost optimization function used in this work evaluates the error current at the next sampling time. In order to select the optimal switching state that must be applied to the power converter, ABC optimization is used in this work which selects the best minimal optimal value "g".

This paper is organized as follows. Section 2 deals with the proposed methodology. Section 3 discusses about the three leg converter model. Section 4 describes about the proposed ABC based predictive current control model. Section 5 narrates about current reference generation. Section 6 validates the simulation results to proof the performance of the proposed system.

2. Proposed Methodology

Figure 1 shows the proposed SAPF system model with RES interconnection. The electrical energy consumption behaviour is an unpredictable, and random in nature. It may be single or three-phase, balanced or unbalanced, and linear or nonlinear. A shunt active power filter is connected at the point of common coupling in parallel to compensate current harmonics, current unbalance, and reactive power [17]. As shown in **Figure 1**, it is composed by an electrolytic capacitor, a PWM converter and a first order output ripple filter. This circuit utilizes the power system equivalent impedance Z_s, output ripple filter impedance Z_f of the converter and the impedance Z_L of the load. When RES generates excess power than the load demand, then the excess power is given to the grid to maintain the load voltage of frequency constant.

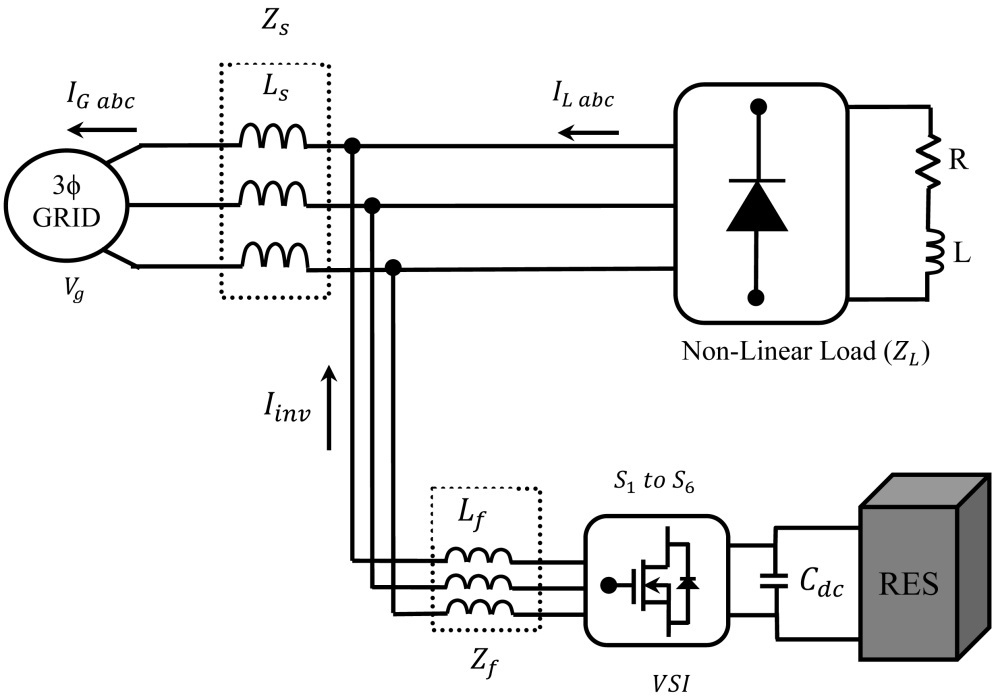


Figure 1. Shunt active power filter model.

The main element of this system is a voltage source inverter, as it interfaces the renewable energy source to the grid and delivers the generated power. In this work, grid interfacing inverter can effectively be utilized to perform the following important functions: 1) non linear load current harmonics mitigation; 2) unbalanced current compensation in case of 3 phase 3 wire system; 3) ABC based Predictive control technique for cost optimization 4) ABC based PLL tuning approach under unbalanced load conditions. Moreover, with adequate control of grid interfacing inverter, all the four objectives can be accomplished either individually or simultaneously.

3. Three Leg Converter Model

An illustration of converter's power circuit employed here is presented in **Figure 2**. Converter topology has similar features to those of traditionally deployed three phase converter that has a three leg system [18]. The switching states of the converter are decided by the gating signals S_u, S_v and S_w, as follows in Equation (1):

$$\begin{aligned} S_u &= \begin{cases} 1 \text{ if } S_1 \text{ ON and } S_2 \text{ OFF} \\ 0 \text{ if } S_1 \text{ OFF and } S_2 \text{ ON} \end{cases} \\ S_v &= \begin{cases} 1 \text{ if } S_2 \text{ ON and } S_5 \text{ OFF} \\ 0 \text{ if } S_2 \text{ OFF and } S_5 \text{ ON} \end{cases} \\ S_w &= \begin{cases} 1 \text{ if } S_3 \text{ ON and } S_6 \text{ OFF} \\ 0 \text{ if } S_3 \text{ OFF and } S_6 \text{ ON} \end{cases} \end{aligned} \tag{1}$$

and Equation (1) can be expressed in vectorial form as in Equation (2).

$$S = \frac{2}{3\left(S_u + aS_v + a^2 S_w\right)} \tag{2}$$

where $a = \mathrm{e}^{\frac{j2\pi}{3}}$.

The output voltage space vectors created by the inverter are defined as in Equation (3)

$$v_i = \frac{2}{3\left(v_u N + a v_v N + a^2 v_w N\right)} \tag{3}$$

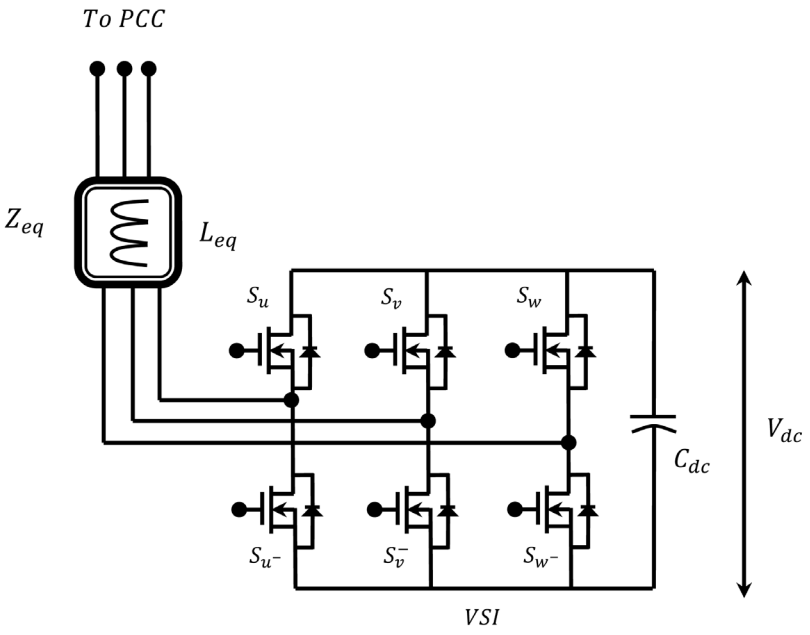


Figure 2. Three leg inverter.

where $v_uN + av_vN + a^2v_wN$ are the phase to neutral (N) voltages of the inverter (**Figure 2**). Then, the load voltage vector can be related to the switching state vector S as in Equation (4)

$$v = V_{dc}S \tag{4}$$

where V_{dc} is the DC link voltage.

Taking in to consideration gating signals combinations of S_u, S_v and S_w eight switching states, and as a result, eight voltage vectors are thus obtained. Note that $v_o = v_7$, which results in only seven different voltage vectors, as shown in **Figure 3**. Filter's mathematical model derivation is given in Equation (5).

$$v_o = v_i - R_{eq}i_0 - L_{eq}\frac{\mathrm{d}i_o}{\mathrm{d}t} \tag{5}$$

where R_{eq} and L_{eq} are the 3L-VSI output parameters expressed as Thevenin impedances at the converter output terminals Z_{eq}. Hence, the Thevenin's equivalent impedance is calculated by a series connection of the ripple filter impedance Z_f and the arrangement in parallel between the system equivalent impedance Z_s and the load impedance Z_L as shown in Equation (6).

$$Z_{eq} = \frac{Z_S Z_L}{Z_S + Z_L} + Z_f \tag{6}$$

For this model, it is assumed that $Z_L \gg Z_S$, and the resistive part of the system's equivalent impedance is neglected, and the series reactance is considered in the range of 3% - 7% p.u., which is a satisfactory approximation of the real system. Finally, in Equation (5) $R_{eq} = R_f$ and $L_{eq} = L_s + L_f$. For complete understanding the PWM switching time calculation of the inverter switches are given in **Table 1**.

Table 1. Switching time calculation of the inverter.

Sector	Switching time vector
1	$S_1 = T_1 + T_2 + (0.5 \times T_0)$ $S_2 = T_2 + (0.5 \times T_0)$ $s_3 = (0.5 \times T_0)$
2	$S_1 = T_1 + (0.5 \times T_0)$ $S_2 = T_1 + T_2 + (0.5 \times T_0)$ $s_3 = (0.5 \times T_0)$
3	$S_1 = T_1 + (0.5 \times T_0)$ $S_2 = T_1 + T_2 + (0.5 \times T_0)$ $s_3 = T_2 + (0.5 \times T_0)$
4	$s_1 = (0.5 \times T_0)$ $S_2 = T_1 + T_2 + (0.5 \times T_0)$ $S_3 = T_1 + (0.5 \times T_0)$
5	$s_1 = T_2 + (0.5 \times T_0)$ $S_2 = (0.5 \times T_0)$ $S_3 = T_1 + T_2 + (0.5 \times T_0)$
6	$s_1 = T_1 + T_2 + (0.5 \times T_0)$ $S_2 = (0.5 \times T_0)$ $S_3 = T_2 + (0.5 \times T_0)$

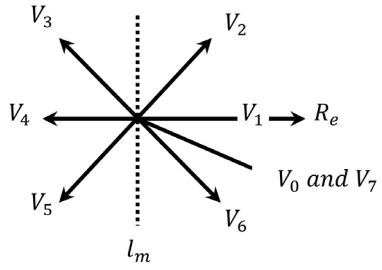


Figure 3. Voltage vector generated by the inverter.

3.1. Design of DC Link Capacitor

The value of dc link capacitor is chosen from the reference dc voltage, ($V_{\text{dlink}-\max}$) is the maximum voltage level of the dc bus, I is the phase current of VSI, ω is the angular frequency and (t) time for which dc bus voltage is to be recovered. It is given as in Equation (7).

$$C_{dc} = \pi \times \frac{I_c(\text{rated})}{\sqrt{3} \times \omega t \times V_{\text{dlink}-\max}} \tag{7}$$

where $\omega = 2\pi \times 50 = 314.159$; $I_{c(\text{rated})}$ = rated current, $V_{\text{dlink}-\max} = 700$ V

3.2. Design of Filter Inductance

The amount of filtering inductance to be added to the SAPF is

$$L_f = \frac{V_{\text{dlink}}}{2 \times \left(\Delta I_{rip-peak}\right) \times f_{sw-\max}} \tag{8}$$

where (V_{dlink}) represents dc link voltage, ($f_{sw-\max}$) represents maximum switching frequency, ($\Delta I_{rip-peak}$) represents peak to peak ripple current. $V_{\text{dlink}} = 700$ V, $\Delta I_{rip-peak} = 11.6$ Amps, $f_{sw-\max} = 30000$ Hz $= 30$ kHz.

4. Predictive Current Control

Figure 4 shows the block diagram of the proposed predictive current control scheme. Predictive control is characterized by its system model usage that helps in predicting variables for future behaviour that necessitates controlling. Controller utilizes the particular information in order to choose the optimum switching state which in turn will be applied to the power converter, as per predefined optimization decisive factors.

4.1. Current Reference Generator

It is derived and designed so that the required current reference may be generated and the same may be utilized for compensating any undesirable load current components. With respect to this one, system voltages, DC link voltage of converter as well as the load currents are measured. During the unbalanced current/voltage conditions, PLL tuning is required. But, in order to improve the conventional PLL tuning, an intelligent ABC optimization algorithm is used in this approach

4.2. Predictive Model Using ABC

Converter model is employed for prediction of output current of the converter. Implying that considering a given sampling time T_s, identifying converter switching states and control variables at instant kT_s, prediction of next states is feasible at any instant $(k+1)T_s$. On account of first order nature that is inherent in state Equations (3-6) that entail details of the model, a relatively accurate first order approximation of the derivative has been taken in to consideration here as in Equation (9).

$$\frac{\mathrm{d}x}{\mathrm{d}t} \approx \frac{x(k+1) - x(k)}{T_s} \tag{9}$$

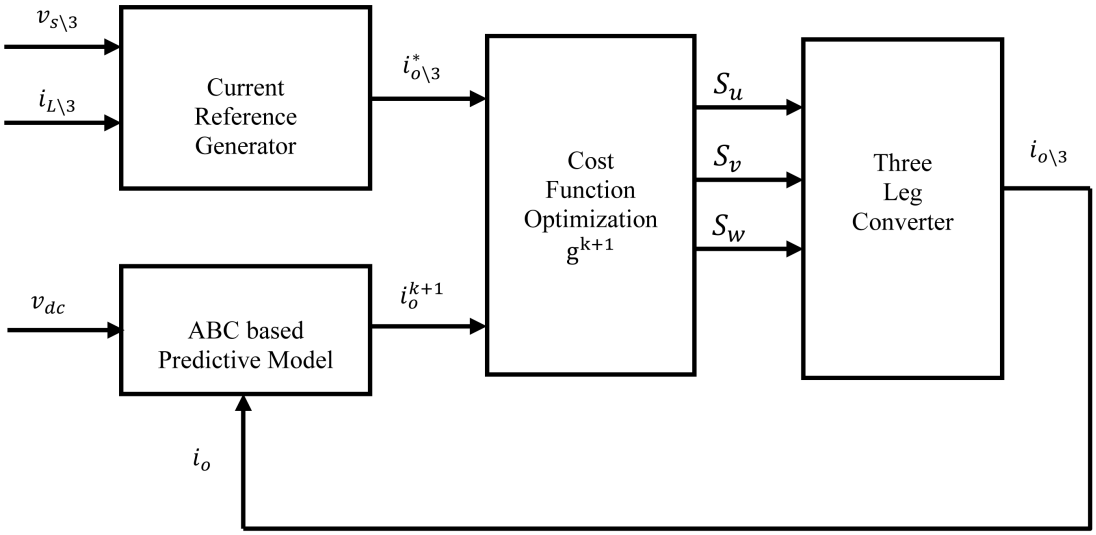


Figure 4. Proposed ABC based predictive current control scheme.

4.3. Proposed ABC Algorithms for Optimal Switching of the Converter

In [19] the authors proposed the Artificial Bee Colony algorithm wherein each of the colonies comprises of three groups the employed, the onlookers and the scouts. A random switching state $(V_1,\cdots,V_8)$ is initialized and each solution vector is generated. Then, each employed bee found new sources whose quantity is equal to half of the total sources. The main purpose for determining the new food source is evaluation of nectar amount and subsequently greedy selection is carried out. In ABC, both employed and onlooker contribute as being part of the operation and scouts carry out exploration. Bees aim at maximizing food quantity brought back into the nest.

Step 1: Generate the initial switching state V_i, where $i = 0,1,2,\cdots,7$

Step 2: Calculate the voltage for each switching state (particle) to obtain output voltage for each switching state V (P_i), and select the best $\theta_k(c)$ as P_i.

Evaluate the fitness (output voltage for each switching state) ($f_i = P_i$) of the switching state

Step 3: Use the iteration formulae of ABC to get a new routing path.

For each employed bee Do

Produce new solution X_i of switching state of the inverter

Calculate the value f_i of switching state of the inverter

Apply greedy selection process

Calculate the probability values P_i for the solutions V_i

For each onlooker bee

Select a solution V_i depending on P_i

Produce new solution X_i

Calculate the values f_i Apply greedy selection process

If there is a discarded solution for the scout then replace it with a new solution which will be randomly produced.

Memorize the best solution so far.

The algorithm iterates to the preferred cycle number and the sources having the best nectar in mind gives the possible values of the variables. The obtained nectar amount denotes the solution of the objective function. The 8 possible output current predicted values can be obtained as in Equation (10)

$$i_o[k+1] = \frac{T_s}{L_{eq}}\left(v_i[k] - v_o[k]\right) + \left(1 - \frac{R_{eq}T_s}{L_{eq}}\right) i_0[k] \tag{10}$$

As shown in Equation (10), in order to predict the output current i_o at the instant $[k+1]$, the input voltage value v_i and the converter output voltage v_o are required. The algorithm calculates all 8 values associated with the possible combinations that the state variables can achieve.

4.4. Cost Function Optimization

Selection of optimal switching state applicable to power converter requires, comparison of 8 predicted values obtained for $i_o[k+1]$ with reference by deploying a cost function g, as follows in Equation (11).

$$g[k+1] = \left(i^*_{ou}[k+1] - i_{ou}[k+1]\right)^2 + \left(i^*_{ov}[k+1] - i_{ov}[k+1]\right)^2 + \left(i^*_{ow}[k+1] - i_{ow}[k+1]\right)^2 \quad (11)$$

Here $g[k+1]$ represents the error difference between the actual filter currents i_{oa}, i_{ob} and i_{oc} and the reference filter currents i^*_{oa}, i^*_{ob} and i^*_{oc}. The output current i_o is equal to the reference current i^*_o when g = 0. Therefore, the main goal of the cost optimization is to achieve the g value close to zero. Voltage vector $v \times N$ is selected as it reduces cost function and applicable for subsequent sampling state. Through each sampling state, switching state generating minimum value of g is chosen amongst 8 probable function values. Algorithm chooses that switching state which generates minimal value and then the same is applicable to the converter during the $[k+1]$ state. An accurate and fast detection of the theta and frequency is essential to assure the correct generation of the reference signals. So, in this work, ABC optimization is used in PLL to optimize its parameters $(K_p, K_i, K_v$ and $K_o)$ to obtain better steady state response, settling time, voltage magnitude and DC component elimination.

5. Current Reference Generation

DQ based reference current generation scheme has been employed here to attain active power filter current reference signals. The scheme offers quick and precise signal tracking capabilities. This particular feature negates voltage fluctuations deteriorating reference current signal that influence compensation performance [8]. **Figure 5** shows how reference current signals are attained through matching load currents. This module calculates the necessary reference current signals for the converter so as to compensate reactive power, current harmonic & current imbalance respectively. The displacement power factor $(\sin(\varnothing_L))$ and the maximum Total Harmonic

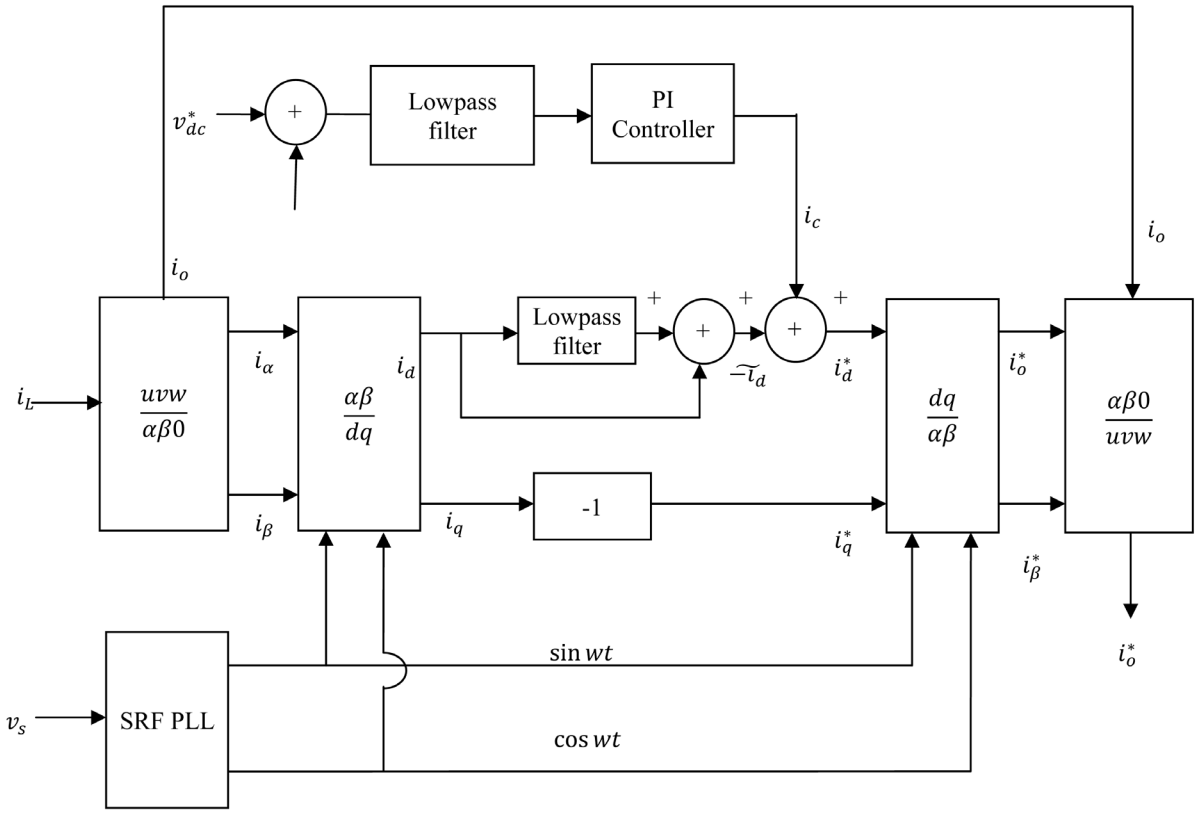


Figure 5. dq based reference current generator.

Distortion (THD) of the load THD_L defines the relationships between the apparent power needed by the active power filter, with related to the load, as shown in Equation (12)

$$\frac{S_{APF}}{S_L} = \frac{\sqrt{\sin \varnothing_L + THD_L^2}}{\sqrt{1+THD_L^2}} \tag{12}$$

where the value of THD_L includes the maximum compensable harmonic current, defined as double the sampling frequency f_s. The frequency of the maximum current harmonic component to be compensated is equal to one half of the converter switching frequency.

DQ based scheme is operational as part of the rotating reference structure, hence measured currents need to be multiplied using $\sin \omega t$ and $\cos \omega t$ signals. Deployment of dq transformation, d current component synchronization needs to be done with respect to corresponding phase to neutral system voltage; q current component is phase shifted by 90˚. Obtaining $\sin \omega t$ and $\cos \omega t$ synchronized reference signals are done using SRF-PLL [20]. A pure sinusoidal waveform is generated by the SRF-PLL when there is severe distortion in system voltage.

Eliminating of tracking errors is feasible as SRF-PLLs are designed so that phase voltage unbalancing is evaded, harmonics (*i.e.*, less than 5% and 3% in fifth and seventh, respectively) and resultant offset generated on account of nonlinear load conditions and measurement errors.

Thus, for the complete removal of DC component and sudden response of frequency ABC is used in this work to tune the PLL block $\left(K_p, K_i, K_v \text{ and } K_o\right)$. The settling time and the steady state response of the frequency are tuned by K_i and K_p gain values. Similarly, elimination of DC component and identifying the voltage magnitude are tuned through K_o and K_v gain values through the ABC optimization approach.

Equation (13) shows the relationship between the real currents $i_{Lx}(t)$ where $x = u, v$ and w and the associated dq components (i_d and i_q) is

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin \omega t & \cos \omega t \\ -\cos \omega t & \sin \omega t \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{Lu} \\ i_{Lv} \\ i_{Lw} \end{bmatrix} \tag{13}$$

The DC component of the phase currents i_d is extracted by a Low Pass Filter (LPF) to generate the harmonic reference components $-\widetilde{i_d}$. The corresponding Alternating Current (AC) and DC components of i_q are phase shifted by 180˚ to obtain the reference components (reactive) of the phase currents. Maintaining DC voltage constant, the amplitude of the converter reference current should be modified by adding an active power reference signal i_c with the d component discussed below. The resulting signals i_d^* and i_q^* are transformed as three phase signals by applying the inverse Park and Clark transformation, as shown in Equation (14). In this paper the cut off frequency of the LPF is used as 20 Hz.

$$\begin{bmatrix} i_{ou}^* \\ i_{ov}^* \\ i_{ow}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \sin \omega t & -\cos \omega t \\ 0 & \cos \omega t & \sin \omega t \end{bmatrix} \begin{bmatrix} i_o \\ i_d^* \\ i_q^* \end{bmatrix} \tag{14}$$

A significant advantages that dq based current reference generator scheme offers is that it facilitates a linear controller implementation in DC voltage control loop. Though, an obvious disadvantage that arises from dq based current reference frame algorithm, deployment for producing reference current generation is of second order harmonic components in i_d and i_q in an unbalanced operating state. Harmonics amplitude is based on the unbalanced load current percentage expressed as the relationship between the positive sequence current i_{L1} and the negative sequence current i_{L2}.

Traditionally PI controller is used to control the DC voltage of the converter. This is an important issue in the evaluation, since the cost function according to the Equation (9) is designed using only reference currents, in order

to avoid the use of weighting factors. In general, these weighting factors are obtained experimentally, and they are not well defined for different operating conditions. In addition to that, the slow dynamic response of the voltage across the electrolytic capacitor will not affect the current transient response. For this reason, the PI controller represents a simple and successful way for the DC voltage control. The DC voltage remains constant (with a minimum value of $\left(\sqrt{6}v_s\left(rms\right)\right)$ until the active power absorbed by the converter decreases to a level of the inability to compensate it's losses.

The absorbed active power by the converter is controlled by adjusting the amplitude of the active power reference signal i_c, which is in phase with each phase voltage. In the block diagram shown in **Figure 6**, the DC voltage v_{dc} is measured and then compared with a constant reference value v_{dc}^*. The error (e) is processed by a PI controller, with two gains, K_p and K_i. **Figure 6** shows that the output of the PI controller is given to the DC voltage transfer function G_s, which is represented by a first order system are briefly explained in [21].

In the conventional tuning of PLL there is a frequency jump in the grid voltage and a delay in theta tracking. Both will be varies with respect to the type of load used. Moreover the varying nature of RES produces ripples in the output which affects the grid voltage [22] [23], which is given to PLL as feedback here. This will affect the injection time of the compensating current into the grid. To avoid these demerits in this paper the conventional method of tuning is replaced by ABC based tuning to enhance the performance of the overall system.

5.1. Modified Three-Phase PLL to Avoid DC Error

For a three phase balanced set of input signals is as shown in the Equation (15)

$$v_{abc}=\left(V\sin\left(\theta\right),V\sin\left(\theta-\frac{2\pi}{3}\right),V\sin\left(\theta+\frac{2\pi}{3}\right)\right)^{\mathrm{T}} \tag{15}$$

and the d component is given as in the Equation (16)

$$V_d=V\sin\left(\theta-\varphi\right) \tag{16}$$

The loop regulates this quantity to zero and, thus, regulates φ to θ. Assume that the input signal has a DC component of $\left(d_a,d_b,d_c\right)^{\mathrm{T}}$; then, a term as shown in Equation (17) will superimpose on v_d. If the DC offset is unbalanced (*i.e.*, has unequal values on three phases), this causes an error whose frequency is the same as

$$\frac{2}{3\left[d_a\cos\varphi+d_b\cos\left(\varphi-\frac{2\pi}{3}\right)+d_c\cos\left(\varphi+\frac{2\pi}{3}\right)\right]} \tag{17}$$

fundamental frequency. The proposed ABC based modified three phase PLL is shown in **Figure 7**. Here the block denoted by "dot" makes the dot product of its inputs: $\langle x,y\rangle=x^{\mathrm{T}}y$ It is to be observed that the output of this block is equal to $\left[\frac{3}{2}V_d\right]$. Thus, the factor 2/3 is placed to make it equal to V_d.

5.2. Objective Function for Tuning PLL Using ABC Algorithm

This section discusses about the tuning of gain values to attain the optimal performance of PLL. K_i value depends on the frequency factor ω, K_p gain value depends on the angle ∅. The voltage magnitude is based on the K_v gain value where as the K_o gain value depends on the DC component. The objective function of this approach would be to minimize the THD and Settling Time 'ST' of the proposed model in **Figure 8** as follows.

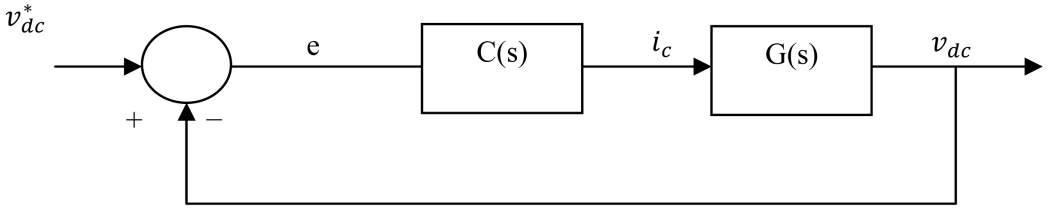


Figure 6. DC voltage control block diagram.

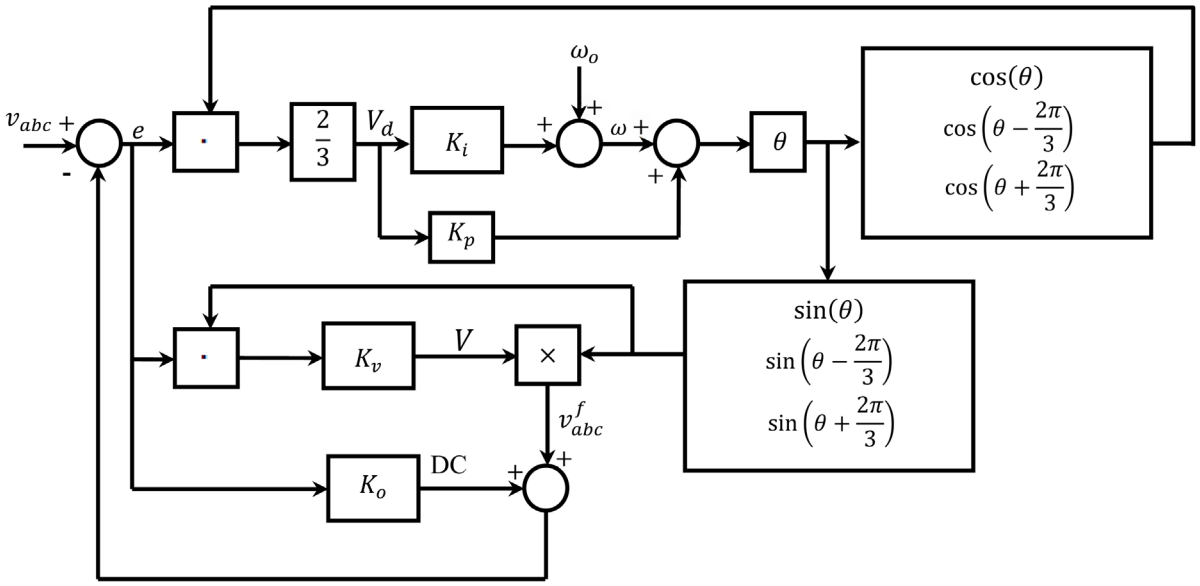


Figure 7. ABC based modified three-phase PLL to avoid DC error.

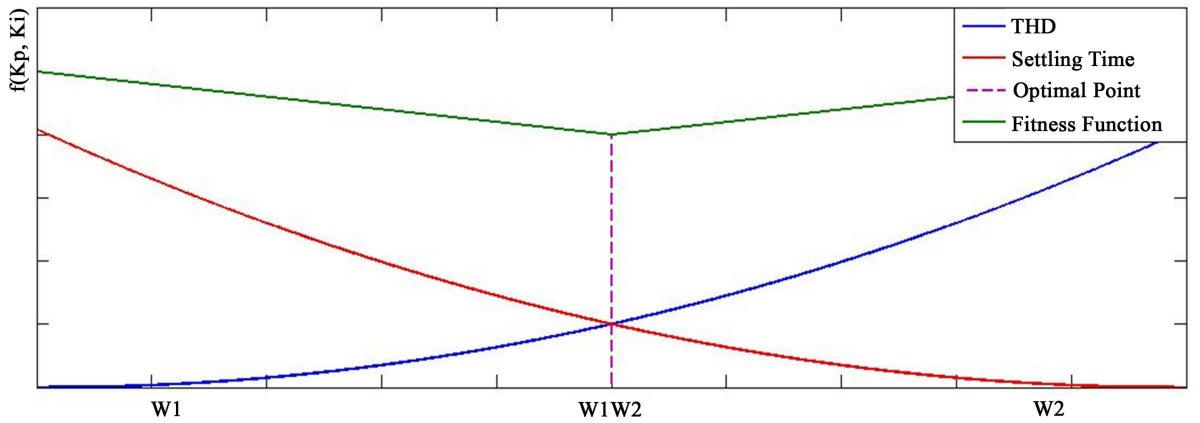


Figure 8. Minimum cost function evaluation.

$$\text{Minimize } f\left(K_p, K_i, K_v \text{ and } K_o\right) = w_1 * THD + w_2 * ST \tag{18}$$

where w_1 and w_2 are the parameters for calibration. The parameters subjected to limit, considered in this research work are

$$\begin{aligned} K_{p_{\min}} &< K_p < K_{p_{\max}} \\ K_{i_{\min}} &< K_i < K_{i_{\max}} \\ K_{v_{\min}} &< K_v < K_{v_{\max}} \\ K_{o_{\min}} &< K_o < K_{o_{\max}} \\ Sat_{\min} &< Sat < Sat_{\max} \end{aligned} \tag{19}$$

Manual tuning of the controller parameters in removing the performance becomes more difficult and consumes more time. To overcome this major drawback, ABC based optimization approach is proposed here to auto tune the controller parameters and also to improve the efficiency of the control strategy in extracting reference currents for SAPF under non linear load conditions also.

5.3. Working of the Proposed ABC based PI Self Tuning

1) Initialize the population (v_{abc}) of solutions
2) Initially, the controller parameter are generated which is of size N
3) Produce new solutions of DC components through employed bees and then apply greedy selection process
4) Probability values are calculated for the above solution
5) Produces new set of population for the parameters of the controller
6) Update the best values achieved so far, and sort the obtained values
7) Based on probability values again the new solutions are obtained through onlooker bees and then apply greedy selection process
8) Determine the left out solution for the scout, if exists, and replace it with a new randomly produced solution
9) Update the best value achieved so far

The proposed structure of **Figure 7** the DC component in the input signal is detected by the branch comprises three integrators with equal gains K_o to estimate the DC components on three phases. Since the DC components are estimated by this branch and added to the output, the signal e will have no DC. Thus the error in the whole loop is eliminated by removing the DC component, which assures the PLL operation no longer suffers from such components. The modified PLL equations are given in Equation (20).

$$\dot{V} = \mu_1 e \sin\varnothing, \quad \dot{\omega} = \mu_2 e \cos\varnothing$$
$$\dot{\varnothing} = \mu_3 e \cos\varnothing + \omega, \quad \dot{d} = \mu_o e \tag{20}$$

where $e = v - d - V\sin\varnothing$.

The variables V, ω and $\varnothing$ estimate voltage magnitude, frequency and angle of the input signal with nominal fundamental frequency of ω_o. Thus it is observed that, besides THD and Settling Time of the DC link voltage TV_{dc} , the work also concentrates on choosing the optimal filter current with a minimum cost function.

6. Simulation Results and Evaluation

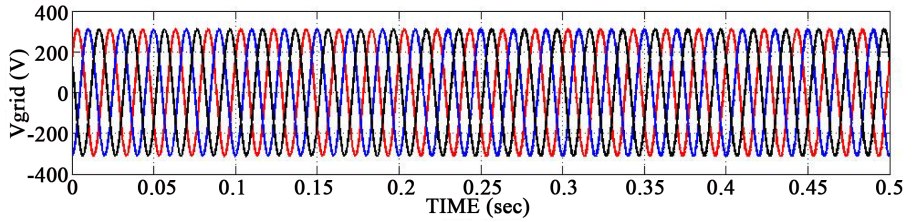
This work has been simulated in MATLAB SIMULINK r2011a. This section clearly discusses about the performance evaluation of the proposed model in which the voltage source converter is controlled to achieve minimized current harmonics under non linear load conditions at unity power factor. Moreover, this proposed model is verified for the RES interconnection with inverter to attain balanced sinusoidal grid currents under unbalanced load conditions through ABC optimization technique. The other simulation scenario wherein the PLL is tuned to eliminate DC component, minimizing the peak overshoot and improving the settling time of frequency and theta is considered. In this simulation, the V_{grid} represents grid voltage, I_{grid} represents grid current, I_{Load} represents the load current, I_{inv} represents the inverter current and V_{dc} represents DC link voltage.

6.1. System Behavior with SAPF for Nonlinear Load under Balanced Condition

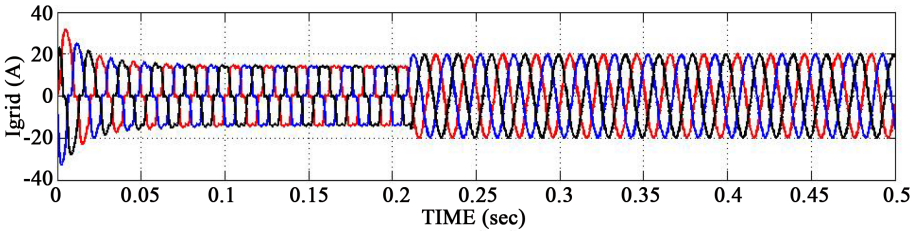
The nonlinear behavior of the three phase grid system with nonlinear balanced load condition and how the compensation is done with the help of the voltage source converter acting as SAPF for the grid connected PV system is clearly depicted in **Figure 9**. **Figure 9(a)** shows the grid voltage profile with the magnitude of 325 V, taken between line to ground for all the three phases. Here for the analysis a three phase diode bridge rectifier feeding resistive load is considered as nonlinear load throughout the simulation discussion. Due to this nonlinear load, the sinusoidal nature of the grid current is affected as shown in **Figure 9(b)** up to 0.22 seconds.

The nonlinear diode bridge rectifier will draw a nonlinear load current as shown in **Figure 9(c)**. The effect of the SAPF on the grid current, load current and the DC link voltage is recognized from 0.22 seconds, since the converter starts to inject the compensating current, acting as SAPF from that moment as shown in **Figure 9(d)**.

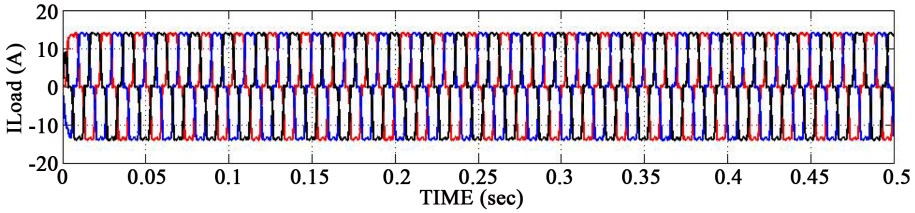
Now the compensating performance of the SAPF could be clearly understood from **Figure 9(e)** and **Figure 9(f)**. For the clarity of understanding the current waveform is shown for phase "A" alone in **Figure 9(e)**. The source current compensation could also be seen in **Figure 9(b)** after 0.22 seconds. The DC link grid voltage has rising nature up to 0.22 seconds and after the injection of compensating current, it is quickly forced to be maintained at 680 V as per the system design and the steady state nature could also be realized from **Figure 9(f)**.



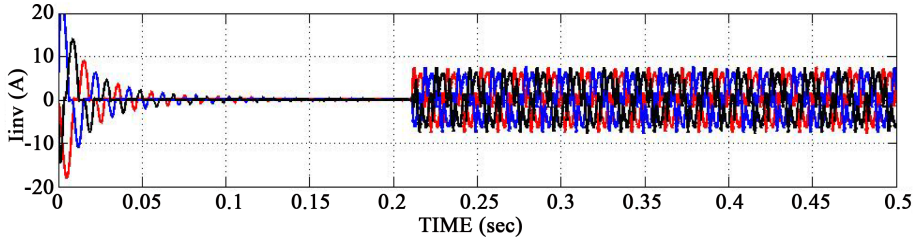
(a)



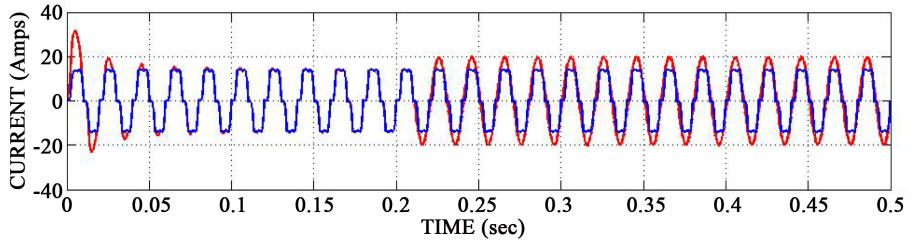
(b)



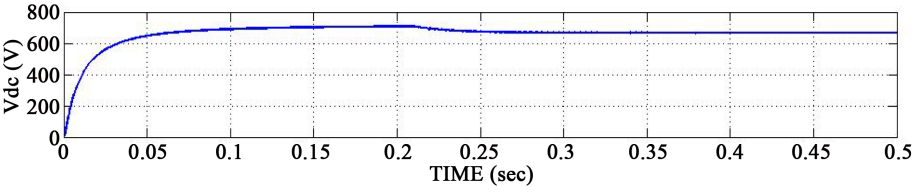
(c)



(d)



(e)



(f)

Figure 9. (a) Grid voltage; (b) Grid current; (c) Nonlinear load current; (d) Inverter current; (e) Load current vs source current; (f) DC link voltage.

6.2. System Behavior with SAPF for Nonlinear Load under Unbalanced Condition

The performance of the ABC tuned SAPF for both nonlinear and unbalanced load conditions could be appreciated by analysing the waveforms shown in **Figure 10**.

Here the unbalanced condition is considered from 0.2 seconds onwards and up to that the system operates the nonlinear load under balanced condition only. Load unbalancing is created at 0.2 seconds, only on two phases *i.e.*, phase A and phase B having 20A as unbalanced load currents. Phase C is kept in balanced nonlinear condition with the current magnitude of 14 A. This is shown in **Figure 10(a)**. **Figure 10(b)** illustrates the compensating current generated by the SAPF which is to be injected into the grid for reducing harmonics and maintaining the balanced condition of the system.

Till 0.2 seconds the system has nonlinearity alone as shown in **Figure 10(a)**. This nonlinear nature of the grid current for balanced condition is compensated by the proposed SAPF model to reduce the harmonic currents. After 0.2 seconds the SAPF is producing the compensating current to compensate the harmonic current as well as to make the system as balanced one.

The performance of the proposed model for the unbalanced nonlinear system is evaluated by investigating the waveform shown in **Figure 10(c)**. Till 0.2 seconds the proposed model injects the compensating current waveform and thus making the grid current as sinusoidal one for the balanced system. The unbalanced system which is created at 0.2 seconds has become as a balanced linear system by drawing the current as 18 A in each phase approximately due to the optimal reference current generator.

6.3. Performance Evaluation of Proposed ABC Tuned and Conventional PLL

The main objective of this paper which is known as ABC tuned PLL with predictive current control method of SAPF is for optimizing the control parameters of the PLL can be evaluated by comparing it with the conventional PLL model, based on the factors frequency response, theta tracking, elimination of DC component and maintain the voltage magnitude of the system. **Figure 11** shows the evidence for the better performance of the proposed PLL model compared to the conventional model.

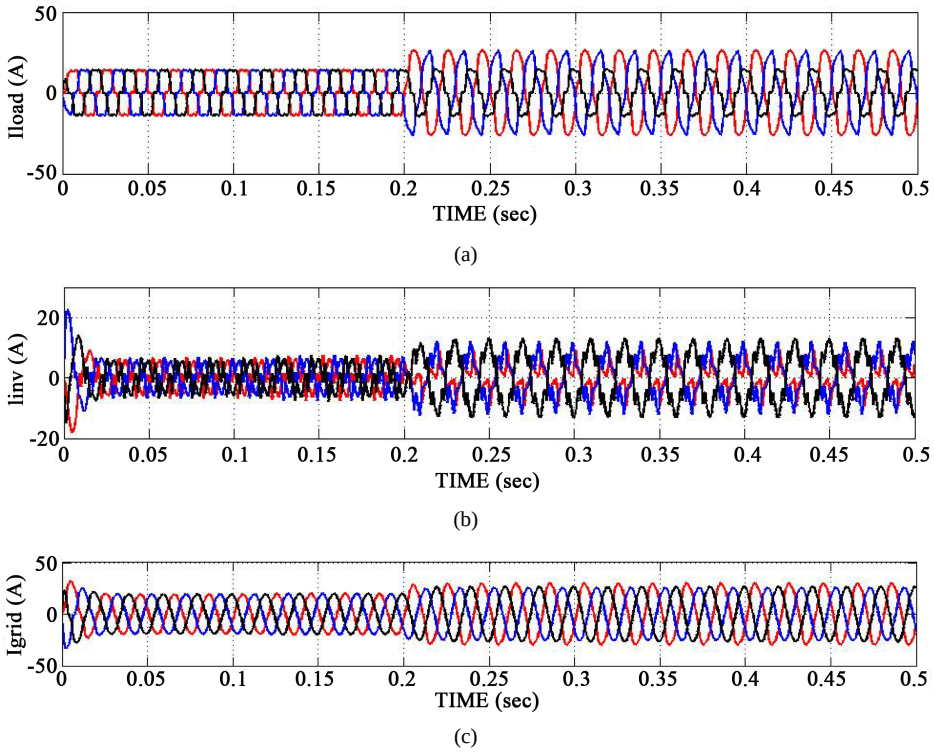


Figure 10. (a) Unbalanced nonlinear load current; (b) Inverter current for unbalanced load; (c). Grid current for unbalanced load.

Figure 11(a) compares the frequency response of the proposed model with the conventional model in tuning the PLL. It is clearly shown that the proposed model results in lesser peak overshoot and quicker settling time of the system frequency at 50 Hz. Moreover it holds good even under unbalanced load conditions. It could also be realized from the same figure at 0.2 seconds, at which the unbalancing is created in the system. Improving the frequency response is taken care by the proper tuning of the PLL parameter K_i.

Figure 11(b) compares the theta tracking response of the proposed model with the conventional model. It is clearly understood that the proposed ABC tuned PLL tracks the theta quickly even from 0.01 seconds where as it is higher for the conventional model of the PLL. The quicker theta tracking influences the generation of reference current, selecting the optimal switching of the converter and thus improving the harmonic compensation. By the proper tuning of K_p gain value, good response in tracking the theta value could be done.

Figure 11(c) shows the voltage DC component response of proposed ABC tuned PLL and the conventional SRF-PLL. The DC component may be naturally present in the input signal or may be generated due to nonlinear/unbalanced load conditions. This DC component creates low frequency oscillations that cannot be removed using conventional filtering techniques as it may degrade the overall performance of the system and thus an efficient PLL structure is essential. Now, in order to attain almost zero DC components, an efficient ABC optimization loop is integrated inside the PLL structure which results in effective elimination of the DC component by tuning the K_o gain value. The optimal voltage magnitude response is attained by tuning the K_v gain value as shown in **Figure 11(d)**.

With optimal tuning of K_v gain value, lesser peak overshoot response is achieved in the proposed model and hence the quick settling and the improved magnitude response of the three phase system voltage with the fundamental frequency is as shown in **Figure 11(e)** in per unit value. Obtaining zero error in the comparison of v_{abc}^{f} and v_{abc} as shown in **Figure 11(f)** increases the overall performance of the PLL and thus improving the performance of the proposed SAPF model for the interconnected PV system to the grid. The power factor of the grid system is nearest to unity as shown in **Figure 11(g)**.

6.4. THD Analysis of the System

Table 2 shows the harmonic analysis of the waveforms for the system without SAPF, with conventional SAPF and with the modified SAPF. It gives the THD value of the harmonic current of the system for the each case in balanced and unbalanced load conditions. It gives the THD comparison for the system under various harmonic orders.

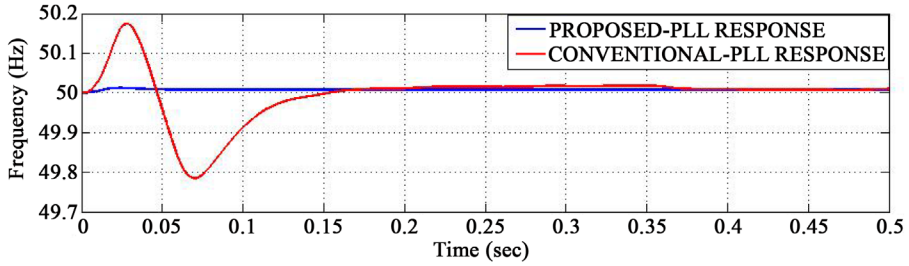
7. Conclusion

The design of ABC based PLL tuned SAPF has been proposed in this paper for a grid connected solar PV system. The dynamic performance of the proposed model in compensating current harmonics and reactive power consumption is evaluated through the Matlab simulation. In this research, ABC optimization is proposed to select the optimal switching states that must be applied to the power converter, by selecting the best minimal optimal

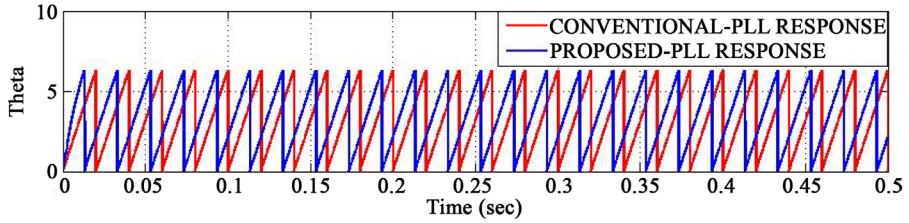
Table 2. Analysis of % THD for the nonlinear load under balanced and unbalanced condition.

Grid current THD in % for nonlinear load at balanced condition								
Method	5th	7th	9th	11th	13th	15th	17th	THD
SRF-PLL based SAPF (Conventional)	0.40	0.66	0.14	0.96	0.40	0.09	0.70	1.85
ABC based PLL tuning of SAPF (Proposed)	0.04	0.01	0.06	0.50	0.04	0.06	0.39	1.20
Grid current THD in % for nonlinear load at Unbalanced condition								
SRF-PLL based SAPF (Conventional)	2.10	1.95	1.69	1.56	0.94	0.81	0.67	4.62
ABC based PLL tuning of SAPF (Proposed)	1.70	1.47	1.41	1.34	0.78	0.81	0.69	3.79

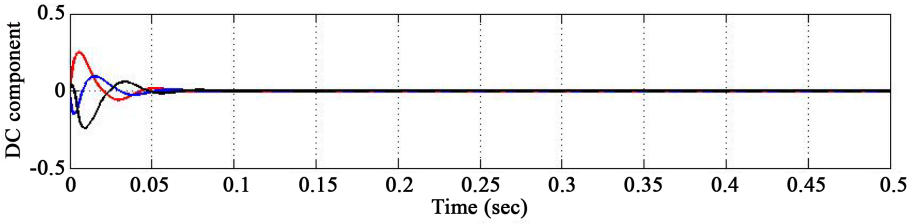
Note : In both cases nonlinear load current (without SAPF) %THD = 25.01


PROPOSED-PLL RESPONSE
CONVENTIONAL-PLL RESPONSE
Frequency (Hz)
Time (sec)

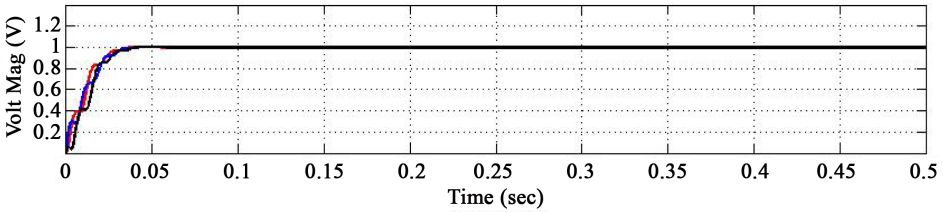
(a)


CONVENTIONAL-PLL RESPONSE
PROPOSED-PLL RESPONSE
Theta
Time (sec)

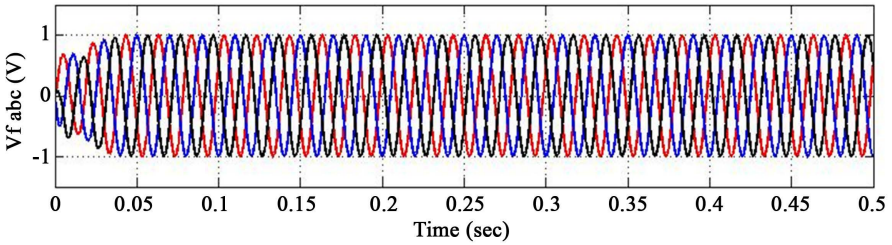
(b)


DC component
Time (sec)

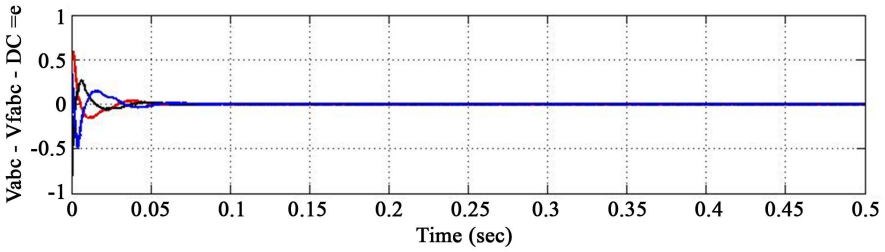
(c)


Volt Mag (V)
Time (sec)

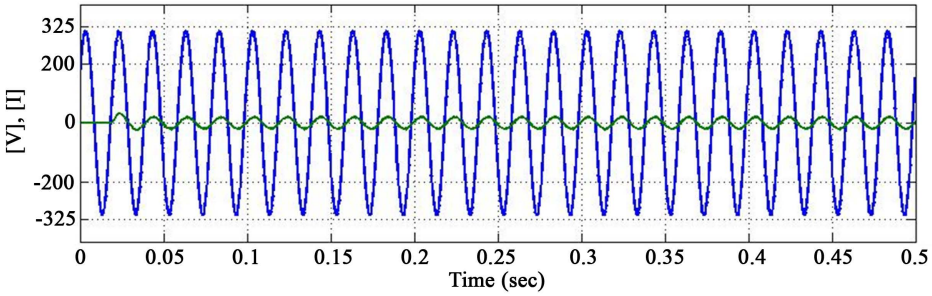
(d)


Vf abc (V)
Time (sec)

(e)


Vabc - Vfabc - DC =e
Time (sec)

(f)



(g)

Figure 11. (a) Frequency response; (b) Theta response; (c) DC component; (d) Voltage magnitude; (e) Grid voltage (pu); (f) Dc error; (g) Phase sequence of the grid voltage and grid current.

value "g". Simulated results have proved that the proposed predictive control algorithm is a good choice to classical linear control methods and the compensation effectiveness of the proposed shunt active power filter with ABC based PLL tuning. The performance of the proposed approach has been evaluated under unbalanced load conditions and it is observed that the proposed modified PLL approach attains fast theta tracking as 0.15 seconds, quick settlement of frequency compared with ±0.2 Hz jumping of conventional model, maintaining of the DC voltage magnitude in 700 V within 0.4 seconds, zero error for the presence of DC component, improved settling time and minimal attainment of THD as 1.2% for balanced load and 3.79% for unbalanced load. In the future the work can be extended to improve the voltage quality of the system and the converter operation can be analyzed as a simple inverter for injecting the power derived from solar PV and as SAPF for current harmonic compensation. Instead of VSI, multilevel inverters may be used for harmonic reduction.

References

[1] Fuchs, E.F., Roesler, D.J. and Kovacs, K.P. (1987) Sensitivity of Electrical Appliances to Harmonics and Fractional Harmonics of the Power System's Voltage. Part II: Television Sets, Induction Watt-Hour Meters and Universal Machines. *IEEE Transaction on Power Delivery*, **2**, 445-453.

[2] Pinto, J.G., Neves, P., Gonçalves, D. and Afonso, J.L. (2009) Field Results on Developed Three Phase Four Wire Shunt Active Power Filters. 35*th Annual Conference of IEEE Industrial Electronics*, Porto, 3-5 November 2009, 480-485.

[3] Salam, Z., Cheng, T.P. and Jusoh, A. (2006) Harmonics Mitigation Using Active Power Filter: A Technological Review. *ELEKTRIKA*, **8**, 17-26.

[4] Mahapatra, K.K., Ghosh, A. and Doradla, S.R. (1998) Simplified Model for Control Design of STATCOM Using Three Level Inverter. *IEEE Region* 10 *International Conference on Global Connectivity in Energy, Computer, Communication and Control*, Vol. 2, 536-539.

[5] Rahmani, S., Mendalek, N. and AlHaddad, K. (2010) Experimental Design of a Nonlinear Control Technique for Three Phase Shunt Active Power Filter. *IEEE Transaction on Industrial Electronics*, **57**, 3364-3375.

[6] Akagi, H. (1996) New Trends in Active Filter for Power Conditioning. *IEEE Transaction on Industrial Applications*, **32**, 1312-1322.

[7] Rocabert, J., Luna, A., Blaabjerg, F. and Rodríguez, P. (2012) Control of Power Converters in AC Microgrids. *IEEE Transaction on Power Electronics*, **27**, 4734-4749.

[8] Montero, M.I.M., Cadaval, E.R. and Gonzalez, F.B. (2007) Comparison of Control Strategies for Shunt Active Power Filters in Three-Phase Four Wire Systems. *IEEE Transaction on Power Electronics*, **22**, 229-236.

[9] Nam, S.-R., Park, J.-Y., Kang, S.-H. and Kezunovic, M. (2009) Phasor Estimation in the Presence of DC Offset and CT Saturation. *IEEE Transaction on Power Delivery*, **24**, 1842-1849.

[10] Ciobotaru, M., Teodorescu, R. and Agelidis, V.G. (2008) Offset Rejection for PLL Based Synchronization in Grid Connected Converters. 23*rd Annual IEEE Applications of Power Electronics Conference and Exposition*, Austin, 24-28 February 2008 1611-1617.

[11] Stringer, N.T. (1998) The Effect of DC Offset on Current Operated Relays. *IEEE Transactions on Industrial Applications*, **34**, 30-34.

[12] Ghartemani, M.K., Khajehoddin, S.A., Jain, P.K., Bakhshai, A. and Mojiri, M. (2012) Addressing DC Component in

PLL and Notch Filter Algorithms. *IEEE Transactions on Power Electronics*, **27**, 78-86.

[13] Basilio, J.C. and Matos, S.R. (2002) Design of PI and PID Controllers with Transient Performance Specification. *IEEE Transactions on Education*, **45**, 364-370.

[14] Abdennour, A. and Alturki, F.A. (2008) A Comparative Study of PI/PID Classical and Intelligent Tuning Methods. *Journal of Engineering and Computer Sciences*, **1**, 29-42.

[15] Cheng, M., Sun, Q. and Zhou, E. (2006) New Self Tuning Fuzzy PI Control of a Novel Doubly Salient Permanent Magnet Motor Drive. *IEEE Transaction on Industrial Electronics*, **53**, 814-821.

[16] Khorramabadi, S.S. and Bakhshai, A. (2014) Critic Based Self Tuning PI Structure for Active and Reactive Power Control of VSCs in Microgrid System. *IEEE Transaction on Smart Grid*, **6**, 92-103. http://dx.doi.org/10.1109/TSG.2014.2354651

[17] De Araujo Ribeiro, R.L., de Azevedo, C.C. and de Sousa, R.M. (2012) A Robust Adaptive Control Strategy of Active Power Filters for Power Factor Correction, Harmonic Compensation and Balancing of Nonlinear Loads. *IEEE Transaction on Power Electronics*, **27**, 718-730. http://dx.doi.org/10.1109/TPEL.2011.2161334

[18] Rodriguez, J., Pontt, J., Silva, C.A., Correa, P., Lezana, P., Cortés, P. and Ammann, U. (2007) Predictive Current Control of a Voltage Source Inverter. *IEEE Transactions on Industrial Electronics*, **54**, 495-503. http://dx.doi.org/10.1109/TIE.2006.888802

[19] Karaboga, D. and Ozturk, C. (2011) A Novel Clustering Approach: Artificial Bee Colony (ABC) Algorithm. *Applied Soft Computing*, **11**, 652-657. http://dx.doi.org/10.1016/j.asoc.2009.12.025

[20] Chung, S.-K. (2000) A Phase Tracking System for Three Phase Utility Interface Inverters. *IEEE Transaction on Power Electronics*, **15**, 431-438. http://dx.doi.org/10.1109/63.844502

[21] Acuna, P., Moran, L., Rivera, M., Dixon, J. and Rodriguez, J. (2014) Improved Active Power Filter Performance for Renewable Power Generation Systems. *IEEE Transactions on Power Electronics*, **29**, 687-694. http://dx.doi.org/10.1109/TPEL.2013.2257854

[22] Reddy, N.J., Kaliamoorthy, M. and Ashok, K.D. (2008) Control of Grid Connected PV Cell Distributed Generation Systems. *TENCON* 2008—2008 *IEEE Region* 10 *Conference*, Hyderabad, 19-21 November 2008, 1-6. http://dx.doi.org/10.1109/TENCON.2008.4766748

[23] Mylsamy, K., Vairamani, R., Irudayaraj, G.C.R. and Lawrence, H.T.R. (2014) Experimental Validation of a Cascaded Single Phase H-Bridge Inverter with a Simplified Switching Algorithm. *Journal of Power Electronics*, **14**, 507-518. http://dx.doi.org/10.6113/JPE.2014.14.3.507