Circuits and Systems, 2015, 6, 179-187
Published Online August 2015 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2015.68019

A 0.5-V, 1.2-GS/s, 6-Bit Flash ADC Using Temporarily-Boosted Comparator

Kenichi Ohhata, Masataro Iwamoto, Naoto Yamaguchi

Department of Electrical and Electronics Engineering, Kagoshima University, Kagoshima, Japan
Email: k-ohhata@eee.kagoshima-u.ac.jp

Received 25 July 2015; accepted 16 August 2015; published 20 August 2015

Abstract

A low-voltage, high-speed flash ADC is designed. The bottleneck of the operation speed in the low-voltage region is the delay time increase of the comparator. The temporarily boosted comparator is proposed to address this problem. The proposed circuit only boosts the supply voltage in the comparison phase, and therefore, can reduce the delay time while keeping the power overhead to a minimum. Moreover, the body bias control calibration is combined with the temporarily boosted technique. This helps to create a low-power and high-precision comparator. A 0.5-V, 6-bit flash ADC was designed by using 65-nm CMOS technology to demonstrate the effectiveness of the proposed technique. The simulation results showed a high sampling frequency of 1.2 GHz, a low power consumption of 1.4 mW, and an FOM of 28 fJ/conv.-step even at a low supply voltage of 0.5 V.

Keywords

ADC, Low Voltage, Flash, Comparator, Calibration

1. Introduction

Power reduction in a medium resolution and high-speed analog-to-digital convertor (ADC) is strongly required for front end of wireless systems and read channels of disk systems. The power consumption of a CMOS circuit is proportional to the square of the supply voltage; therefore, reducing the supply voltage is the most effective method for reducing the power consumption. However, supply voltage reduction and high-speed operations are incompatible because the delay time is significantly increased when the supply voltage is simply reduced. Thus, it is important to select a suitable circuit architecture that can run at a low supply voltage. Successive approximation registers (SAR) and flash ADCs are mainly used for medium resolution and high-speed applications. A SAR ADC uses a low amount of power and covers only a small area; however, a comparator should be used the

How to cite this paper: Ohhata, K., Iwamoto, M. and Yamaguchi, N. (2015) A 0.5-V, 1.2-GS/s, 6-Bit Flash ADC Using Temporarily-Boosted Comparator. *Circuits and Systems*, **6**, 179-187. http://dx.doi.org/10.4236/cs.2015.68019

same number of times as there are bits [1]-[3]. For example, an operation speed of more than 6 GHz is required for the comparator in a 6-bit, 1-GHz SAR ADC. Therefore, the SAR ADC is unsuitable for use in low voltage operations because the operation speed of the comparator is degraded due to the low supply voltage. On the other hand, a flash ADC is tolerant of the speed degradation in the comparator because the comparator is used only once for the conversion [4]-[6]. Therefore, several previous works on low-voltage and high-speed flash ADCs have been conducted [7] [8]. These ADCs run on a 0.5-V supply voltage; however, the sampling frequencies are 600 MHz and 420 MHz, which are insufficient values for the above-mentioned applications. The sampling frequency of a flash ADC running on a 0.5-V supply voltage is limited by the comparator delay; therefore, reducing the comparator delay is essential for enhancing the sampling frequency.

We discuss the speed limiting factors of the conventional comparators running on a 0.5-V supply voltage in Section 2. We then propose our temporarily boosted comparator for reducing the delay time while maintaining a low power consumption in Section 3. Finally, we show the simulation results of a designed flash ADC by using the proposed comparator.

2. Problem with Conventional Low Voltage Comparators

A conventional comparator running on a 0.5-V supply voltage is shown in **Figure 1** [7]. This type of comparator is referred to as a double-tail analog latch (DTAL). This circuit is composed of two stages. The first stage is a dynamic amplifier and the second one is an analog latch. During the reset phase (CK = 0), the outputs of the dynamic amplifier (AOP and AON) are precharged to the V_{DD} and the outputs of the analog latch (OUTP and OUTN) are reset to GND. The voltages of the AOP and AON drop to GND when the CK rises to the V_{DD} and the phase shifts to the comparison phase. The falling rates of the AOP and AON depend on the input voltages, so the voltage difference between them is generated according to the difference in input voltage. The voltage difference between the AOP and AON is latched by the second stage, and thus, the digital signals (OUTP and OUTN) are output. The forward body bias technique is used to enhance the speed performance. The body voltage is 0.5-V forward biased to reduce the threshold voltage. This enables the delay time of the comparator to be reduced even when the supply voltage is 0.5 V. Special consideration is required for the offset calibration in the low supply voltage region. The MOS varactor is widely used to compensate for the offset voltage of the dynamic comparator [9]. However, the offset compensation range decreases as the supply voltage is reduced because the change in capacitance of the MOS varactor is reduced in the low supply voltage region. Therefore, an offset cancellation technique using a variable delayer was adopted in the previous work shown in **Figure 1**. The activation timing of the dynamic amplifier is controlled by the variable delayer for the offset calibration. For example,

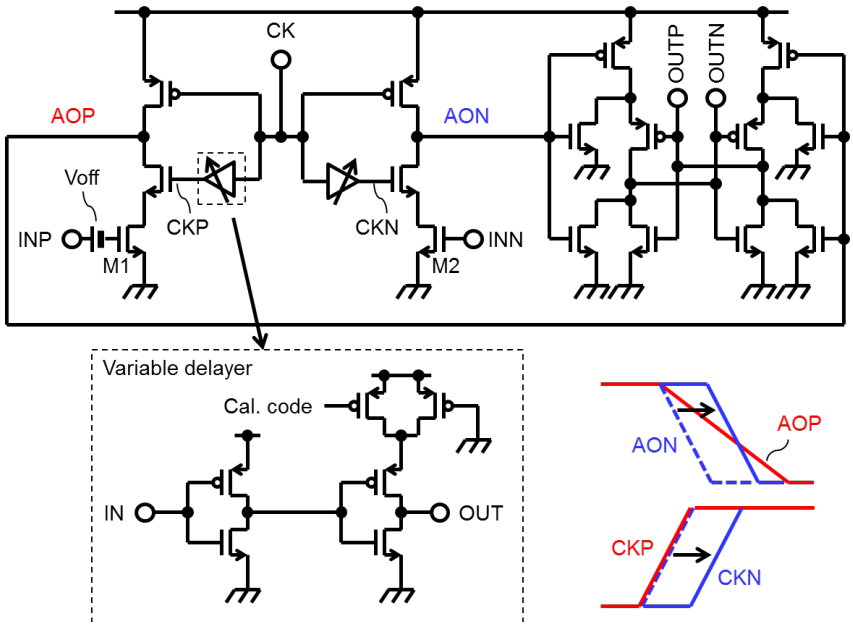

Figure 1. Conventional comparator using variable delay calibration.

let the threshold voltage of M1 be higher than M2. The falling rate of the AOP is slower than that of the AON when the input voltages are equal because the drain current of M1 is less than that of M2. The delay time of the delayer of CKN is increased to compensate for the delay difference between the AOP and AON. The offset voltage can be completely compensated for by properly adjusting the delay time. However, the minimum delay time of the delayer is significantly large because the delayer is composed of a two-stage inverter; therefore, the delay time of the comparator is large. Moreover, the noise voltage of the comparator is also relatively large because the jitter of the delayer is large.

Another conventional comparator, which is shown in **Figure 2**, overcomes the above mentioned problems [8]. A varactor comprised of metal oxide metal (MOM) capacitors and MOS switches are used to compensate for the offset voltage. The capacitance can be changed by connecting and disconnecting the MOM capacitor using the MOS switch. This method can provide a sufficient change in capacitance to compensate for any offset voltage. This comparator can achieve a smaller delay time and noise voltage compared with the comparator shown in **Figure 1**. However, the delay time is still too large for use in a GHz sampling flash ADC.

The simulated V_{DD} dependences of the delay time and power consumption of the conventional comparator using the MOM capacitor and MOS switch are shown in **Figure 3**. The simulation is performed by using 65-nm CMOS technology. The t_{pd_amp} and t_{pd} represent the delay time of the dynamic amplifier and that of the entire comparator, respectively. The t_{pd_amp} is defined as the time between a 50% CK rising edge and a 50% AOP or AON falling edge. The t_{pd} is defined as the time between a 50% CK rising edge and a 90% difference in the OUTP and OUTN. The power consumption can be successfully reduced as the V_{DD} is decreased. The power consumption at V_{DD} = 0.5 V is decreased to approximately 1/4 that at a V_{DD} = 1 V. The t_{pd_amp} is almost constant even when the V_{DD} is decreased, because the operating current of the dynamic amplifier is not determined by the V_{DD} but by the common level of the input signals. On the other hand, the t_{pd} rapidly increases when the V_{DD} is decreased because the delay time of the latch circuit strongly depends on it.

3. Temporarily Boosted Comparator

The supply boosted comparator (SBC) was reported to reduce the delay time under low supply voltage condition [10]-[12]. It attained high-speed operation by boosting the supply voltage locally. However, the current biased comparator was used in the SBC; therefore, the large boost capacitor was required. We apply the boosting technique to the dynamic comparator shown in **Figure 4**; thereby, sufficient boosted voltage can be obtained by the small boost capacitor. The proposed comparator is based on a stacked analog latch (STAL) to reduce the power consumption.

The delay time of the STAL is approximately the same as that of the DTAL; therefore, a temporarily boosted technique is combined with the STAL (TB-STAL) to reduce the delay time. A boost circuit is connected to the V_{DD} terminal of an analog latch and reset pMOSs are connected to the normal V_{DD}. The boosted V_{DD} (V_{DDB}) can be supplied to only the analog latch and only in the comparison phase. This enables for the reduction of the delay time while keeping the power overhead to a minimum. The operating waveforms of the proposed comparator at the supply voltage of 0.5 V are shown in **Figure 5**. In the reset phase (CK = 0), the V_{DDB} is equal to the normal

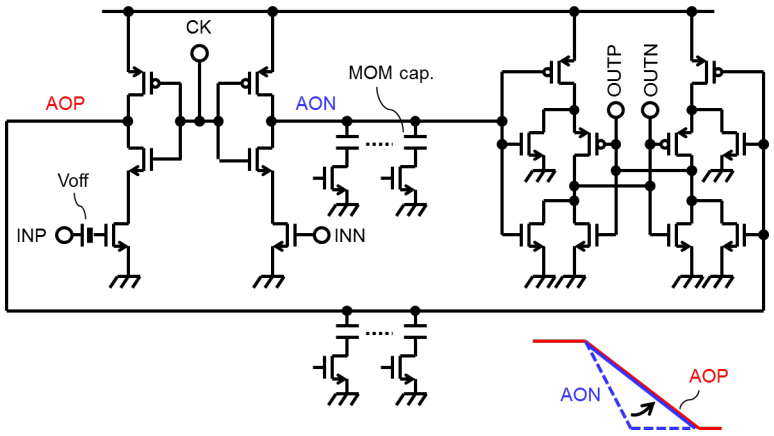

Figure 2. Conventional comparator using MOM capacitor calibration.

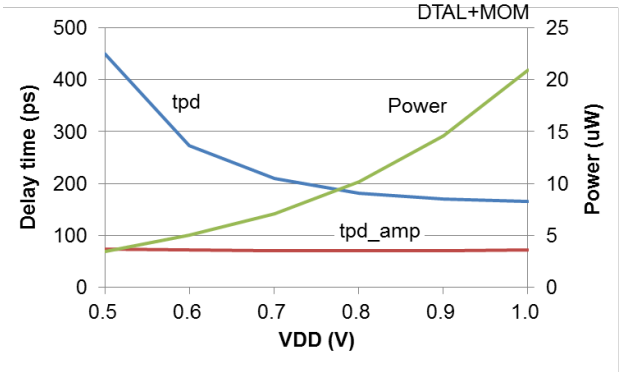

Figure 3. Simulated V_{DD} dependence of delay time and power consumption of conventional comparator.

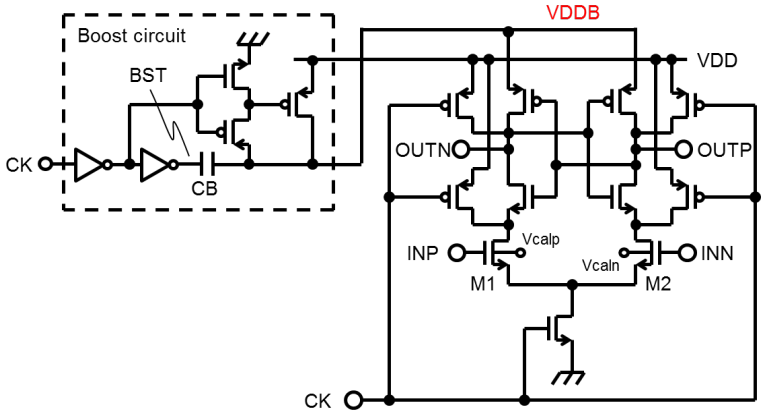

Figure 4. Temporarily boosted comparator.

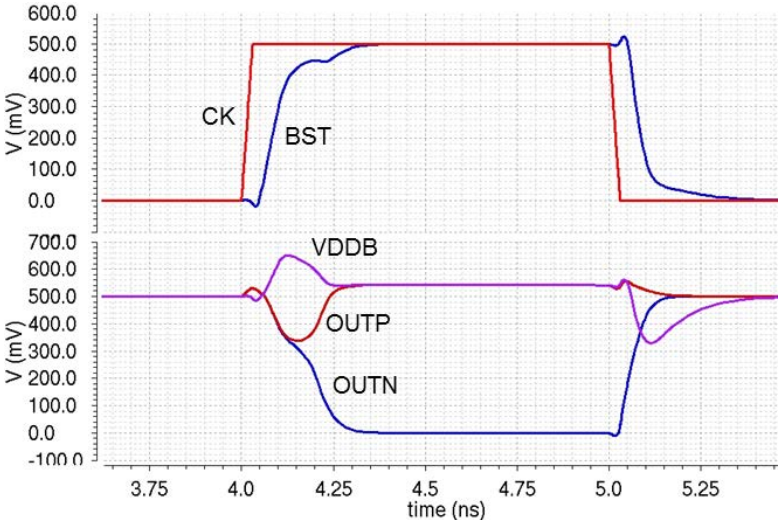

Figure 5. Operation waveforms of temporarily boosted comparator.

V_{DD}. Then, when the CK rises, the boost control signal (BST) rises, and thus, the V_{DDB} is boosted by the boost capacitor (CB). The peak voltage of the V_{DDB} is approximately 0.65 V. This accelerates the transition of the OUTP and OUTN. The stored charge in the CB is consumed to charge the parasitic capacitance of the OUTP and OUTN; therefore, the V_{DDB} returns to the normal V_{DD}. The capacitance of the CB should be designed so that

the high level of the OUTP and OUTN is nearly equal to the normal V_{DD}.

Body bias control calibration [13] is used to compensate for the offset voltage. In this technique, no additional circuitry is added to the dynamic amplifier; the control voltages (V_{calp} and V_{caln}) are connected to the body of the differential MOS transistors (M1 and M2). This method does not introduce any additional capacitive loading in the analog signal path; therefore, there is negligible speed overhead.

The supply voltage dependences of the delay time and the power consumption are shown in **Figure 6**. The power consumption is less than that of the conventional comparator (**Figure 3**). The delay time is maintained almost constant even when the supply voltage is decreased owing to the temporarily boosted technique. The delay time at the supply voltage of 0.5 V is 205 ps. A performance comparison between the conventional and proposed comparators is summarized in **Table 1**. The combination of a simple STAL and the body bias control calibration is also shown for comparison with the TB-STAL. The TB-STAL can successfully reduce the delay time. The delay time of the TB-STAL is less than half that discussed in Ref. [8] and its power consumption is less than that presented in Ref [8]. The offset voltage after the calibration and the noise voltage of the TB-STAL are also sufficiently small for use in a 6-bit flash ADC.

4. Design of 6-Bit Flash ADC Using Proposed Comparator

A 0.5-V, 6-bit flash ADC was designed using 65-nm CMOS technology to demonstrate the effectiveness of the proposed technique. A block diagram of the 6-bit flash ADC is shown in **Figure 7**. The analog inputs (INP and INN) are compared with the reference voltages generated by the reference ladder. The temporarily boosted

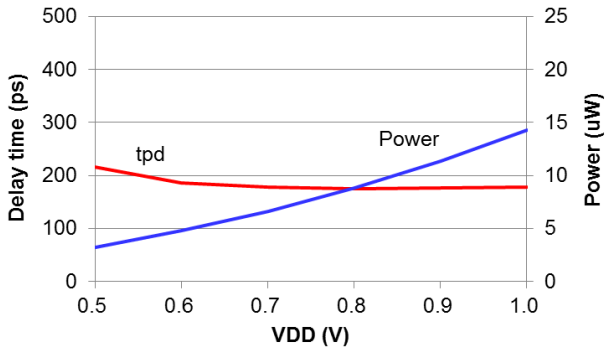

Figure 6. Simulated V_{DD} dependences of delay time and power consumption.

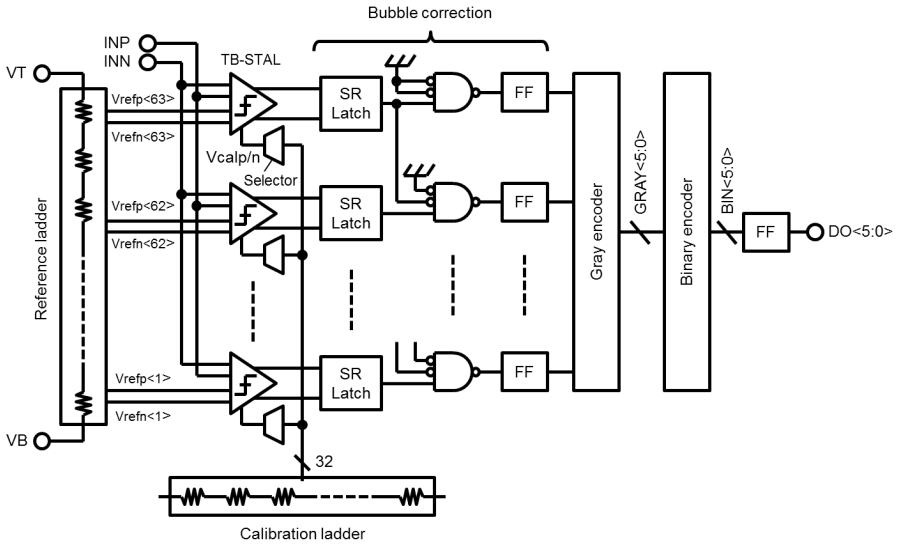

Figure 7. Block diagram of designed 6-bit flash ADC.

Table 1. Performance comparison between conventional and proposed comparators.

	DTAL + Delay cal. Ref. [7]	DTAL + MOM var. Ref. [8]	STAL + BB cal.	TB-STAL + BB cal. Proposed	Note
Delay time [ps]	478	450	362	205	Vin = 1 mV
Power [uW]	5.41	3.45	1.51	3.25	Vin = 1 mV
Offset before cal. [mV(rms)]	15.5	12.8	13.2	12.9	
Offset after cal. [mV(rms)]	1.50	0.93	1.02	0.96	
Noise [mV(rms)]	1.23	0.87	0.95	0.76	

stacked analog latch is used as a comparator. The output of the comparator is latched to a set-reset latch (SR Latch) and the bubble correction is performed using a 3-input NAND circuit. Then, the binary code is generated through the gray and binary encoders. The body voltage (V_{calp} and V_{caln}) for the offset calibration is generated by the calibration ladder and is selected by a selector. The gray and binary encoders are assigned as a pipeline stage; therefore, the total delay time of these circuits should be less than a cycle time. The forward body bias technique is applied to all the logic gates of the encoders to reduce the delay time. Moreover, a parallel binary encoder is used instead of a serial binary encoder. The serial and parallel binary encoders are shown in **Figure 8**. The serial binary encoder transforms a gray code into a binary code one by one. This configuration requires only five EXOR gates; however, a critical path has five stages. On the other hand, the parallel binary encoder has seven EXOR gates; however, the critical path has only three stages. The delay time can be reduced by approximately 30% using the parallel binary encoder.

The ADC output codes before and after the calibration are shown in **Figure 9**. The sampling and input frequencies are 1200 and 9.4 MHz and the supply voltage is 0.5 V. A Monte Carlo simulation including transient noise is performed, that is, the device mismatch and the noise are considered in the simulation results. A large error occurs due to the offsets in the comparators before the calibration, resulting in a poor signal to noise and distortion ratio (SNDR) of 17.9 dB. The body bias control calibration successfully improves the SNDR to 35.9 dB. The sampling frequency dependencies of the SNDR and spurious free dynamic range (SFDR) are shown in **Figure 10**. The input frequency is set to half the sampling frequency. The dashed lines show the simulation results under standard conditions and the solid lines show the simulation results after the calibration, including the device mismatch and the noise. The SNDR is almost constant up to 1.2 GHz and begins to degrade at more than 1.3 GHz. The SNDR and SFDR at the sampling frequency of 1.2 GHz are 34.0 and 39.4 dB. The input frequency dependencies of the SNDR and SFDR are shown in **Figure 11**. The sampling frequency is 1.2 GHz. The SNDR is almost constant even when exceeding the Nyquist frequency. The effective bandwidth is approximately 800 MHz. The power consumption breakdown at the sampling frequency of 1.2 GHz is shown in **Figure 12**. The total power consumption is 1.4 mW and approximately 50% is consumed in the comparators. A performance comparison with the current state-of-the-art technology is summarized in **Table 2**. The sampling frequency and the figure of merit (FOM) are greatly improved compared with that in the previous works at a supply voltage of 0.5 V [7] [8]. The FOM is only 28 fJ/conv.-step, which is less than that of the SAR ADC when using 32-nm technology [14].

5. Conclusion

A low-voltage, high-speed flash ADC is designed. The most effective method for reducing the power dissipation of an ADC is the reduction of the supply voltage; however, simply reducing the supply voltage causes operating speed degradation. The bottleneck of the operation speed in a low-voltage region is the delay time increase of the comparator. The temporarily boosted comparator is proposed to address this problem. The proposed circuit only boosts the supply voltage in the comparison phase; therefore, it can reduce the delay time while keeping the power overhead to a minimum. Moreover, the body bias control calibration is combined with the temporarily boosted technique, which helps to create a low-power and high-precision comparator. A 0.5-V, 6-bit flash ADC was designed by using 65-nm CMOS technology to demonstrate the effectiveness of the proposed technique. The simulation results showed a high sampling frequency of 1.2 GHz, a low power consumption of 1.4 mW, and

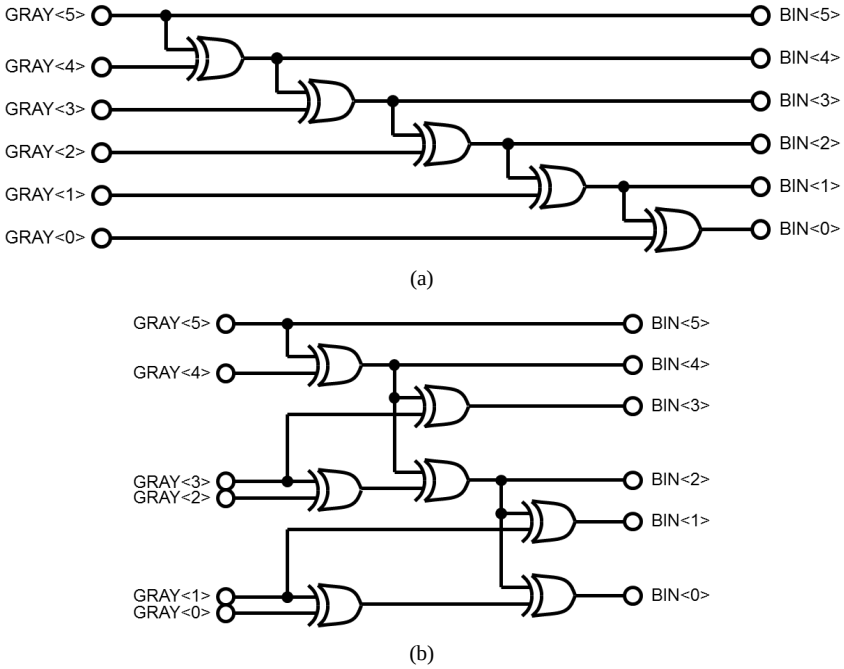

Figure 8. Binary decoder. (a) Serial binary decoder; (b) Parallel binary decoder.

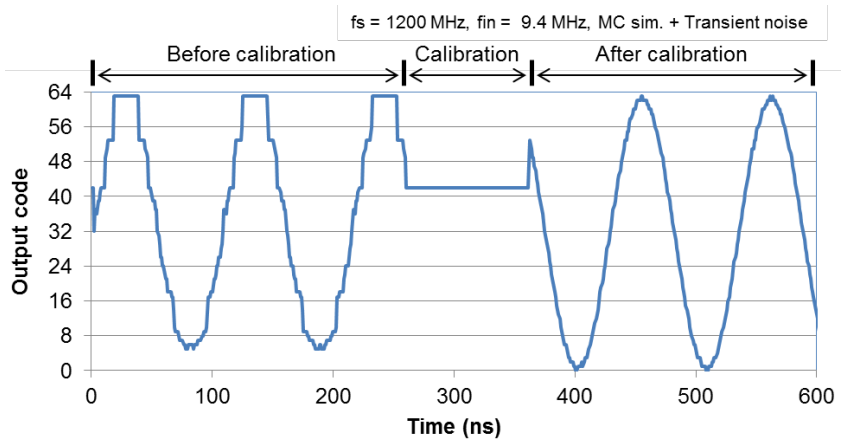

Figure 9. ADC output codes before and after calibration.

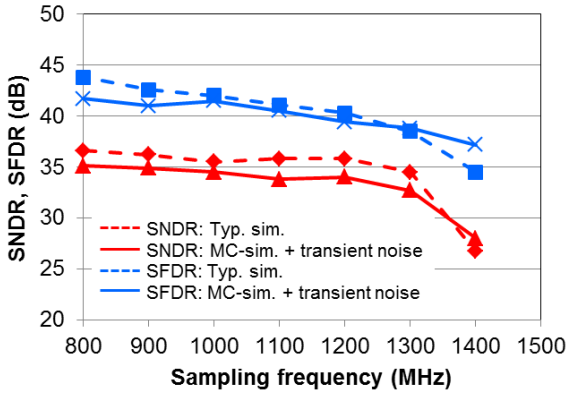

Figure 10. Simulated sampling frequency dependences of SNDR and SFDR.

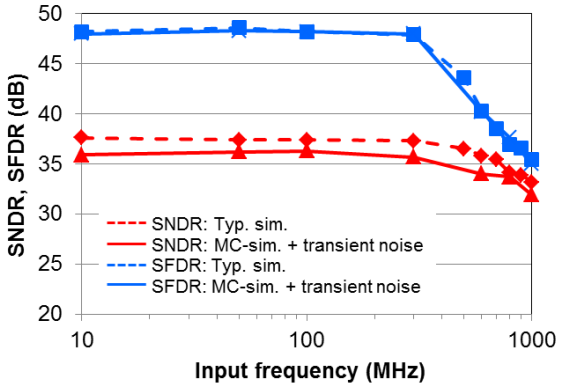

Figure 11. Simulated input frequency dependences of SNDR and SFDR.

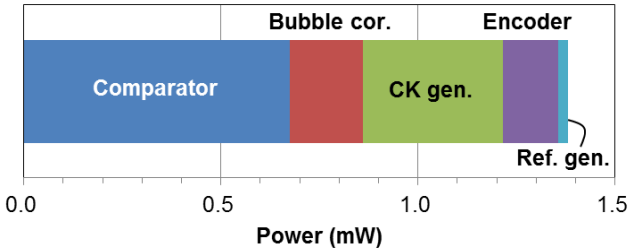

Figure 12. Breakdown of power consumption.

Table 2. ADC performance comparison.

	Ref. [14]	Ref. [7]	Ref. [8]	This work (MC + tran. noise sim.)
Technology (nm)	32	90	90	65
Architecture	SAR	Flash	Flash	Flash
Resolution	8	5	7	6
Supply voltage (V)	1.0	0.5	0.5	0.5
Sampling freq. (MHz)	1200	600	420	1200
SNDR (dB)	39.3	27	35	34
Power (mW)	3.1	1.2	4.1	1.4
FOM (fJ/c.-s.)	34	160	906	28

an FOM of 28 fJ/conv.-step even at a low supply voltage of 0.5 V.

Acknowledgements

This work was supported by the VLSI Design and Education Center (VDEC) and The University of Tokyo in collaboration with Cadence Design Systems, Inc.

References

[1] Alpman, E., Lakdawala, H., Carley, L.R. and Soumyanath, K. (2009) A 1.1 V 50 mW 2.5 GS/s 7 b Time-Interleaved C-2C SAR ADC in 45 nm LP Digital CMOS. *IEEE International Solid-State Circuits Conference Digest Technical Papers*, San Francisco, 8-12 Feburary 2009, 76-77.

[2] Yang, J., Naing, T.L. and Brodersen, B. (2009) A 1-GS/s 6-Bit 6.7-mW ADC in 65-nm CMOS. *IEEE Custom Integrated Circuits Conference*, San Jose, 13-16 September 2009, 287-290.

[3] Tai, H.-Y., Tsai, P.-Y., Tsai, C.-H. and Chen, H.-S. (2013) A 0.004 mm^2 Single-Channel 6-Bit 1.25 GS/s SAR ADC in

40 nm CMOS. *IEEE Asian Solid-State Circuits Conference*, Singapore, 11-13 November 2013, 277-280.

[4] Jiang, X.C., Wang, Z.Y. and Chang, M.F. (2003) A 2 GS/s 6 b ADC in 0.18 µm CMOS. *IEEE International Solid-State Circuits Conference Digest Technical Papers*, San Francisco, 9-13 February 2003, 322-323.

[5] Shu, Y.-S. (2012) A 6 b 3 GS/s 11 mW Fully Dynamic Flash ADC in 40 nm CMOS with Reduced Number of Comparators. *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, 13-15 June 2012, 26-27.

[6] Chen V.H.-C. and Pileggi, L. (2013) An 8.5 mW 5 GS/s 6 b Flash ADC with Dynamic Offset Calibration in 32 nm CMOS SOI. *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, Kyoto, 12-14 June 2013, C264-C265.

[7] Miyahara, M., Lin, J., Yoshihara, K. and Matsuzawa, A. (2010) A 0.5 V, 1.2 mW, 160 fJ, 600 MS/s 5 Bit Flash ADC. *IEEE Asian Solid-State Circuits Conference*, Beijing, 8-10 November 2010, 1-4.

[8] Lin, J., Mano, I., Miyahara, M. and Matsuzawa, A. (2012) A 0.5 V, 420 MSps, 7-Bit Flash ADC Using All-Digital Time-Domain Delay Interpolation. *IEEE International Conference on Electron Devices and Solid State Circuit*, Bangkok, 3-5 December 2012, 1-2.

[9] Plas, G.-V., Decoutere, S. and Donnay, S. (2006) A 0.16 pJ/Conversion-Step 2.5 mW 1.25 GS/s 4 b ADC in a 90 nm Digital CMOS Process. *IEEE International Solid-State Circuits Conference Digest Technical Papers*, San Francisco, 6-9 February 2006.

[10] Mesgarani, A., Nelson, F.Z., Alam, M.N. and Ay, S.U. (2010) Supply Boosting Technique for Designing Very Low-Voltage Mixed-Signal Circuits in Standard CMOS. 53*rd IEEE International Midwest Symposium on Circuits and Systems* (*MWSCAS*), Seattle, 1-4 August 2010, 893-896. http://dx.doi.org/10.1109/mwscas.2010.5548658

[11] Ay, S.U. (2011) A Sub-1Volt 10-bit Supply Boosted SAR ADC Design in Standard CMOS. *An International Journal of Analog Integrated Circuits and Signal Processing*, **66**, 213-221. http://dx.doi.org/10.1007/s10470-010-9515-3

[12] Ay, S.U. (2011) Energy Efficient Supply Boosted Comparator Design. *Journal of Low Power Electronics and Applications*, **1**, 247-260. http://dx.doi.org/10.3390/jlpea1020247

[13] Kim, J.-I., Sung, B.-R.-S., Kim, W. and Ryu, S.-T. (2013) A 6-b 4.1-GS/s Flash ADC With Time-Domain Latch Interpolation in 90-nm CMOS. *IEEE Journal of Solid-States Circuits*, **48**, 1429-1441.

[14] Kull, L., Toifl, T., Schmatz, M., Francese, P.A., Menolfi, C., Braendli, M., Kossel, M., Morf, T., Andersen, T.-M. and Leblebici, Y. (2013) A 3.1 mW 8 b 1.2 GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32 nm Digital SOI CMOS. *IEEE International Solid-State Circuits Conference Digest Technical Papers*, San Francisco, 17-21 February 2013, 468-469.