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A Quadrature Oscillator Based on a New "Optimized DDCC" All-Pass Filter

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ABSTRACT

In this paper, a new voltage-mode (VM), all-pass filter utilizing two second-generation current conveyors and tow differential difference current conveyors (DDCCs) is proposed. This filter uses a number of passive elements grounded capacitor. This structure of filter is used to realize a quadrature oscillator. The proposed circuits employ tow optimized differential difference translinear second generation current conveyers (DDCCII). These structures are simulated using the spice simulation in the ADS software and CMOS 0.18 μm process of TSMC technology to confirm the theory. The pole frequency can be tuned in the range of [11.6 - 39.6 MHz] by a simple variation of a DC current.

Keywords: Proposed Current Controlled Oscillators; CMOS 0.18 μm Process of TSMC; Current Conveyor; Differential Difference Current Conveyors

1. Introduction

Differential difference current conveyors (DDCCs) are useful current-mode building blocks and many authors have demonstrated their versatility in CMOS analog circuit esign [1]. Generalized impedance converter, filter, oscillator, quadrature oscillator, floating or grounding resistor and inductance simulation are an important domain of application of DDCCs [2-4]. Indeed, the realization of voltage-mode (VM) first-order all-pass filters is quite recent [5]. These structures present some advantages, such as the possibility to control the frequency or the gain after integration [6-8]. DDCC-based filter or quadrature oscillator presents a good solution to avoid limitations of Surface Acoustic Wave, such as problems of integration, impedance matching, tuning, linearity, etc [3,6].

In order to get tuning parameters for the proposed structure, translinear differential difference second generation current controlled conveyor based structure seems to be the most attractive [9-11]. This DDCC gives a possibility to control the functions [5-8] characteristics by parasitic resistor at port X by means of a current source [12-14]. These DDCCs are extended in CMOS technology to realize a high frequency application such as filters, oscillators, quadrature oscillator and buffer [10,15,16]. To minimize the problem given by the passive element, floating and grounding resistor or floating and grounding capacitor or floating and grounding inductor, DDCC seems to be the most attractive [3,4,14].

This paper is organized as follows: In Section II, we present the proposed all-pass filter which uses two second generation current conveyor and two optimized differential difference current conveyors (DDCCs) and one grounded capacitor. This structure is ameliorated by replacing the grounding capacitor by CMOS Varactors. In Section III, we give the optimized DDCC implementation CMOS 0.18 μm process of TSMC technology. After this, we illustrate the simulation results of the optimized differential difference translinear second generation current conveyors (DDCCs) implemented in 0.18 μm CMOS technology. In Section IV, we illustrate the simulation results of the proposed DDCC all pass filter. In Section V, we present the CCII-based Quadrature oscillator architecture. This application using the proposed filter connected to an integrator in a closed loop. Finally, to validate theoretical analysis, the different circuits are

designed and simulated using spice simulation in the ADS software.

2. The Proposed All-Pass Filter

A number of current and voltage mode all-pass filters employing the DDCC have been suggested [17]. However most of these realizations employ floating capacitors and resistors which require a large area to be implemented by MOS transistors. The proposed structure use two DDCC, two CCII and only grounded capacitor. The input of the voltage-mode (VM) all-pass filter is connected to the Y terminal (high input impedance) and its output is connected to the X terminal (low output impedance). For this reason the proposed structure doesn't necessitate a buffer cascade with another bloc. The architecture of the filter is given in **Figure 1**.

The transfer function and the phase of this filter can be expressed by:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 - jCR_{eq}w}{1 + jCR_{eq}w} \tag{1}$$

$$\theta(w) = -2\text{arctg}\left(R_{eq}Cw\right) \tag{2}$$

The pole frequency of the filter is calculated as:

$$f_o = \frac{1}{2\pi CR_{eq}} \tag{3}$$

The type of the filter gives a good solution to realize a controlled Quadrature oscillator [17]. The oscillator frequency can be adjusted by means of the value of the capacitor or the bias current of $CCII_{2,3}$ (the value of R_{eq}). However the capacitor values are not variable after integration, for this reason we present an ameliorate structure for the filter when we replaced the grounding capacitor by CMOS Varactors or by a multiplier capacitor [18]. **Figure 2** displays the architecture of the ameliorated filter.

3. The Optimized Differential Difference Translinear Current Conveyor

The DDCC is a four terminal active block. The symbol and the equivalent circuit of the the DDCC are illustrated in **Figure 3**.

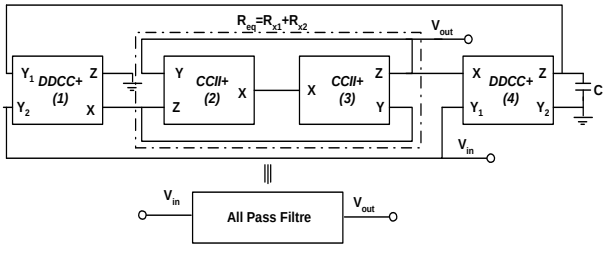

Figure 1. The proposed all-pass filter.

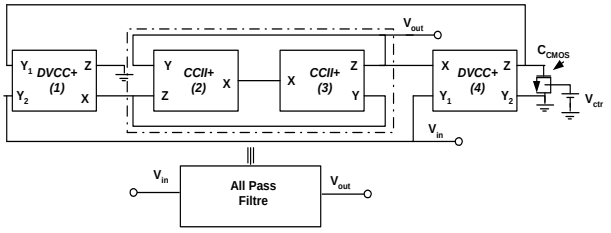

Figure 2. The ameliorated all-pass filter.

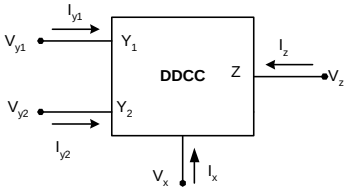

Figure 3. General representation of DDCC.

The DDCC ensures two functionalities between its terminals:

- A Current follower between terminals X and Z.
- A Voltage follower between terminals X and (Y_1 - Y_2).

In order to get ideal transfers, a DDCC should be characterized by low impedance on terminal X and high impedance on terminals Y_1, Y_2 and Z. In this configuretion, the relation between terminal voltages and currents can be given by the following matrix:

$$\begin{pmatrix} V_x \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix} \tag{4}$$

To realize this structure it's necessary to cascade CMOS differential voltage buffer (DVB) with a CCII. An implementation of the CMOS differential voltage buffer (DVB) and the CCII are respectively shown in **Figures 4** and **5** [2-4].

A. CMOS Differential Voltage Buffer

The (DVB) is shown in **Figure 4** [3,4]. The input transconductance elements are realized with two differential stages (M1 and M2, M3 and M4). The high gain stage is composed of a current mirror (M5 and M6). It converts the differential current to a single-ended output current (M7). The output voltage of this amplifier can be expressed as:

$$V_x' = \beta_{y1}V_{y1} - \beta_{y2}V_{y2} \tag{5}$$

where

$$\beta_{Y1} \approx \frac{g_{m7}g_{m1}\left(g_{m6} + g_{d2} + g_{d4} + g_{d6}\right)}{g_{m4}g_{m5}g_{m7} + g_{m6}g_{d7}\left(g_{d1} + g_{d3} + g_{d5}\right)} \tag{6}$$

$$\beta_{Y2} \approx \frac{-g_{m\acute{e}}g_{m5}g_{m7}}{g_{m4}g_{m5}g_{m7} + g_{m6}g_{d7}\left(g_{d1} + g_{d3} + g_{d5}\right)} \tag{7}$$

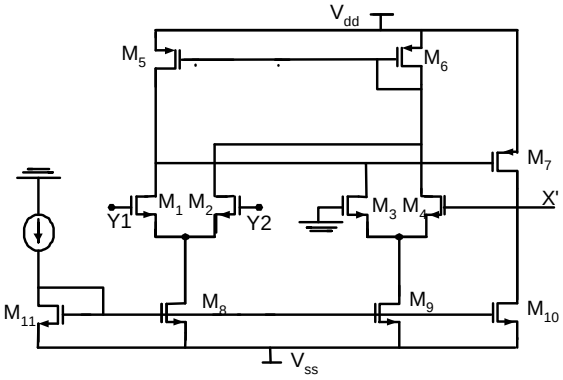

Figure 4. CMOS differential voltage buffer.

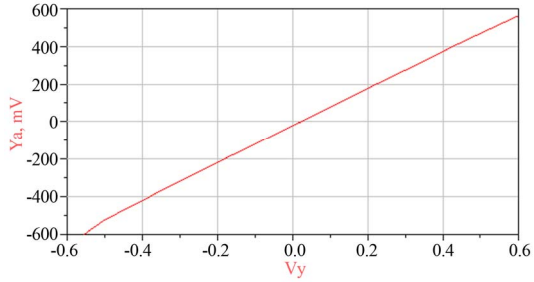

Figure 5. Voltage DC transfer characteristic of the DVB (where *Ya* = *Vx'* and *Vy* = *Vy*$_1$ - *Vy*$_2$).

To determinate the optimal transistor sizes (W and L) for this structure we will use the heuristic methodology [6,7]. This strategy consists on minimizing the impedance output value, assuming that the current mirror has unity gain and closer β_{y1} and β_{y2} to the unity. The output resistor is calculated as:

$$Z_{x'} \approx \frac{g_{m6}\left(g_{d1}+g_{d3}+g_{d5}\right)}{g_{m4}g_{m5}g_{m7}+g_{m6}g_{d7}\left(g_{d1}+g_{d3}+g_{d5}\right)} \qquad (8)$$

Simulation conditions are summarized in **Table 1** and the resultant optimal transistor sizes (W and L) are presented in **Table 2**.

The optimized CMOS differential voltage buffer was simulated with Spice simulation in the ADS software. Main obtained results are represented in **Figures 5** and **6**. **Figure 5** displays the DC transfer characteristics of the DVB. The voltage transfer can be linear between −0.6 V and 0.6 V. Moreover, the bandwidths of output terminals are shown in **Figure 6**. The −3dB bandwidths of $V_x'/\left(V_{y1}-V_{y2}\right)$ are located at 3.75 GHz.

The time-domain response of the optimized DVB is shown in **Figure 7**. A sine wave of 100 mV and −100 mV amplitude and 200 MHz is respectively applied as the input Y_1 and Y_2 to the filter. We notice that the output Waveforms are confused with the differential input Waveforms $V_{y1}(t)$ - $V_{y2}(t)$. This result confirms the good functionality of this structure.

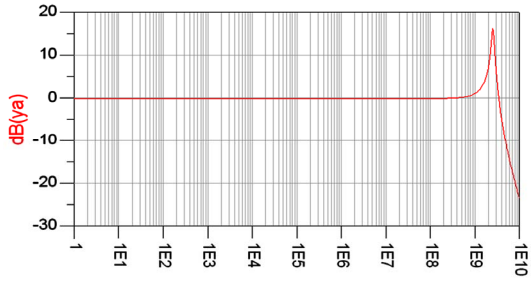

Figure 6. Frequency response of the voltage follower *Vx'*/ (*Vy*$_1$ - *Vy*$_2$).

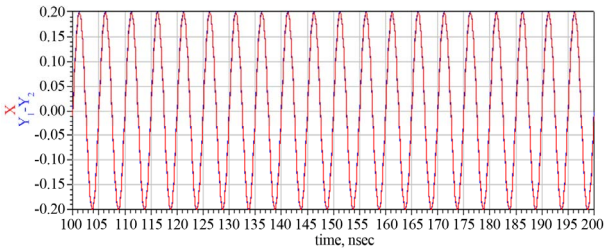

Figure 7. The simulation result of voltage waveforms of *Vx'* and (*Vy*$_1$ - *Vy*$_2$).

Table 1. Simulation conditions.

Technology	0.18 µm CMOS
Supply voltage	1.5 V
Bias current	100 µA

Table 2. Optimal device sizing.

Device Name	Aspect ratio W/L (µm)
M5-6	13.725/0.18
M1-4	0.25/0.18
M7	7/0.18
M8-11 (current mirrors)	3.05/0.18

B. Transinear Loop Based CCII Configurations

An implementation of the second-generation translinear loop based current conveyor with a positive current transfer from X to Z (CCII+) is shown in **Figure 8** [7]. In **Table 3** we give the different transistor size.

Table 3 shows the optimal device scaling that we get after applying the optimization approach.

The static and dynamic characteristics of the translinear configuration are summarized at **Table 4**.

4. Simulation Results of the Proposed All-Pass Filter

The VM all-pass filter (**Figure 1**) is simulated with the SPICE program using 0.18 µm TSMC CMOS technol-

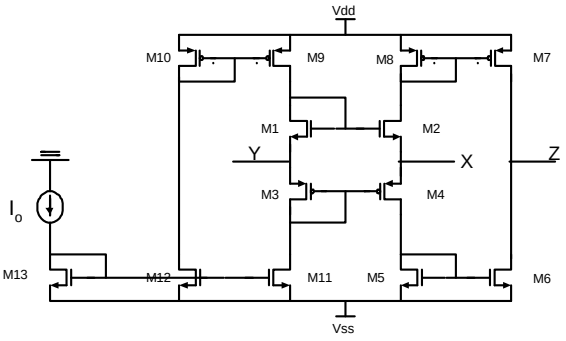

Figure 8. Translinear loop MOS based implementation of CCII.

Table 3. Optimal device sizing.

Device Name	Aspect ratio W/L (μm)
M1, M2	6.1/0.18
M3, M4	27.45/0.18
Mxx (in PMOS current mirrors)	13.725/0.18
Mxx (in NMOS current mirrors)	3.05/0.18

Table 4. Performance characteristics of the optimized CCII with Io = 100 μA and 1.5 supply voltage.

Voltage gain β	0.943
Current gain α	1.1
Fci	2.7 GHz
Fcv	4.33 GHz
Relative current Error	0.15%
Relative Voltage Error	0.093%
Input Impedance (RY//CY)	18 KΩ//87 fF
Input Impedance (Rz//Cz)	24 KΩ//25 fF
Input Resistance Rx	380 Ω
The offset current	−2.2 μA
The offset voltage	13 mV

ogy. The CMOS implementation of the DDCC+ is shown in **Figure 9**. The transistor aspect ratios of MOS transistor were chosen as in **Tables 2** and **3** and the supply voltage was ±1.5 V. The biasing current was taken respectively as 100 μA for the DDCC and 30 μA for the CCII ($R_{eq} = R_{X2} + R_{X3}$ = 1.5 KΩ). The simulation results for the magnitude and phase responses of Vout are shown in **Figure 10** where we take C = 6 pF. In this figure, the pole frequency of 19MHz is obtained. The pole frequency is 19 MHz instead of 17.7 MHz owing to the effect of the parasitic impedances of the DDCC. The relative error between theoretical and simulation value is equal to 7%.

To confirm this result, the circuit is inputted with a sinusoidal signal of 19 MHz. The input and +90˚ phase shifted output (V_{out}) are shown in **Figure 11**. **Figure 12**

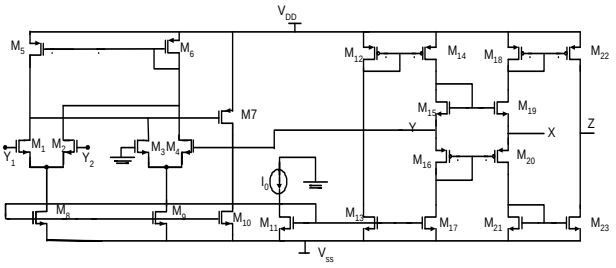

Figure 9. CMOS realization of the DDCC.

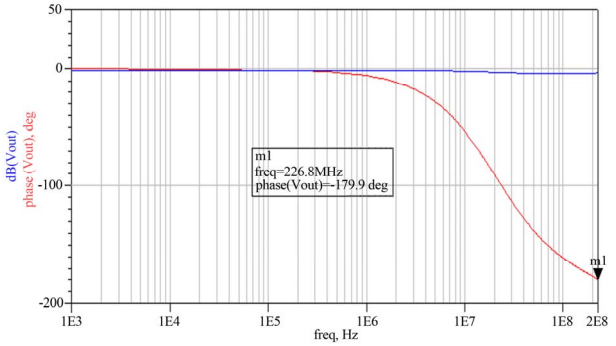

Figure 10. Gain and phase responses of proposed all-pass section.

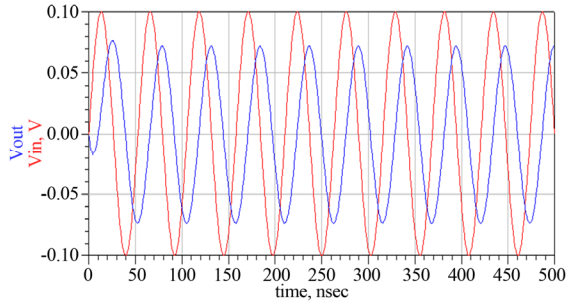

Figure 11. Input and output waveforms for the circuit at 19 MHz.

shows the variability of the pole frequency of **Figure 1** with the bias current $I_{o2,3}$. The pole frequency can be controlled in the range [11.6 MHz, 36.6 MHz] by varying $I_{o2,3}$ in the range [10 μA, 200 μA].

5. Quadrature Oscillator Based on the Proposed All-Pass Filter

To illustrate the utility of the proposed first-order all-pass filter (high input and low output impedances), no buffer is required to connect it to the integrator circuit $\left(V_{out} = -2/(sRC\omega)\right)$ [18]), it is connected in cascade to an integrator in a closed loop [17] to construct a quadrature oscillator, as shown in **Figure 13**. It is seen that the proposed architecture uses three optimized CMOS DCCIIs, tow CCII's, one floating resistor and tow grounded capacitors. The corresponding characteristic

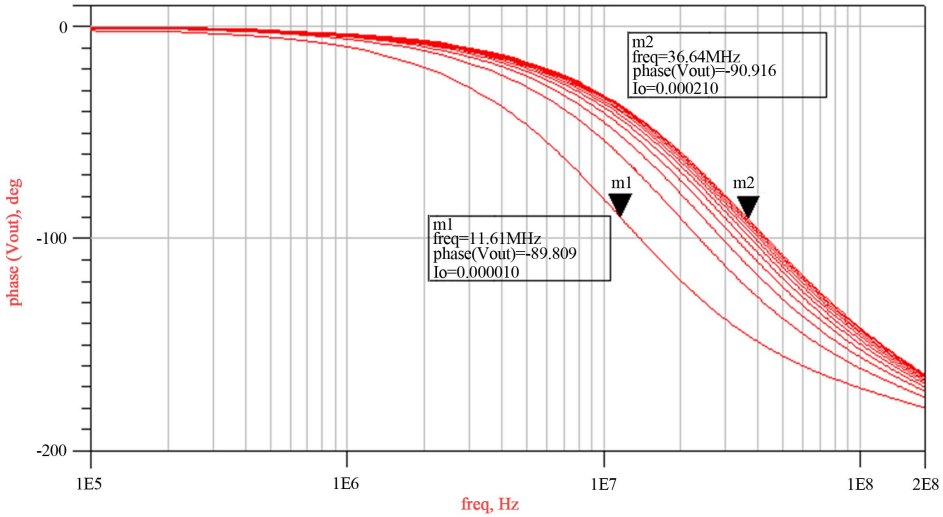

Figure 12. Pole-frequency tuning with bias current $I_{o2,3}$.

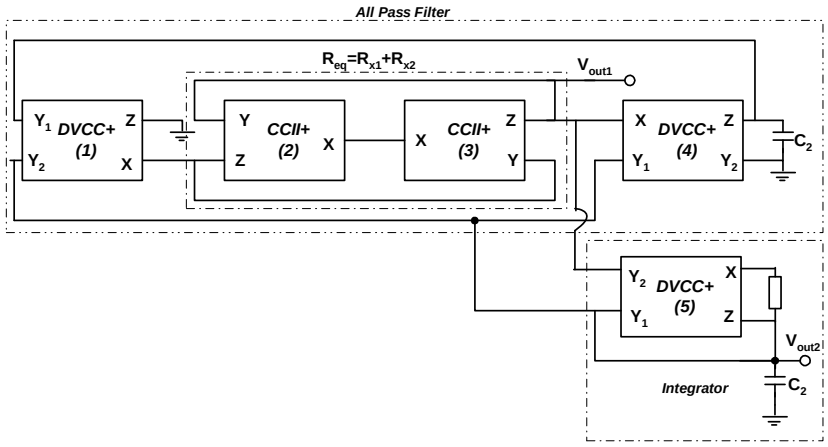

Figure 13. The proposed quadrature oscillator implementation.

equation is given by:

$$s^2 + s\left(\frac{1}{C_1 R_{eq}} - \frac{1}{RC_2}\right) + \frac{2}{C_1 R_{eq} C_2 R} = 0 \qquad (9)$$

This leads to the following oscillation condition and oscillation frequency respectively:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{2}{C_1 R_{eq} C_2 R}} \qquad (10)$$

$$CO: C_1 R_{eq} \geq C_2 R \qquad (11)$$

The confirmed performance of the quadrature oscillator can be seen in **Figure 14**, showing the responses of the oscillator where C_1 = 6 pF, C_2 = 10 pF, R = 600 Ω, and $I_{o2,3}$ = 30 μA ($R_{eq} = R_{X2} + R_{X3}$ = 1.5 KΩ). The phase difference between two out puts V_{out1} and V_{out2} is 90° and the oscillation frequency is equal to 26 MHz (the theoretical value of the oscillation frequency is 30.5 MHz).

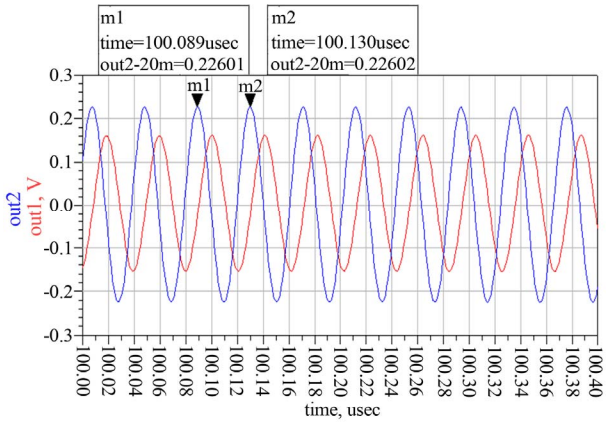

Figure 14. The simulated quadrature output waveforms of V_{out1} and V_{out2}.

The quadrature relationships between the generated waveforms have been verified using Lissagous figure and shown in **Figure 15**.

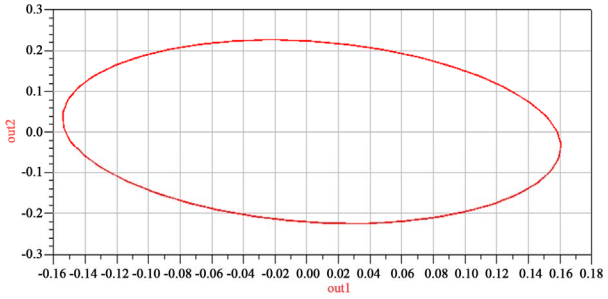

Figure 15. Lissagous figure.

6. Conclusion

In this paper, we have proposed a new design of VM first-order all-pass filter. In order to get high performances of the filter, a translinear DCCII and CCII structures are optimized in 0.18 µm CMOS process of TSMC. The theoretical analysis is verified with the SPICE simulation program. The application example as the quadrature oscillator is included. It shows good usability of the proposed all-pass filter.

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