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Millimeter Wave Ring Oscillator Using Carbon Nano-Tube Field Effect Transistor in 150 GHz and Beyond

Davood Fathi*, Baback Beig Mohammadi
School of Electrical and Computer Engineering, Tarbiat Modares University (TMU), Tehran, Iran
Email: *davfathi@modares.ac.ir

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ABSTRACT

Carbon Nano-Tube Field Effect Transistors (CNTFETS) are the competitor of the conventional MOSFET technology due to their higher current drive capability, ballistic transport, lesser power delay product, higher thermal stability, and so on. Based on these promising properties of CNTFETs, a CNTFET-based millimeter wave ring oscillator operating around 150 GHz and beyond is introduced here in 32 nm technology node. To prevent overestimation, the CNT interconnects between transistors are also included in simulation, which are assumed to be a single layer of ballistic metallic CNTs in parallel. For the sake of simplicity in RF design, the oscillator is based on CNTFET-based inverters. The inverters with DC gain of 87.5 dB are achieved by proper design with the non-loaded delay around 0.6 ps, which is at least one order of magnitude better than the same 32 nm MOSFET-based inverters. The oscillator's average power consumption is as low as 40 μW with the fundamental harmonic amplitude of around −6.5 dB. These values are, based on our knowledge, for the first time reported in the literature in CNTFET-based oscillator designs. Also, on the average, the performance of the designed oscillator is 5 - 6 times better than MOSFET-based designs.

Keywords: CNTFET; CNT Interconnect; Millimeter Wave; Ring Oscillator

1. Introduction

Carbon nanotubes (CNTs) have shown promising electrical and mechanical performance over the conventional materials used in semiconductor industry. Electrically, CNTs are divided into two major groups: metallic and semiconducting, based on their chirality [1]. The metallic CNTs are used as interconnect in the novel integration processes [2,3] and the semiconducting ones are used in the novel semiconductor devices, beyond the conventional silicon/GaAs based technologies, like Carbon Nano-Tube Field Effect Transistors (CNTFETs) [4].

The large mean free path and hence, the ballistic transport characteristic of CNTs [5] with high current density capability, combining with extraordinary mobility [6] and very low shot noise [7], leads to CNTFETs with acceptable and outstanding electrical characteristics like high transit and maximum frequency [8] and inherent linearity [9].

Here, we present a high performance, low power CNTFET-based ring oscillator at 150 GHz and beyond with good THD. The amplitude of fundamental frequency of oscillation achieves around −6.5 dB which is to our knowledge 4 - 5 times better than the same MOSFET-based ring oscillators. The CNTFET used in this paper is a MOSFET-like CNTFET with gate length of 32 nm. In order to prevent overestimation of the ring oscillator performance, the CNT interconnects between CNTFETS are modeled and included in simulation, which have been arranged in a single layer of ballistic metallic CNTs.

This paper is organized as follow. Section II includes explanations on the CNTFET and its model used in our simulations. In Section III we discuss the modeling of metallic CNTs as interconnects. CNT-based inverter design and advantages over MOSFET-based inverters and its corresponding simulation results are represented in Section IV. Section V includes CNTFET-based ring oscillator design and simulation results. Finally, Section VI concludes this paper.

2. CNTFET and Its Modeling

There are several CNTFET models reported in literature [10-13]. The model used here is based on the [12,13].

*Corresponding author.

This model includes all the necessary parameters needed for simulating CMOS-like CNTFETs (*n*-type and *p*-type) up to the minimum gate length of 10 nm for both large signal and small signal simulations. These parameters are quantum confinement effects on both circumferential and axial directions, acoustic, elastic and optical scattering in the channel region, screening effects of CNTs in parallel under the gate, resistive source and drain, Schottky barrier effects and the parasitic gate capacitances [12,13].

As mentioned before, the CNTFET used here is CMOS-like CNTFET. This is due to superior device parameters and fabrication feasibility of MOSFET-like CNTFETs compared with the Schotkey barrier controlled FETs [14] which makes CMOS-like CNTFETS suitable for our purpose of operating at 150 GHz and beyond.

Figure 1 shows the CMOS-like CNTFET 3D Structure. The CNTs under the gate are intrinsic and are used in such a condition that they are semiconducting. According to the analysis reported in [1], CNTs with the chirality vector (n, m) are semiconducting when $n - m \neq 3k$ where k is an integer. For instance, a CNT with the chirality vector (19, 0) will behave as a semiconductor.

All the CNTs simulated in this CNTFET model are assumed to be semiconducting. Of course, this is an optimistic assumption, there are so many methods developed to purify the semiconducting CNTs from metallic types. In [1], there is a method to fabricate arrays of CNTFETs without the need to separate semiconducting CNTs from metallic types, called "constructive destruction", which is beyond our scope. The existence of metallic CNT under the gate would yield in the performance degradation through the reduction of transconductance of transistor and the increase of idle power consumption.

Despite the fact that the back-gated structure for CNTFETs is preferred to top-gate one due to simplicity in device production; we have used the top-gated topology. This is because the top-gated topology will yield higher control of gate on the channel region which enhances the transistor ability to perform better than the back-gated topology at high frequencies. Also, the structure of the circuit does not let us to utilize the back-gated topology, because the substrate that performs as the back gate is shared among all the transistors in our design.

The source and drain extensions are assumed to be made with the help of doped CNTs in parallel. This would help the device to enhance the performance of the transistor through the reduction of parasitic capacitances significantly [15]. Of course, an attention must be made that according to the lessening of mean free path of doped CNTs versus intrinsic CNTs, the length of the extended regions must be short enough in order to benefit from ballistic transport phenomena. So, there is a trade-off between parasitic capacitance reduction and ballistic transport at the extended highly doped CNT regions.

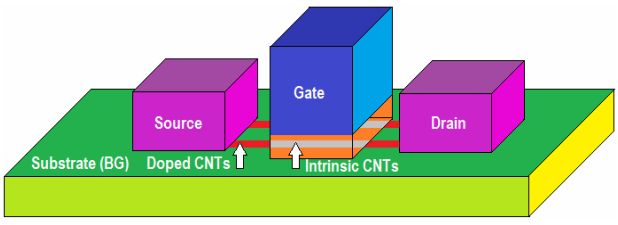

Figure 1. The three dimensional CMOS-like CNTFET structure.

The work function of conventional CNTs with the radius of 1 - 2 nm would be around 4.5 eV which is in a good agreement with palladium [13]. So, the palladium is used as the source and drain metal contacts. Also HfO_2 with 4 nm thickness and relative permittivity of 16 has been used as the high-*k* gate insulator in our design.

The diameter of a CNT can be calculated from

$$d = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \quad (1)$$

where n and m are the indices of chirality vector (n, m) and a is the lattice constant of CNT which is around 2.46 Å. Relation (1) suggests that for a CNT with chirality vector of (19, 0) a radius of 1.5 nm must be assumed. This radius is less than the 4 nm thickness of the gate dielectric. So, there is no need to further increasing the gate insulator thickness.

The CNTs under the gate would have screening effect on each other which would degrade the CNTFET performance with increasing the number of CNTs under the gate despite the fact that increasing the number of CNTs under the gate, at first glance, must theoretically increase the transconductance of the transistor. This phenomenon will introduce an important tradeoff between the number of the CNTs under the gate and maximum CNTFET achievable performance. As a result, a distance of 4 nm is assumed between each CNT tube pairs. Further increasing of this distance will lead to undesirable increasing of the gate width which adds up more parasitic capacitances to the circuit.

We have used Stanford University CNFET HSPICE model v. 2.2.1 in simulating CNTFETs.

3. CNT Interconnect Modeling

Due to the high frequency simulation, it is necessary to include the interconnect modeling in the design. Because of the good matching between palladium source/drain contacts' work-function and the metallic CNTs' and according to high durability of CNTs, we choose to use CNTs as interconnect material between our logic gates described in the next section.

According to [2], due to longer mean free path of single walled carbon nanotubes versus multi walled ones, it

is desirable to use SWCNTs as the interconnect material. For decreasing the resistance of the SWCNT, we may use single layer paralleled CNTs. **Figure 2** shows the model for parallel CNT interconnects used in our design.

The resistance of a SWCNT is divided into two parts: Quantum resistance (R_Q) and Scattering resistance (R_S) [2]. The Quantum and scattering resistances can be calculated using [16]

$$R_Q = \left(\frac{h}{4e^2}\right); \quad l < \lambda, \tag{2}$$

$$R_S = \left(\frac{h}{4e^2}\right)\left(\frac{l}{\lambda} - 1\right); \quad l > \lambda \tag{3}$$

where, λ is the mean free path, l is the length of CNT, h is the Plank's constant, and e is the electron charge.

When the length of CNT is shorter than the mean free path, the resistance is reduced to $h/4e$ which is the value of quantum resistance and remains constant at this value. This condition is maintained in our design. For longer lengths, the electron scattering increases the resistance with a linear increasing behavior.

Though the value of quantum resistance is high in ballistic CNTs; the capacitance of the CNT is significantly small, making the delay of the ballistic CNT small enough for our purpose.

The capacitance also is divided into 2 parts: The electro static capacitance (C_E) and quantum capacitance (C_Q). The electro static capacitance between a CNT with diameter of d and the ground plane at the distance of h from the center of CNT can be calculated using (4). For a typical value of h/d, this capacitance can be approximated, with the typical value of 50 aF/μm, as [3]

$$C_E = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2h}{d}\right)} \approx \frac{2\pi\varepsilon}{\ln\left(\frac{h}{d}\right)}. \tag{4}$$

The quantum capacitance is in series with the electrostatic capacitance and can be calculated using [3]

$$C_Q = \frac{e^2}{\hbar\pi v_F}. \tag{5}$$

The value of this capacitance is around 100 aF/μm, with e as the electron charge, $\hbar$ as the Plank's constant and v_F as the Fermi velocity [3]. Also, a coupling capacitance exists between each pair of CNT interconnects, which is named C_C in **Figure 2**. The coupling capacitance between two CNTs with diameters of d at the space of D can be calculated using [3]

$$C_C = \frac{\pi\varepsilon l}{\ln\left(\frac{D}{d} + \sqrt{\left(\frac{D}{d}\right)^2 + 1}\right)}. \tag{6}$$

According to the previous discussion, we have assumed 4 nm space between each pair of CNT interconnects, in order to prevent the screening effect and also to decrease the coupling capacitances significantly. The total inductance of a CNT interconnect is also divided into two parts: The kinetic inductance (L_K) and the magnetic inductance (L_M). The kinetic inductance of a CNT can be obtained using [3]

$$L_K = \frac{\hbar\pi}{e^2 v_F}. \tag{7}$$

The value of this inductance has been assumed to be 16 nH/μm in our design. In addition to the kinetic inductance, there is a magnetic inductance in the structure of a CNT interconnect model. This inductance is small in comparison with the kinetic inductance and can be approximated to have a value of about 1 nH [3]. The exact value of the magnetic inductance can be obtained using [16]

$$L_M = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2h}{D}\right) \tag{8}$$

where μ is the carrier mobility and the other parameters in (8) are identical to those defined before. It should be noted here that, due to CNT's band structure and electron's two different spins, there are 4 conductive channels for each CNT. As a result, the effective quantum capacitance of a single CNT is four times the quantum capacitance introduced in (5). On the other hand, the effective kinetic inductance would be one quarter of the kinetic inductance in (7). So, we used $C_{Q,\,eff}$ and $L_{K,\,eff}$ in our simulations

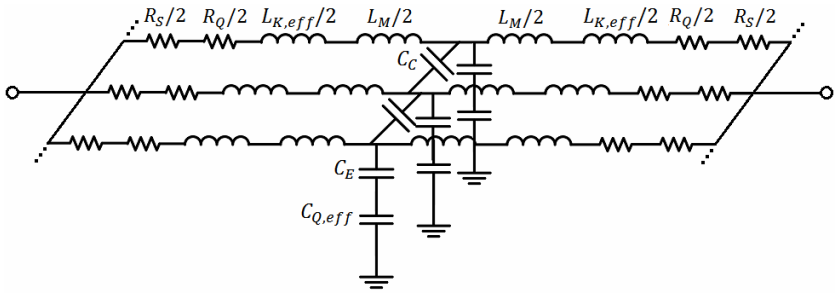

Figure 2. Parallel CNTFET interconnect model.

$$C_{Q,eff} = 4C_Q , \quad (9)$$

$$L_{K,eff} = \frac{L_K}{4} . \quad (10)$$

4. CNTFET-Based Inverter Design

The core of the high frequency ring oscillator is based on inverters. The higher speed inverter will lead to higher frequency ring oscillator.

The high to low and low to high delays in inverters play an important role in frequency determination of an inverter based ring oscillator. Here, the total delay is a function of several parameters like the time constant of each inverter, supply voltage and the delay introduced by interconnects and connections to other gates in a real implementation.

The delay of a CNTFET based inverter is a function of CNTFET diameter under the gate. It is shown in [13] that the FO1 delay of CNTFET based inverter would be at its minimum constant value when the diameter of the CNT is around 1.4 and beyond. So, we have chosen the diameter of CNTs to be about 1.5 nm which is obtainable by a (19, 0) CNT. It must be mentioned here that for CNTs with less than 1.3 nm diameter, the higher source/drain resistance with smaller current drive capability and hence, lower speed would be resulted [13].

There is a difference between MOSFET-based and CNTFET-based inverter design. In CMOS, there is a bulk connection for each NMOS and PMOS transistor that must be connected to proper voltages to reversely bias the *p*-*n* junctions. But here, due to physically different operational concept of CNTFETS, we have no such a connection. The back gate of the *n*CNTFET and *p*CNTFET are both the substrate and are connected to ground node in our design.

With supply voltage equal to 0.9 volts in order to prevent dielectric punch through and with proper design, the high to low and low to high delays of our CNTFET-based inverters are measured to be around 0.3 ps. The DC gain of the CNTFET-based inverter is about 87.5 dB with 5 CNTs under the gate; a value that is rarely achievable with the CMOS technology.

Figure 3 represents the voltage transfer function of a 32 nm CNTFET-based inverter and MOSFET-based inverter with different supply voltages. The significant improvement of the DC gain of the CNTFET-based inverter over MOSFET-based one is evident.

The power delay product and maximum leakage power of the CNT-based and MOSFET-based inverters are plotted versus different supply voltages and temperatures in **Figures 4** and **5** respectively.

As seen from **Figure 4**, CNTFET-based inverter has better performance by means of maximum leakage power

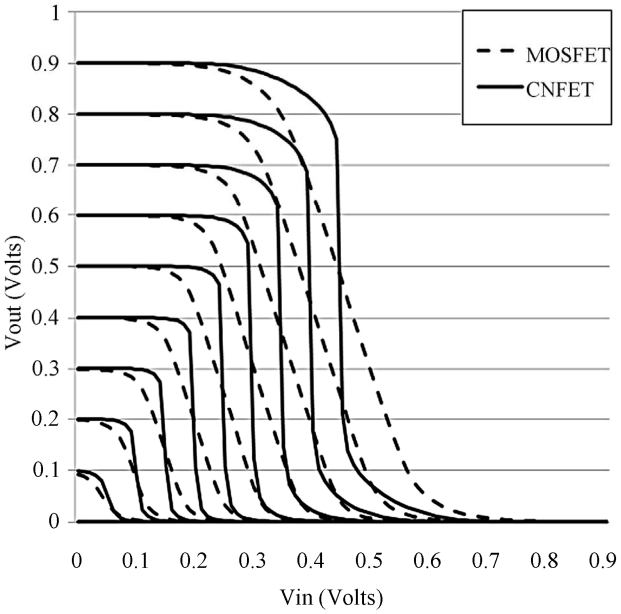

Figure 3. 32 nm CNTFET-based and CMOS based inverters' voltage trasfer function for different supply voltages [17].

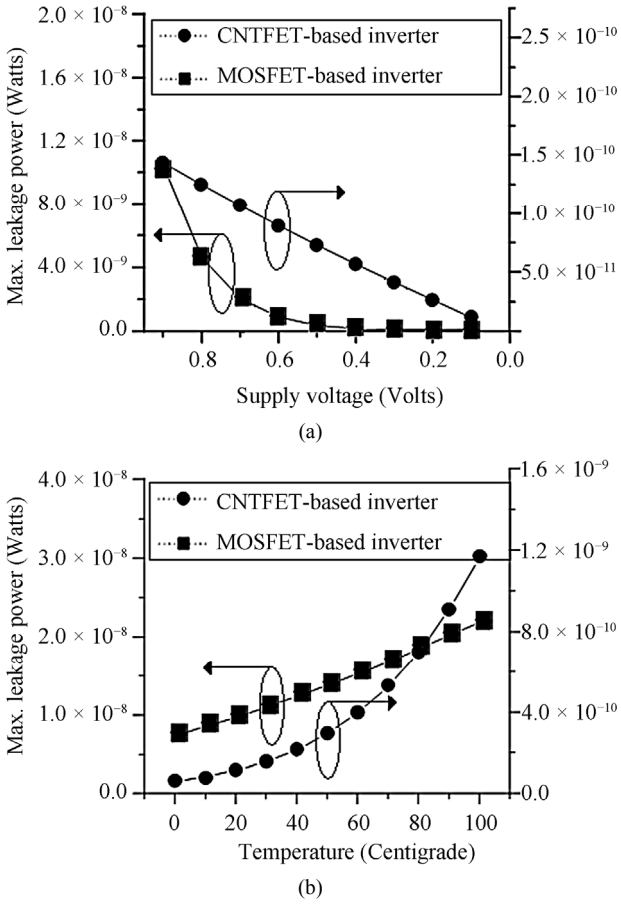

Figure 4. The maximum leakage power of CNTFET-based and MOSFET-based inverters versus (a) supply voltage and (b) temperature changes [17].

in both different supply voltages and different temperatures. On average, the overall CNTFET-based inverter's leakage power is 40 times lesser than the MOSFET-based inverter's.

Figure 5 illustrates the power delay product of CNTFET-based and MOSFET-based inverters with different supply voltages and in different temperatures. Again, the CNTFET-based inverter wins against MOSFET-based inverter.

Despite the fact that leakage power of CNTFET-based inverter increases exponentially with temperature, the overall leakage power on CNTFET-based inverter is about 25 times lesser than MOSFET-based inverter. Also, due to the strong stability of CNTs' electrical characteristics against thermal variations [17], the power delay product of CNTFET-based inverter does not change sensibly in **Figure 5(b)**.

It must be mentioned here that an overall improvement factor of at least 5 - 6 is achievable utilizing CNTFETs instead of MOSFETs by means of delay, power consumption and thermal stability [13,17].

The process variation is also important in designing and integrating reproducible electronic products. According to [17] the effective process variations in CNTFETs are different from those important in MOSFETs. The MOSFETs are 60 (26) times more sensitive to length (width) variation in gate dimensions than the CNTFETs. This is due to the fact that the current of CNTFETs is not directly related to the width and length of the channel under the gate and mostly is controlled through the number of CNTs under the gate and their chirality. Of course, this means that the purity control of CNTs under the gate is much important than dimension control in CNTFETs. It can be found that a 10% change in CNT diameter would yield a 17% change in CNTFETs current in 32 nm technology node with 0.9 V supply voltage.

5. CNTFET-Based Ring Oscillator Design

For the sake of simplicity in RF design, we have chosen the simplest inverter based ring oscillator. The ring oscillator designed here is based on the inverter-based structure including three inverters in series making a closed loop. The minimum number of three inverters is chosen to achieve the highest frequency of oscillation. The frequency of the oscillation may be predicted by

$$F = \frac{1}{2\pi N\left(\tau_{PHL} + \tau_{PLH}\right)} \tag{11}$$

where N is the number of inverter stages in ring, τ_{PHL} is the high to low delay and τ_{PLH} is the low to high delay of each inverters having all the parasitic loads at input and output nodes.

The interconnect structure between the three inverters

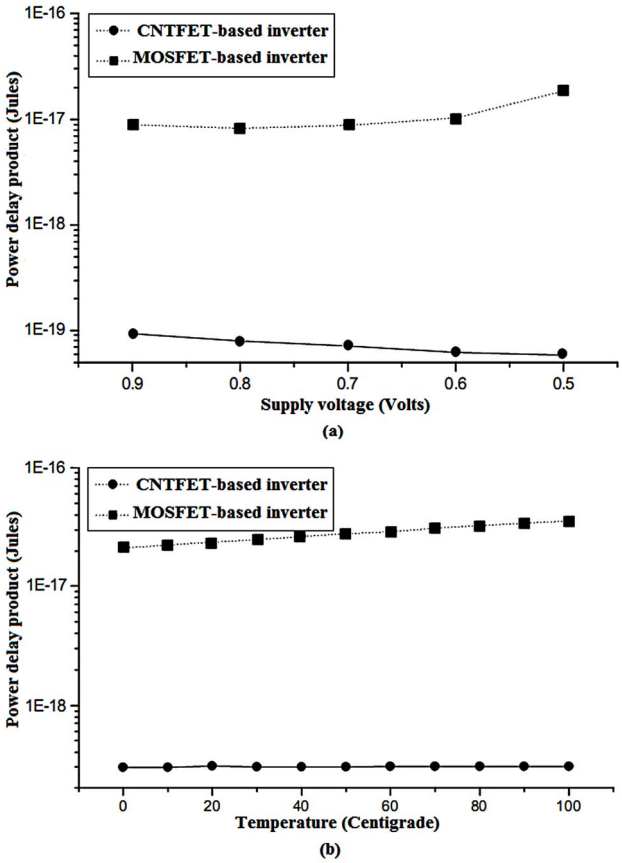

Figure 5. The power delay product of CNTFET-based and MOSFET-based inverters versus (a) supply voltage and (b) temperature changes [17].

play an important role in defining the total delay of each state and hence, the maximum achievable oscillating frequency. The interconnect modeling has been discussed previously in Section III. Our suggestion is to connect the inverters as packed as possible by stretching the palladium used in the gate while closing the loop using the CNT interconnect structure, to benefit from the fixed and noiseless conductance of metallic CNTs discussed before.

As mentioned before, there are tradeoffs between different parameters like the number of metallic CNTs in a paralleled single layer set and the parasitic capacitors, the number of CNTs under the gate and CNTFET performance and delay through screening effects and gate width which will introduce more capacitors and so on. So, we have simulated different conditions to achieve the best performance of the ring oscillator by means of higher frequency and higher fundamental harmonic amplitude with lower total harmonic distortion. All the simulations are done in HSPICE simulator environment.

Table 1 represents the simulation results for different number of metallic CNTs in the single layer interconnect structure in the closing loop of ring oscillator, as shown

Table 1. Oscillation frequency, fundamental harmonic amplitude, total harmonic distortion, average power consumption and FOM for different number of CNTs in parallel as interconnect (gate length = 32 nanometers and number of CNTs under the gate = 5).

Number of CNTs in Parallel as Interconnect	Oscillation Frequency (GHz)	Fundamental Harmonic Amplitude (dB)	THD (%)	Average Power Consumption (μW)	FOM
1	95.71	−5.98	11.49	25.46	0.164
2	125.93	−6.25	9.93	35.37	0.174
3	141.04	−5.87	14.6	40.57	0.120
4	156.15	−7.54	5.11	42.7	0.299
5	161.19	−5.95	14.98	43.48	0.125
6	166.23	−7	4.25	43.59	0.400
7	166.23	−7.33	3.47	43.73	0.471
8	171.27	−7.34	4.95	43.92	0.338
9	171.27	−6.13	13.5	44.07	0.142
10	171.27	−5.89	16.81	44.32	0.116

in **Figure 6**. Increasing the number of CNTs will increase the oscillation frequency, due to the increase of driving capability of inv. #3 and the reduction of interconnect resistance. But eventually, after achieving the required driving capability, increasing the number of CNTs will introduce more parasitic capacitances to the circuit and consequently, the oscillator performance will be degraded. As **Figure 7** shows, based on **Table 1**, the optimal condition for 32 nm technology node is achieved when 7 metallic CNTs are in parallel as interconnect. The similar result will be achieved with 5 semiconducting CNTs under the gate.

The figure of merit (FOM) in **Table 1** is calculated using

$$\mathrm{FOM} = \frac{\mathrm{FHM} \cdot \mathrm{OF}}{\mathrm{THD} \cdot \mathrm{APC}} \qquad (12)$$

where FHM is the fundamental harmonic amplitude, OF is the oscillation frequency, THD is the total harmonic distortion, and APC is the average power consumption.

As **Table 2** shows, the oscillation frequency decreases as the number of CNTs under the gate increases, due to the increase of 3 factors: the parasitic capacitances, the length of interconnect, and the screening effects which are not desired in our design.

There are very few CNTFET-based ring oscillators reported in the literature. The simulation results obtained here are far beyond the results reported previously by the others in the literature. In [18], a three stage ring oscillator has been implemented, which does not benefit from the ballistic transport. Due to very large sizes of inverters, the oscillation frequency is about 220 MHz. Also, more novel oscillators reported in [19,20], have achieved the oscillation frequencies of around 80 MHz and 500 MHz respectively.

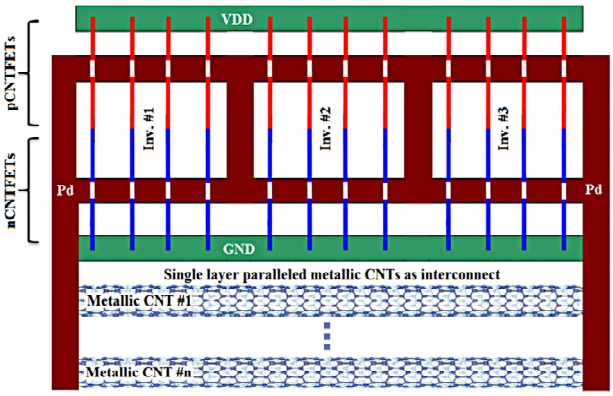

Figure 6. Connecting three inverters in chain in order to benefit from the ballistic transport phenomena in interconnect.

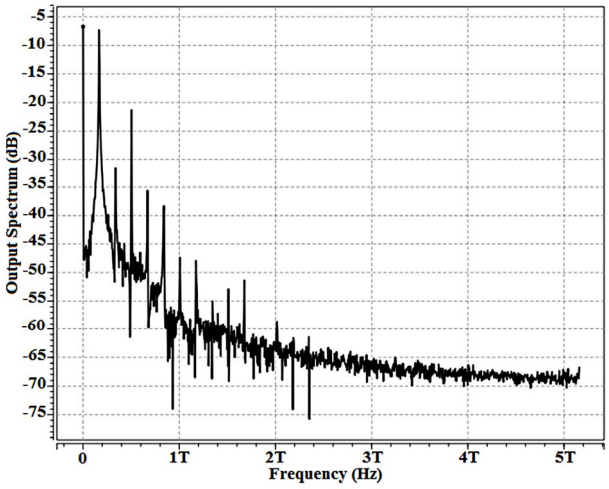

Figure 7. The output spectrum for 32 nm gate length CNTFET-based oscillator, with 5 CNTs under the gate and 7 metallic CNTs in parallel as interconnect.

Table 2. Oscillation frequency, fundamental harmonic amplitude, total harmonic distortion, average power consumption and FOM for different number of CNTs under the gate and different gate lengths (for 7 CNTs in parallel as interconnect).

Gate Length (nanometer)	Number of CNTs under the Gate	Oscillation Frequency (GHz)	Fundamental Harmonic Amplitude (dB)	THD (%)	Average Power Consumption (μW)	FOM
32	1	181.34	−7.20	6.55	10.04	1.202
32	2	186.38	−8.01	4.57	20.36	0.790
32	3	186.38	−6.46	11.39	28.02	0.279
32	4	176.30	−6.29	11.97	35.65	0.199
32	5	166.22	−7.34	3.46	43.73	0.471
32	6	161.19	−7.55	4.10	52.39	0.314
32	7	151.11	−5.59	19.5	59.83	0.067
32	8	141.04	−5.49	20.13	65.51	0.056
25	5	186.37	−6.03	12.96	42.28	0.170
25	6	176.28	−7.67	5.34	50.76	0.268
13	5	161.18	−8.80	7.62	25.14	0.305
13	6	151.10	−8.20	4.98	28.66	0.412

6. Conclusion

In this paper, we have designed and simulated a high performance millimeter wave ring oscillator, based on CNTFET-based inverters. The inverter and ring oscillator designed here have shown promising features versus MOSFET-based ones. The low-power consumption around 40 μ watts, the oscillation frequency of 150 GHz and beyond, the fundamental harmonic amplitude of about −6.5 dB with a good THD, above one order of magnitude improvement in the leakage power and also in the power delay product, and good thermal stability have been obtained. Also, different tradeoffs between several design parameters have been discussed in details. It should be noted that, the scope of this paper is to introduce the novel CNTFET technology and its significant benefits over the conventional MOSFET technology, in order to encourage electrical engineers to have a glance at this new promising technology.

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