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A 0.9 V Supply OTA in 0.18 μm CMOS Technology and Its Application in Realizing a Tunable Low-Pass Gm-C Filter for Wireless Sensor Networks

Soolmaz Abbasalizadeh*, Samad Sheikhaei, Behjat Forouzandeh
School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran
Email: *abasalizadeh89@ut.ac.ir

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ABSTRACT

A low voltage low power operational transconductance amplifier (OTA) based on a bulk driven cell and its application to implement a tunable Gm-C filter is presented. The linearity of the OTA is improved by attenuation and source degeneration techniques. The attenuation technique is implemented by bulk driven cell which is used for low supply voltage circuits. The OTA is designed to operate with a 0.9 V supply voltage and consumes 58.8 μW power. A 600 mV_{ppd} sine wave input signal at 1 MHz frequency shows total harmonic distortion (THD) better than −40 dB over the tuning range of the transconductance. The OTA has been used to realize a tunable Gm-C low-pass filter with gain tuning from 5 dB to 21 dB with 4 dB gain steps, which results in power consumptions of 411.6 to 646.8 μW. This low voltage filter can operate as channel select filter and variable gain amplifier (VGA) for wireless sensor network (WSN) applications. The proposed OTA and filter have been simulated in 0.18 μm CMOS technology. Corner case and temperature simulation results are also included to forecast process and temperature variation affects after fabrication.

Keywords: OTA; Low Voltage; Low Power; Bulk Driven; Gm-C Filter

1. Introduction

Due to the spreading market of portable electronic equipments, low power low voltage circuit design has become an important goal of electronic circuits industry. Many applications, like wireless sensor networks (WSNs), need low supply voltage circuits for proper operation which results in reducing their weight and increasing their battery life time. In wireless sensor networks, the voltage of battery drops over time. Since the nodes in this application cannot be easily accessed in some cases, and they should operate few months or years on a single battery, they must be designed to operate under low supply voltages to overcome voltage drop issues.

Operational transconductor amplifier (OTA) is an important building block of many analog circuits like filters, data converters, etc. This block converts input voltage to output current with a linear transformation factor. Its fast speed and bias based tunability makes this block more appropriate for analog circuits compared with conventional opamps, but it has a linearity limitation drawback. The linearity of the OTA is an important issue because the linearity of the overall system would be determined by this block. This issue becomes very challenging under the low supply voltage and limited power consumption. Also, other specifications of the OTA would be affected by low supply voltage. So, novel circuit design techniques should be considered to improve linearity performances of the OTA and overcome the deterioration of its specifications.

In order to improve linearity of the OTA, many techniques have been reported recently, such as attenuation [1], source degeneration [2-4], nonlinear terms cancellation [5-10], and triode based transconductor [11-13]. In attenuation technique, the linearity improvement is achieved by reducing input voltage. In this technique nonlinear terms of output current is reduced by reducing input voltage. One attenuator that can be used for reduceing input signal is bulk driven transistor. This cell attenuates input signal with γ factor which is the body effect coefficient and has a value between 0.2 and 0.4 [14].

In the bulk driven cell, the input signal is applied to bulk of transistor rather than its gate, and by connecting the gate to an appropriate bias voltage, the channel is formed. Since, the input signal is applied to bulk, it is not necessary to spend a part of the input voltage range to turn the transistor on and this removes the limitation that is produced by threshold voltage requirements of the transistors in low voltage designs. So, this cell can be

*Corresponding author.

used in low supply voltage circuits. In fact, the bulk driven cell can improve linearity of the OTA while operating with reduced supply voltages. In [15] and [16], two low voltage bulk driven OTAs are reported. However, these low voltage cells have some drawbacks. The bulk driven transconductance is 2 to 5 times smaller than that of the gate driven, based on the technology used. This issue leads to low DC gain, low gain bandwidth (GBW) and high input referred noise. Two transconductance enhancement techniques based on positive feedback are reported in [17] to overcome low transconductance value of the bulk driven transistor.

Source degeneration is another linearity improvement technique which is implemented by adding resistance at the source terminal of the input transistors. This technique increases noise factor of the OTA in trade off with linearity improvement. Tunablity of the source degenerated OTA is also achieved with tuning of the source degenerated resistance.

In nonlinear terms cancellation technique, linearity improvement is achieved by an appropriate sum of the nonlinear terms to cancel out nonlinearity. This technique is more suitable for low supply voltage circuits, because pseudo-differential architecture can be used easier in this technique.

In triode based transconductor, the drain-source voltage of input transistors, which is biased in triode region, is kept constant. As a result, a linear OTA with constant transconductance is achieved and tunability of the transconductance is carried out by changing the drain-source voltage of the triode transistors.

Since using these linearization techniques become very challenging under low supply voltages, some circuit design methods should be considered for low supply voltage designs. One of these methods, which is mentioned before, is the bulk driven cell. Some other low voltage circuit design methods are flipped voltage follower cell (FVF) [18], sub-threshold MOSFET [16], pseudo-differential pairs [19], and floating gate. In these methods some of the OTA's specifications such as linearity, noise, open loop DC gain, and unity gain bandwidth (UGBW) are deteriorated in trade off with reduceing supply voltage. So, appropriate topology and biases should be used for getting more optimized circuits.

In this work, a low voltage low power bulk driven OTA is presented. This low voltage OTA can be used for some applications such as WSNs. The proposed OTA uses attenuation and source degeneration techniques for its linearity improvement. By using bulk driven transistors for input pairs, linearity improvement can be achieved while the OTA can operate with reduced supply voltages. The proposed OTA can operate with a 0.9 V supply voltage in a 0.18 μm CMOS n-well process. In order to overcome some drawbacks of using bulk driven transistors, such as low DC gain, low unity gain bandwidth, and high noise, the transconductance enhancement technique, which is reported in [17], is applied to input pairs. In [17], this technique is applied to the bulk driven transistors, too. But no other linearity improvement technique is applied to input pair for further improving linearity. In the proposed OTA, this technique is applied to source degenerated bulk driven input pair and a self-cascode structure is used for increasing output impedance and so the DC gain. Also, in this work, tuning is added to the OTA for compensating the PVT variations. Tuning of the proposed OTA is achieved by varying the source degenerated resistance, which is implemented by a transistor.

As an application of the proposed low voltage low power OTA, a third-order low-pass Butterworth filter is designed. This low voltage Gm-C filter acts as a channel select filter and variable gain amplifier (VGA) for some wireless sensor network applications, such as those compliant with IEEE 802.15.4 standard, also known as ZigBee. The proposed filter has a gain tuning from 5 dB to 21 dB with 4 dB gain steps.

The rest of this manuscript is organized as follows. In Section 2, the proposed OTA with circuit details is discussed. Gm-C filter design and its gain tuning are described in Section 3. Section 4 shows the simulated performances of the OTA and filter. Some discussion about the circuit simulations are made in Section 5. Finally, the conclusions are drawn in Section 6.

2. Design of the Transconductance

2.1. Design of the Input Stage

In the bulk driven cell, input signal is applied to the bulk of input transistors rather than their gates. The bulk driven MOSFET cell acts similar to a JFET. The channel conductivity is varied by bulk-source voltage and, as a result, the bulk driven transistor can conduct with zero, negative, or slightly positive input voltage, similar to a depletion type device [20]. However, this low voltage cell has some disadvantages. The transconductance of the bulk driven transistor is much smaller than that of the gate driven, and this causes low DC gain, low gain bandwidth, and high input referred noise. Another disadvantage of this cell is that for an n-well process, only PMOS bulk driven MOSFETs are available. In order to use NMOS bulk driven MOSFETs, deep n-well layer is needed to achieve a twin well process. To reduce cost of circuit implementation, we have used bulk driven PMOS transistors, in this paper.

Figure 1 shows the input stage of the proposed bulk driven transconductance, which consists of the bulk driven fully-differential pair and tuning transistor. Bulk driven input transistors implement attenuation technique

for linearity improvement of the OTA, which is appropriate for low voltage circuits. The tuning transistor, which acts as source degenerated resistance, improves linearity of the OTA and vary the transconductance value of the OTA for compensation of PVT variations. Although source degeneration technique, increases noise factor of the OTA, but, in trade off, can reduce third order harmonic distortion. When input transistors operate in strong inversion region, their drain current is expressed as follows:

$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{SG} - |V_{th}|\right)^2 \tag{1}$$

in which, parameters have their usual meanings and the channel length modulation is ignored for simplicity. In the bulk driven transistor, threshold voltage is described by:

$$|V_{th}| = |V_{th0}| + |\gamma|\left[\sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|}\right] \tag{2}$$

in which, φ_F is the surface potential, γ is the body effect coefficient, and V_{th0} is threshold voltage when the bulk-source voltage is zero.

By using Equations (1) and (2), the transconductance value of the input transistors, not considering the source degenerated resistance, is given by:

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{|\gamma|}{2\sqrt{2|\varphi_F| + V_{BS}}} \cdot \sqrt{2\mu_P C_{ox}\frac{W}{L} I_D} \tag{3}$$

By applying source degeneration technique to the input stage, the transconductance value is changed to:

$$g_{mb,sd} = \frac{g_{mb}}{1 + \left(g_{mb} \cdot R\right)} \tag{4}$$

in which, R is the half of the resistance of the source degenerated transistor. From Equation (4), it is obvious that, by varying the value of R, the transconductance tuning can be achieved. Although the source degenerated technique, reduces transcondactance value by $1 + g_{mb}R$ factor, but greatly reduces the third order harmonic distortion term by factor of $(1 + g_{mb}R)^2$. The third order harmonic distortion term of the input transistors can be calculated from Equation (1) to Equation (4), as below.

$$\begin{aligned} HD_{3,\text{saturation}} &= \frac{\partial^3\left(I_{D,sat}\right)}{3!\partial\left(V_{BS}\right)^3} \\ &= -\frac{\mu_P C_{ox} W\left(\gamma^2\sqrt{2|\phi_F|} + |\gamma|\left(V_{SG} - |V_{th0}|\right)\right)}{16L\left(\sqrt{2|\phi_F| + V_{BS}}\right)\left(2|\phi_F| + V_{BS}\right)^2}\frac{1}{\left(1 + g_{mb}R\right)^2} \end{aligned} \tag{5}$$

As can be seen from Equation (5), the third order harmonic distortion term is attenuated by γ and $(1 + g_{mb}R)^2$ factors, which are related to the bulk driven transistors and the source degeneration transistor, respectively.

2.2. Complete Design of the Proposed Transconductance

The complete OTA is demonstrated in **Figure 2** which consists of the transconductance main stage, the common mode feedback circuit (CMFB), and the bias circuit. In this figure, all transistors with the same dimensions are labeled with the same symbols and the tuning transistor is labeled with SD (source degenerated).

In order to overcome the main bulk driven issue (low transconductance value), the transconductance enhancement technique is applied to the input pairs [17]. This technique is implemented by M_1, M_3, M_4, M_5 and M_6. A partial positive feedback which is implemented by M_3, reduces the conductance of the node A and increases $g_{mb,sd}$ by the factor η as below.

$$\eta = \frac{1}{1 - \left(g_{m,M_3}/g_{m,M_4}\right)} \tag{6}$$

Because the overall feedback must remain negative, $g_{m,M4}$ must be larger than $g_{m,M3}$. In fact, by choosing $g_{m,M3}/g_{m,M4}$ close to unity, the circuit is very prone to instability, and linear input voltage range becomes small. So, proper sizing for M_3 and M_4 should be used to achieve a stable circuit. The flipped voltage follower current mirror is used for mirroring current to the output.

At the output stage of the OTA, self-cascode structure, which is accomplished by M_8 and M_9, is used for increasing output impedance. In low voltage circuits, it is not possible to stack transistors for increasing output impedance. Self-cascode structure is one solution, which is used in low voltage circuits to increase output impedance [21]. The self-cascode structure has much larger effective channel length and therefore much lower effecttive output conductance. The transistor M_9 in this structure is in linear region and acts as a resistor. For optimal operation of the structure, the dimension of M_8 should be kept larger than M_9. The self-cascode structure is more

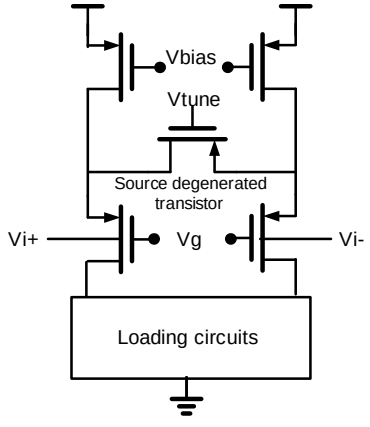


Figure 1. The input stage of the proposed bulk driven transconductance.

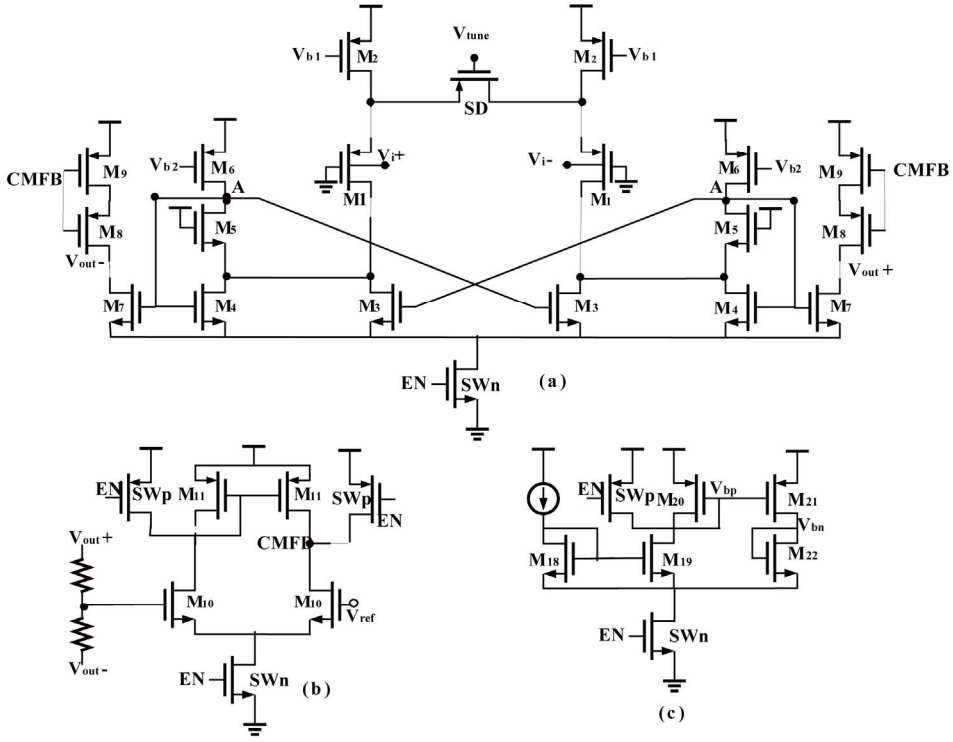


Figure 2. The complete OTA (a) The transconductance main stage; (b) The CMFB circuit; (c) The bias circuit.

suitable for low voltage circuits compared with conventional cascode, as it has high output impedance similar to that of a conventional cascode, while the output voltage requirements of the self-cascode could be similar to a single transistor.

Figure 2(b) shows the CMFB circuit, which sets the dc voltage of the output to V_{ref}. In order to achieve maximum output swing, output common mode is set to VDD/2. In the CMFB circuit, the output voltage of the OTA is averaged by resistance network and is compared with V_{ref}. The resultant signal adjusts the bias of the self-cascode structure and set the output dc voltage around V_{ref}.

The bias circuit which is used to generate the proper bias voltages of the OTA is shown in **Figure 2(c)**. In this figure, the diode connected transistors produce the fixed voltages of V_{bp} and V_{bn} for biasing of PMOS and NMOS transistors, respectively.

In **Figure 2** the transistors SWn and SWp are switches for turning on and off the OTA for gain tuning of the filter (will be described in details in Section 3). When EN is high, the SWp and SWn switches are off and on, respectively. In this mode, the OTA is active and acts normally. For turning of the OTA, EN signal should go low. In this mode, the SWn switches are turned off and thus no current path exists to the ground. On the other hand, the SWp switches turn on and force PMOS biases to VDD. So, PMOS transistors turn off and the OTA becomes disabled.

2.3. Noise in the Proposed OTA

In this section, the noise performance of the proposed OTA is studied. Since, the major part of the voltage gain of the proposed OTA is produced by the output stage, the main part of the input referred noise is generated by the input stage. So, the noise of the output stage can be ignored. The total input referred noise of the overall OTA, which consists of flicker and thermal noise is approximated as: see Equation (7).

In the above equation, K_f is the flicker noise parameter, K is the Boltzmann constant, T is the temperature, f is the

$$\overline{V_{n,in}^2} = \left[2\frac{8KT}{3g_{m\cdot eff}^2}\left(g_{m1} + \left(g_{mb}R/1 + g_{mb}R \right)^2 g_{m2} + g_{m3} + g_{m4} + g_{m6} \right) \right] + \frac{2}{c_{ox}}\frac{1}{f}\left[\left(\frac{k_{fp,sat}}{(WL)_1}\frac{g_{m1}^2}{g_{m\cdot eff}^2} \right) + \left(g_{mb}R/1 + g_{mb}R \right)^2 \left(\frac{k_{fp,sat}}{(WL)_2}\frac{g_{m2}^2}{g_{m\cdot eff}^2} \right) + \left(\frac{k_{fn,sat}}{(WL)_3}\frac{g_{m3}^2}{g_{m\cdot eff}^2} \right) + \left(\frac{k_{fn,sat}}{(WL)_4}\frac{g_{m4}^2}{g_{m\cdot eff}^2} \right) + \left(\frac{k_{fp,sat}}{(WL)_6}\frac{g_{m6}^2}{g_{m\cdot eff}^2} \right) \right] \quad (7)$$

frequency, $g_{m,eff}$ is $\eta^* g_{mb,sd}$ and other parameters have their usual meanings. The factor of 2 is considered for the two halves of the input stage.

Based on Equation (7), although the input referred noise is increased by the noise contribution of M_1 - M_4 and M_6, which is caused by the transconductance enhancement technique, the total input referred noise is reduced. In fact, by using this technique, the DC gain of the OTA enhances. Therefore, the input referred noise of the transistors not involved in this technique is reduced. Based on Equation (7), the total noise can be reduced by minimizing the gate transconductance of all transistors and the current of *M*6.

3. Gm-C Filter Design

The low voltage OTA, which is described in previously, can be used as channel selection filter and variable gain amplifier for the receiver of wireless sensor network applications. IEEE 802.15.4 or ZigBee is one standard which is introduced for wireless sensor networks. This low power standard is deigned for control applications and wireless sensing. It is also appropriate for comercial uses, industrial and home automation, personal health care appliances, and many other applications. In order to satisfy requirements of these articles, the sensors of ZigBee standard should be able to operate for several months on button cells or small batteries [22]. Therefore, the circuits of sensors used in this standard should be low voltage and low power. Considering a zero-IF architecture for the 2.4 GHz ZigBee receiver and assuming some margins in channel selection, a third order Butterworth low-pass filter with more than 2-MHz bandwidth is needed [22]. This filter provides the requirement of 0-dB and 30-dB rejections at the adjacent channel (±5 MHz) and the alternate channel (±10 MHz), respectively [22]. In order to obtain some gain controlling based on the specifications of the receiver, the related filter should be able to operate as a variable gain amplifier, too.

Figure 3 shows the structure of the filter designed for the ZigBee standard. The filter is implemented by cascade of a first-order low-pass stage and a biquad stage for realizing a complex pole pair. This structure, which is reported in [23], is more suitable for low voltage circuits compared with the conventional structure. Because this structure can increase output swing, which is reduced due to low supply voltage. Since, the current delivered to each capacitor of the filter is the same as that of the conventional ones, the new structure does not change the cut off frequency and quality factor of the filter. Due to receiving the signal with the same amplitude and phase in both inputs of the OTA in this structure, the total voltage swing at the inputs of each transconductance is reduced compared with conventional structure and this relieves the need for a high-swing OTA.

Gain tuning of the filter can be obtained based on the fact that by increasing the number of parallel g_m blocks, the transconductance value increases linearly. In fact, by tuning the resistance of the transistor used as degeneration, and by parallelizing the first OTA of each stage in the filter by a similar OTA, gain variation is achieved.

In **Figure 3**, the switches, which are controlled by EN<i> signal, are implemented by transistors. When the cotrolling signal goes high, the related OTA is activated and increases the g_m value and also, gain of the filter. En<1-3> and EN<1-2> refer to the control of three and two OTAs that are placed in parallel, and can be turned

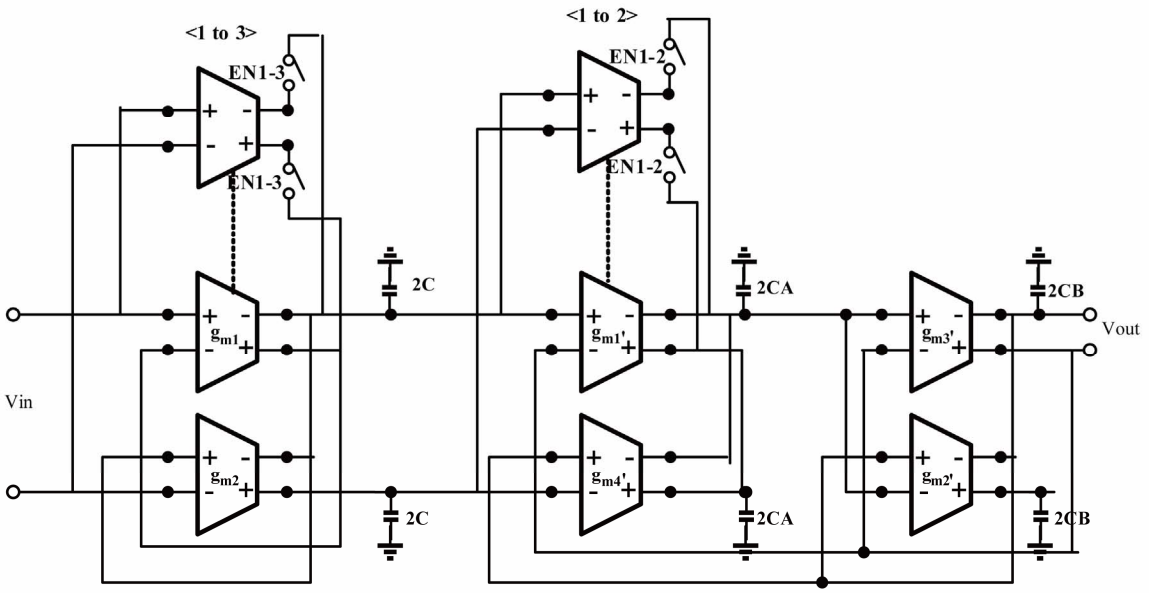


Figure 3. The implementation of the third order low-pass filter.

on and off individually to obtain the required gain value.

The frequency response of the filter is derived as: where,

$$H(S) = \frac{g_{m1}/C}{s+g_{m2}/C}\frac{g'_{m1}g'_{m3}/C_AC_B}{s^2+s\left(g'_{m4}/C_A\right)+g'_{m2}g'_{m3}/C_AC_B} = \frac{k_1}{s+2\pi f_c}\frac{k_2}{s^2+s\left(\omega_0/Q\right)+\omega_0^2} \quad (8)$$

$$\omega_0 = 2\pi f_c\sqrt{\sigma^2+\omega^2}, Q = \frac{\sqrt{\sigma^2+\omega^2}}{2\sigma} \quad (9)$$

in which, σ, ω are the real and imaginary parts of the complex pole, and f_c is the cut off frequency of the filter, k_1 and k_2 are the gain values and other parameters have their usual meanings. Based on Equation (8), it is obvious that by varying the transconductance value of g_{m1} and g'_{m1}, the gain tunability of the filter can be achieved without any variation in the cut off frequency.

4. Simulation Results

4.1. Simulation Results of the OTA

The transconductor and the filter were simulated in a standard 0.18 µm CMOS n-well process with a 0.9 V power supply voltage. The OTA consumes 58.8 µW and 10.6 nW in on and off modes, respectively. The Vtune of the tuning transistor can be varied from 0 to 130 mV to obtain transconductance values of 41.5 µS to 29.7 µS. This 40% tuning can be used for compensating the PVT variations, and also at the same time for tuning the gain of the filter. The tuning of the transconductance value versus differential input voltages is demonstrated in **Figure 4**.

The simulated THD of the OTA is achieved respectively as 55.4 dB, 51.2 dB, and 47.1 dB, by applying 400 mV_{ppd}, 500 mV_{ppd}, and 600 mV_{ppd} differential input signals with 1 MHz frequency. For THD simulations, the Vtune of the tuning transistor is set at 65 mV that is in the middle of the tuning range. Also, simulations show that the THD of the OTA over tuning range of the transconductance, for input amplitude of less than 600 mV_{ppd}, remains below −40 dB.

The input referred noise of the OTA is simulated at 1 MHz frequency and is calculated as 108 nV/√Hz for Vtune of 0 V, which increases to 148.3 nV/√Hz for Vtune of 130 mV. This noise is measured in fully-differential condition, and the large value of it, is due to the bulk driven cell and low supply voltage. In fact, this high noise value can be ignored in trade off with lowering supply voltage and power consumption. The unit of nV/√Hz comes from the dependency of noise to frequency. The noise power density is calculated in voltage squared per hertz, and is called noise power spectral density (PSD) and its rms value is reported in V/√Hz. The common mode rejection ration (CMRR) of the OTA for Vtune of 65 mV is simulated as 139.8 dB, which is measured for a single-ended output. This CMRR will be much higher for differential outputs.

Table 1 contains a summary of the OTA performances. Corner case simulations of the OTA are summarized in **Table 2**. Process and temperature worst case performances of the proposed transconductance are shown in **Table 3**. The temperature of the OTA is varied from −40˚C to 70˚C. As can be seen in these tables, the OTA shows proper operation in process and temperature variations. Performance comparison of the OTA with recently published work are presented in **Table 4**. For better comparison, a figure of merit (FOM) which is defined in [10] is used. In this FOM, shown in Equation (10),

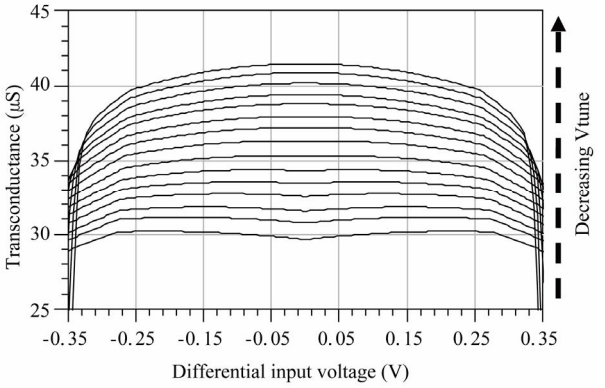


Figure 4. Transconductance tuning versus differential input voltage.

Table 1. Performance summary of the proposed OTA.

Specification	Value
Technology	Standard 0.18 µm CMOS
Power supply	0.9 V
Power consumption (µW)	On mode = 58.8 Off mode = 0.01
THD (dB)	−55.4, −51.2, −47.1*
Input referred noise (nV/√Hz) in tuning range	108 - 148.3@1 MHz
DC gain (dB)**	34.8
Unity gain bandwidth (MHz)**	11
CMRR (dB)**	139.8
PSRR+ (dB)**	82.7
PSRR− (dB)**	47.8

*At 400, 500 and 600 mV_{ppd} input signal, respectively, @1 MHz (Vtune = 65 mV); **Cload = 1 pF and Vtune = 65 mV; Note: CMRR and PSRR values are reported for a single ended output. Differential output values are much higher.

Table 2. Corner case simulations of the OTA.

	TT	SS	SF	FS	FF
Power consumption (μW)	58.8 Off = 0.001	55.9 Off = 0.0006	58.7 Off = 0.0006	58.4 Off = 0.2	60.5 Off = 0.2
THD (dB) (500 mV_{ppd} input signal)*	−51.2	−48.8	−42.8	−49.8	−44.6
Input referred noise (nV/√Hz)*	115	124.6	109.2	123.5	120.9

*@1 MHz, Vtune = 65 mV.

Table 3. Process and temperature worst case performances of the proposed OTA.

	Min	Typical	Max
Power consumption in on mode (μW)	48.8	58.8	65.2
THD (dB) for 500 mV_{ppd} input signal*	−55.7	−51.2	−40.1
Input referred noise (nV/√Hz)*	111.7	115	149.4

*@1 MHz, Vtune = 65 mV.

Table 4. Performance summary of the OTA and comparison with recently published work.

Year	Technology/input structure	Supply voltage (V)	Input voltage range (mV_{ppd})	THD of output current (dB)	Power consumption (W)	Input referred noise (nV/√Hz)	Transconductance value (μS)	FOM	FOM/VDD
2007 [5]	0.18 μm/ Gate driven	1	400	−70@1 MHz	2.5 m	13	1000	87	87
2008 [10]	0.18 μm/ Gate driven	1.5	900	−60 IM3 @40 MHz Or −69.5 THD	9.5 m	23	470	97.2	64.8
2011 [16]	0.18 μm/ Bulk driven	0.5	500	-	60 μ	80@1 MHz	-	-	-
2011 [20]	0.18 μm/ Bulk driven	1	800	−55 @1 MHz	70 μ Vtune = 0.43 V	-	5.6	75.5	75.5
This work	0.18 μm/ Bulk driven	0.9	600	−55.35, −51.2, −47.1*	58.8 μ	115 (Full diff)**	38.8	79.5	88.36

*At 400, 500 and 600 mVppd input signal, respectively (@1 MHz, Vtune = 65 mV); **@1 MHz, Vtune = 65 mV.

transconductance value, linearity performance, speed of the circuit, input swing amplitude, and power consumption are considered.

$$FOM = 10\log\frac{G_m \times V_{id} \times THD \times f_0}{P} \quad (10)$$

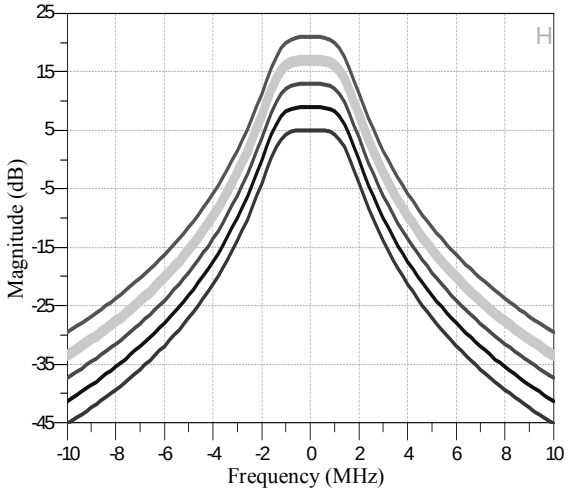
We have also included a new measure, defined as FOM/VDD, in this table to account for the effect supply voltage reduction. As can be seen, by including the effect of supply voltage, it is obvious that the proposed OTA compares well with the others.

4.2. Simulation Results of the Gm-C Filter

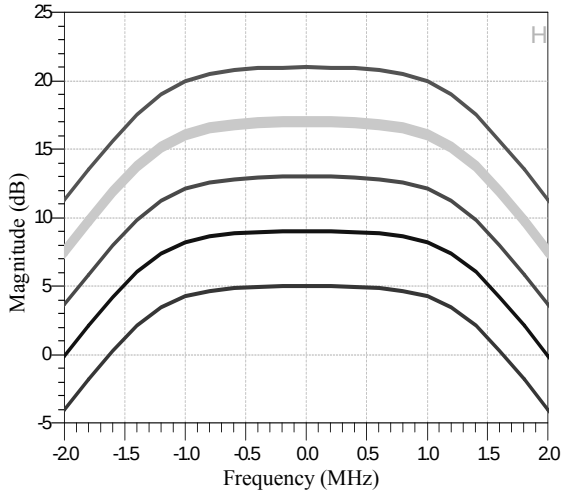
The filter is designed for cut off frequency of more than 1 MHz. This condition guarantees that the filter never removes desired signal power. This consideration is mentioned as the design should be able to compensate the transfer function distortion of the filter (*i.e.*, reduction of the cut off frequency). This distortion comes from truning on the parallel transconductors which leads to reducing output impedance of the related stage.

Figure 5 shows the frequency response of the third order Butterworth low-pass filter over gain tuning of the filter. This filter has gain tuning from 5 dB to 21 dB with 4 dB gain steps. As can be seen in this figure, the cut off frequency of the filter is more than 1 MHz in complete range of the gain tuning. The proposed filter achieves attenuation of 32.1 dB and 50.2 dB at 5 MHz and 10 MHz, respectively for a 5 dB gain of the filter. The proposed filter consumes 411.6 μW to 646.8 μW powers for 5 dB to 21 dB gains of the filter.

The input referred noise of the filter is simulated as 67 nV/√Hz at maximum gain of the filter, which is increased to 167.1 nV/√Hz at minimum gain. This noise value seems good for bulk driven filter with low supply voltage. The simulated in-band IIP_3 of the filter is shown in **Figure 6** which is 10.75 dBm at a 5 dB gain. This IIP_3 value is measured with two input tones of 0.99 MHz and 1.01 MHz. The simulations show that the IIP_3 is reduced to −7 dBm at 21 dB gain of the filter.



(a)



(b)

Figure 5. Frequency response of the third order low-pass filter. (a) Total response; (b) Zoom in on the pass band of the frequency response

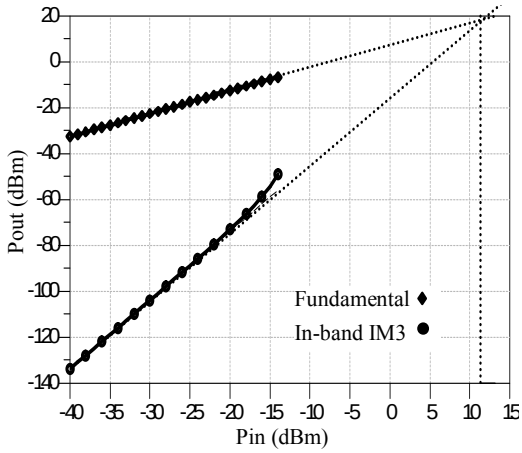


Figure 6. In-band IIP_3 calculation for a 5 dB gain of the filter.

The simulated performances of the filter are listed in **Table 5**. Corner case simulations of the filter are presented in **Table 6**. Corner cases and temperature variations from −40˚C to 70˚C are simulated as well, and show IIP_3 better than 7 dBm, cut off frequency better than 1.2 MHz, attenuation at 5 MHz better than 31 dB and attenuation at 10 MHz better than 49.2 dB, in worst cases, for 5 dB gain of the filter. These values show that the filter operates properly in process and temperature variations. In order to compensate corner case and temperature variations, the Vtune of the tuning transistor is adjusted to obtain appropriate gain of filter and cut off frequency more than 1 MHz. The performance compareson of the filter with recently published work is included in **Table 7**. Performances of the proposed filter are calculated at 5 dB gain of the filter. For better comparison, a figure of merit (FOM) is used as follows [24]:

$$FOM = \frac{\left(\frac{P_C}{N}\right)}{f_c SFDRN^{4/3}},\ SFDR = \left(\frac{IIP_3}{P_N}\right)^{2/3} \qquad (11)$$

in which, P_c is the power consumption of the filter, N is the number of poles and zeros, f_c is the cutoff frequency

Table 5. Performance summary of the proposed filter.

Specification	Value
Technology	0.18 μm CMOS
Power supply	0.9 V
Filter type	3rd order low-pass Butterworth
Cut off frequency (MHz)	More than 1
Gain tuning (dB)	5 to 21
Attenuation (dB)	32.1@5 MHz* 50.2@10 MHz*
Power consumption (μW)	411.6, 646.8**
Differential output swing (V)	0.86*
IIP_3 (dBm)	10.75, −7**
Input referred noise @1 MHz (nV/√ Hz)	67, 167.1**

*At 5 dB gain of the filter; **At 5 dB and 21 dB gain of filter, respectively.

Table 6. Corner case simulation results of the filter (Vtune is adjusted per corner case to obtain gain = 5 dB and fc > 1 MHz).

Performances at 5 dB gain of the filter	TT	SS	SF	FS	FF
IIP_3 (dBm)	10.75	9.5	11.5	11	11.5
Noise figure (dB)	45.2	46	45.7	45.8	45.26
Cut off frequency (MHz)	1.4	1.3	1.3	1.3	1.3
Attenuation (dB) @5 MHz	32.1	34.3	32.7	34.4	32.7
Attenuation(dB) @10 MHz	50.2	52.4	50.8	52.4	50.9

Table 7. Performance summary of the filter and comparison with recently published work.

Year	Technology/ input structure	VDD (V)	Power consumption (W)	IIP_3 (dBm)	Input referred noise (nV/√Hz)	Order of low-pass filter	Cut off frequency (MHz)	FOM (fJ)	FOM* VDD
2011 [24]	90 nm/gate driven	1	4.35 m	21.7 - 22.1	(Diff) 75	6	8.1 - 13.5	0.02*	0.02*
2009 [25]	0.18 µm/gate driven	1.2	4.1 m - 11.1 m	19 - 22.3	12 - 425	3	0.5 - 20	1.54*	1.85*
2011 [16]	0.18 µm/bulk driven	0.5	326 µ	-	171 (@1 MHz)	3	1.4 - 6	-	-
This work	0.18 µm/bulk driven	0.9	411.6 µ**	10.75**	(Diff) 167.1@1 MHz**	3	1	0.41**	0.37**

*Average of FOM, **@5 dB gain.

and the $SFDR.N^{4/3}$ expression is the normalized spurious free dynamic range [24]. For a better comparison of the designs, the average of the FOM is used for filters with cut off frequency tuning. In contrast with the FOM defined for the OTA in Equation (10), the lower FOM in Equation (11) shows a better design. Therefore, for taking effects of supply voltage into account, FOM*VDD is included also in **Table 7**. This table shows that the proposed filter compares favorably with others.

5. Discussion/Analysis

In this paper, a 0.9 V supply transconductance with bulk driven input pairs is represented. A range of 40% tuning of the transconductance value is achieved by varying the source degeneration resistance, which is also used for further improving linearity. This tuning can be used for compensating PVT variations and achieving gain tuning for a third order Butterworth low-pass filter. Further gain tuning of the filter is achieved by parallelizing of transconductor blocks. Using these two methods the gain of the filter can be tuned from 5 dB to 21 dB.

The OTA and filter are simulated in a standard 0.18 µm CMOS technology. The OTA consumes 58.8 µW and filter consumes 411.6 µW to 646.8 µW powers for 5 dB to 21 dB gains. The OTA shows input reffered noise of 108 nV/√Hz to 148.3 nV/√Hz over tuning range of the transconductance value, which is due to the resistance variation of the tuning transistor. The filter shows 167.1 nV/√Hz input reffered noise and 10.75 dBm *IIP*3 at 5 dB gain, too. Process corners and temperature variations from −40˚C to 70˚C are also studied in the paper to forecast the operation of the OTA and filter after fabrication. The simulations show good stability in all process corners and temperatures.

6. Conclusions

A low supply transconductance with bulk driven input pair is proposed in this work. Linearity improvement of the OTA is done by attenuation and source degeneration techniques. Attenuation is implemented by a bulk driven cell, which is used to overcome the threshold voltage limitations of the transistor in low supply voltage circuits. A transconductance enhancement technique is applied to the input pairs of the transconductor to ovecome some drawbacks of the bulk diven cell, including low transconductance value, low DC gain, and high noise. The high noise drawback of the bulk driven cell could be further reduced by some noise cancellation technique. A self cascode structure is also applied to the output stage of the transconductor for further enhancing the DC gain.

As an application of the proposed low voltage OTA, a third order low-pass filter is implemented. The gain of the filter can be tuned. This tunable filter can be used as a channel select filter and variable gain amplifier for wireless sensor network (WSN) applications. The simulation results prove that the proposed design satisfies the required performance of the ZigBee standard, used for wireless sensor network applications.

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