Circuits and Systems, 2012, 3, 317-324
http://dx.doi.org/10.4236/cs.2012.34045 Published Online October 2012 (http://www.SciRP.org/journal/cs)

An Analytical Approach for Fast Automatic Sizing of Narrow-Band RF CMOS LNAs with a Capacitive Load*

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Received July 19, 2012; revised August 19, 2012; accepted August 26, 2012

ABSTRACT

We introduce a fast automatic sizing algorithm for a single-ended narrow-band CMOS cascode LNA with a capacitive load based on an analytical approach without any optimization procedure. Analytical expressions for principle parameters are derived based on an ac equivalent circuit. Based on the analytical expressions and the power-constrained noise optimization criteria, the automatic sizing algorithm is developed. The algorithm is coded using Matlab, which is shown capable of providing a set of design variable values within seconds. One-time Spectre simulations assuming usage of a commercial 90 nm CMOS process are performed to confirm that the algorithm can provide the aimed first-cut design with a reasonable accuracy for the frequency ranging up to 5 GHz.

Keywords: Automatic Synthesis; Analytical Approach; CMOS LNA; Narrow Band; Cascode

1. Introduction

In the field of RF transceiver design, there is a strong demand to digitalize even RF analog parts to mount a transceiver on a single chip [1,2] to utilize the capability of automatic synthesis in digital circuit design. However, the low noise amplifier (LNA), which is a critical building block in any RF front-end, is not ready for digitalization yet. Many efforts have been done for design automation of LNA beforehand since the design of LNA is a time-consuming task that typically relies heavily on the experience of RF designers. LNA design automation can significantly simplify the design task, and also opens a possibility towards digitalization.

There are two basic methods for LNA design automation: simulation based or equation based. Although the simulation-based methods [3,4] are more accurate, they are time consuming due to optimization procedures. On the other hand, equation-based methods [5-7] are faster, but are dependent on the accuracy of the models used. To overcome the disadvantages in some extent, advanced methods using both of equation-based and simulation-based approaches [8-10] have been also suggested.

The difficulties in design automation of LNA lie in several aspects. It is topology dependent, and the design itself is difficult involving trade-offs among critical figures of merits such as *NF*, power gain, impedance matching, power consumption, linearity, and stability. It is desirable if the first-cut design synthesis can be done automatically and fast with an acceptable accuracy.

A methodology for providing a set of first-cut design variables with a reasonable accuracy for a narrow-band LNA with a resistive load was previously suggested [11].

The purpose of this work is to extend the above methodology to a narrow-band LNA with a capacitive load, which is frequently encountered in front-end design.

In this paper, based on an analytical approach without any optimization procedure, we introduce a speedy automatic sizing algorithm for a single-ended narrow-band cascode LNA adopting inductive source degeneration with a capacitive load. In Section 2, design assumptions are discussed. In Section 3, analytical expressions for principle parameters are derived based on an ac equivalent circuit assuming a capacitive output termination. In Section 4, the developed automatic sizing algorithm is explained. In Section 5, verifications are given to check the accuracy of the automatic sizing results.

2. Design Assumptions

The cascode structure with an inductive source degeneration shown in **Figure 1** is chosen as the objective circuit for automatic sizing.

To avoid any confusion, we show the assumptions made in this work, which are same with those in [11].

1) Narrow-band LC matching networks are used for input and output as shown in **Figure 1**. R_1 is used to provide capability for adjusting power gain. As the output termination, two cases are considered: resistive or capacitive termination.

*This work was supported by 2012 Hongik University Research Fund.

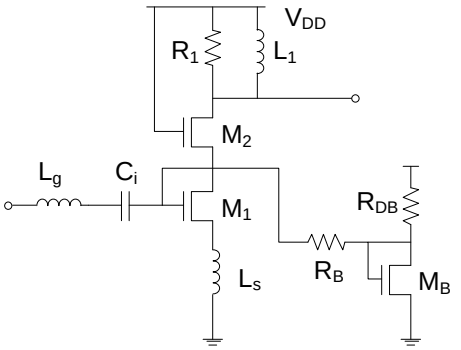


Figure 1. Assumed cascode LNA circuit.

2) For sizing of the MOS transistors M_1 and M_2, the power-constrained noise optimization (PCNO) criteria [12] is adopted to trade off noise performance against power consumption.

3) Ideal inductors and capacitors are used by assuming usage of off-chip components.

4) A current-mirror biasing is adopted as shown in **Figure 1**.

5) The widths of M_1 and M_2 are set as same.

6) The design specifications include operating frequency, input and output terminations, power consumption, power gain, and sufficiently low input and output reflection coefficients S_{11} and S_{22}.

7) The design variables include L_g, L_s, L_1, C_i, R_1, R_{DB}, and R_B including the widths of M_1, M_2, and M_B in **Figure 1**.

3. Derivation of Analytic Expressions for Principal Parameters

3.1. Input Impedance

Figure 2 is the whole ac equivalent circuit for the cascode LNA shown in **Figure 1** including the input signal source and the output capacitive termination C_t. We note that, compared to the complete equivalent circuit of the BSIM4 NMOS transistor in SPICE, only the back-gate transconductance g_{mb} and the gate-body capacitance C_{gb} in the transistor model are ignored to simplify the analysis. The distributed resistances including R_s, R_d, R_g, and R_{sub}, which are included in the BSIM 4 transistor model, are also ignored since they are negligible in large transistors.

In **Figure 2**, g_{m1} and g_{m2} denote the transconductances of M_1 and M_2, respectively. C_{gs}, C_{gd}, and C_{ds} denote the gate-source, gate-drain, and drain-source capacitances of the NMOS transistors, respectively. C_{js} and C_{jd} denote the source-body and drain-body junction capacitances, and C_L is equal to the sum of C_{dg2} and C_{jd2}, which are the capacitances present at the drain node of M_2 in **Figure 1**.

The impedances Z_{in}, Z_{in1}, Z_{in2}, Z_o, Z_{out}, Z_{out1}, and Z_{out2} are self-defined in the circuit. We note that C_{gs}, C_{gd}, and C_{ds} are replaced by C_{sg}, C_{dg}, and C_{sd}, respectively, in some part of our derivations for input and output impedances considering the non-reciprocal nature of gate-oxide capacitances in the BSIM4 MOSFET capacitance model [13].

First, we derive Z_{in} by deriving Z_o, Z_{in2}, and Z_{in1} in order. We note that, we use s and $j\omega$ without differentiation since we are dealing with ac response only.

$Y_o = 1/Z_o$ is simply expressed as

$$Y_o = \frac{1}{sL_1} + sC_t \tag{1}$$

Following the same procedure in deriving $Y_{\text{in2}} = 1/Z_{\text{in2}}$ in [11], we get the same Y_{in2} expression as

$$Y_{\text{in2}} = Y_{\text{in21}} + s\left(C_{sg2} + C_{js2}\right), \tag{2}$$

where $Y_{\text{in21}} = \dfrac{\left(g_{m2} + g_{ds2} + sC_{sd2}\right)}{1 + \left(g_{ds2} + sC_{sd2}\right)Z_p}$

and $Z_p = (1/sC_L)//R_1//Z_o$.

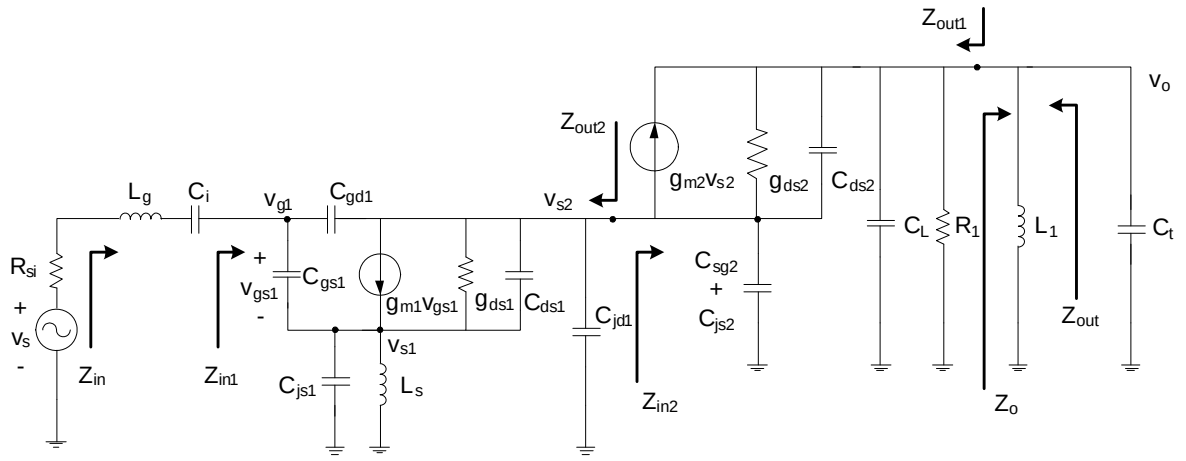


Figure 2. AC equivalent circuit of the cascode LNA in Figure 1.

Following the same procedure in deriving $Y_{in1} = 1/Z_{in1}$ in [11] again, we get the same Y_{in1} expression as

$$Y_{in1} = Y_{in11} + Y_{in12} + Y_{in13}, \quad (3)$$

where $Y_{in11} = \left(sC_{gs1} + sC_{gd1}\right)$,

$$Y_{in12} = \frac{\left[\begin{array}{l}\left(sC_{gs1}+g_{m1}\right)\left(g_{m1}+g_{ds1}+sC_{ds1}\right)\\ +\left(sC_{gd1}-g_{m1}\right)e_1\end{array}\right]\cdot sC_{gd1}}{\left(g_{ds1}+sC_{ds1}\right)\left(g_{m1}+g_{ds1}+sC_{ds1}\right)-e_1e_2},$$

$$Y_{in13} = \frac{\left[\begin{array}{l}\left(sC_{gs1}+g_{m1}\right)e_2+\\ \left(sC_{gd1}-g_{m1}\right)\left(g_{ds1}+sC_{ds1}\right)\end{array}\right]\cdot sC_{gs1}}{\left(g_{ds1}+sC_{ds1}\right)\left(g_{m1}+g_{ds1}+sC_{ds1}\right)-e_1e_2},$$

$$e_1 = \frac{1}{sL_s \,//\, \frac{1}{sC_{js1}}} + sC_{gs1} + g_{m1} + g_{ds1} + sC_{ds1},$$

$$e_2 = \frac{1}{Z_L} + sC_{gd1} + g_{ds1} + sC_{ds1},$$

and $Z_L = (1/(sC_{jd1}))//Z_{in2}$.

Then Z_{in} is expressed as

$$Z_{in} = Z_{in1} + sL_g + \frac{1}{sC_i}. \quad (4)$$

3.2. Output Impedance

Z_{out} derivation can be done similarly as the Z_{in} derivation using the equivalent circuit in **Figure 2** assuming R_{si} input termination. We present the results here, which are same with those presented in [11].

$Y_{out2} = 1/Z_{out2}$ is expressed as

$$Y_{out2} = Y_{out21} + Y_{out22} + Y_{out23} + Y_{out24}, \quad (5)$$

where $Y_{out21} = g_{ds1} + sC_{ds1} + sC_{dg1}$,

$$Y_{out22} = \frac{\left[sC_{sg1}\left(g_{ds1}+sC_{ds1}\right)+sC_{dg1}d_1\right]\cdot\left(g_{m1}-sC_{dg1}\right)}{d_1d_2 - sC_{sg1}\left(sC_{sg1}+g_{m1}\right)},$$

$$Y_{out23} = -\frac{\left[\left(g_{ds1}+sC_{ds1}\right)d_2 + sC_{dg1}\left(sC_{sg1}+g_{m1}\right)\right]\left(g_{m1}+g_{ds1}+sC_{ds1}\right)}{d_1d_2 - sC_{sg1}\left(sC_{sg1}+g_{m1}\right)},$$

$Y_{out24} = sC_{jd1}$,

$$d_1 = \frac{1}{\frac{1}{sC_{js1}} //\, sL_s} + sC_{sg1} + g_{m1} + \left(g_{ds1}+sC_{ds1}\right),$$

$$d_2 = \frac{1}{Z_i} + sC_{dg1} + sC_{sg1},$$

and $Z_i = R_{si} + sL_g + \frac{1}{sC_i}$.

$Y_{out1} = 1/Z_{out1}$ is expressed as

$$Y_{out1} = \frac{1}{Z_2} + sC_L + \frac{1}{R_1}, \quad (6)$$

where $Z_2 = \frac{1}{g_{ds2}+sC_{ds2}} + Z_1\left(1+\frac{g_{m2}}{g_{ds2}+sC_{ds2}}\right)$

and $Z_1 = Z_{out2} \,//\, \frac{1}{s\left(C_{sg2}+C_{js2}\right)}$.

Then Z_{out} is expressed as

$$Z_{out} = Z_{out1} \,//\, sL_1. \quad (7)$$

3.3. Power Gain

To derive the LNA voltage gain, the equivalent circuit in **Figure 2** is simplified into the one shown in **Figure 3**, where the whole circuit is expressed as a 3-stage cascaded amplifier.

Z_{in1}, Z_{in2} and Z_o in **Figure 3** are already derived in (3), (2) and (1), respectively. Notice that A_1v_{g1}, gZ_{out2}, A_2v_{s2}, and gZ_{out1} are the Thevenin equivalent voltages and impedances of the 2nd and 3rd gain stages in **Figure 2**.

The derivation procedures and the expressions are exactly same with those in [11]. Here we show the expressions.

$$gY_{out2} = \frac{1}{gZ_{out2}} = gY_{out21} + s\left(C_{dg1}+C_{jd1}\right) \quad (8)$$

$$A_1 = -\frac{\left(sC_{gs1}+g_{m1}\right)\left(g_{m1}+g_{ds1}+sC_{ds1}\right)+\left(sC_{gd1}-g_{m1}\right)f_1}{\left(g_{ds1}+sC_{ds1}\right)\left(g_{m1}+g_{ds1}+sC_{ds1}\right)-f_1f_2} \quad (9)$$

where $f_1 = \frac{1}{sL_s \,//\, \frac{1}{sC_{js1}}} + sC_{gs1} + g_{m1} + g_{ds1} + sC_{ds1}$

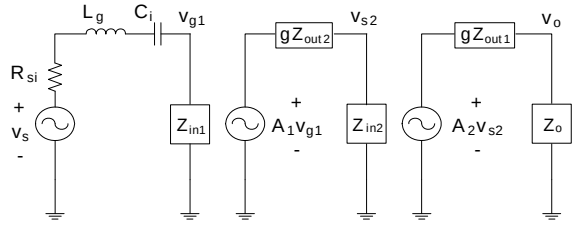


Figure 3. Equivalent circuit to find the voltage gain.

and $f_2 = sC_{jd1} + sC_{gd1} + g_{ds1} + sC_{ds1}$.

$$gZ_{\text{out1}} = g_{ds2} + sC_{ds2} + sC_L + \frac{1}{R_1} \tag{10}$$

$$A_2 \equiv \frac{v_{oo}}{v_{s2}} = \frac{g_{m2} + g_{ds2} + sC_{sd2}}{g_{ds2} + sC_{sd2} + 1 \Big/ \left(\frac{1}{sC_L} // R_1 \right)} \tag{11}$$

In **Figure 2**, the available input power P_i, which is supplied to the LNA when impedance matched, is defined as

$$P_i = \frac{v_s^2}{4R_{si}}. \tag{12}$$

In a capacitive load case, we can derive the available power gain by assuming an additional imaginary load Z_L connected to the v_o node in **Figure 3**. In this situation, the impedence Z_{pp} seen by Z_L is equal to $gZ_{\text{out1}}//Z_o$. When $Z_L = Z_{pp}^*$, the maximum power P_o can be transferred to the load. If we define R_L and R_{pp} are the real parts of Z_L and Z_{pp}, respectively, then P_o can be expressed as

$$P_o = \frac{v_{RL}^2}{R_L} = \frac{v_o^2}{4R_{pp}}. \tag{13}$$

Then the available power gain G is expressed as

$$\begin{aligned} G &= \frac{P_o}{P_i} = \frac{R_{si}}{R_{pp}} \left(\frac{v_o}{v_s} \right)^2 \\ &= \frac{R_{si}}{R_{pp}} \left(\frac{v_{g1}}{v_s} \frac{v_{s2}}{v_{g1}} \frac{v_o}{v_{s2}} \right)^2 \equiv \frac{R_{si}}{R_{pp}} A_{v1}^2 A_{v2}^2 A_{v3}^2, \end{aligned} \tag{14}$$

where A_{v1}, A_{v2}, and A_{v3} can be easily derived from **Figure 3** as follows.

$$A_{v1} \equiv \frac{v_{g1}}{v_s} = Z_{\text{in1}} \Big/ \left(R_{si} + sL_g + \frac{1}{sC_i} + Z_{\text{in1}} \right) \tag{15}$$

$$A_{v2} \equiv \frac{v_{s2}}{v_{g1}} = A_1 Z_{\text{in2}} \Big/ \left(gZ_{\text{out2}} + Z_{\text{in2}} \right) \tag{16}$$

$$A_{v3} = \frac{v_o}{v_{s2}} = A_2 Z_o \Big/ \left(gZ_{\text{out1}} + Z_o \right) \tag{17}$$

4. Automatic Sizing Algorithm

Figure 4 shows the automatic sizing algorithm developed in this work. Here, we explain the procedures from top to bottom.

4.1. 1st Step: Entering Design and Process Specifications

The 1st step in the automatic sizing is to enter the design and process specifications. The design specifications include the operating frequency f, the input output terminations R_{si} and R_{so}, the supply current I_{DD}, the desired power gain Gain_design. Instead of I_{DD}, the power consumption PWR and the supply voltage V_{DD} can be entered to calculate I_{DD} by PWR/V_{DD}. The process specifications include the transistor channel length L, the transistor channel width per finger WF, and the maximum finger number nf_max defined for one unit of transistors.

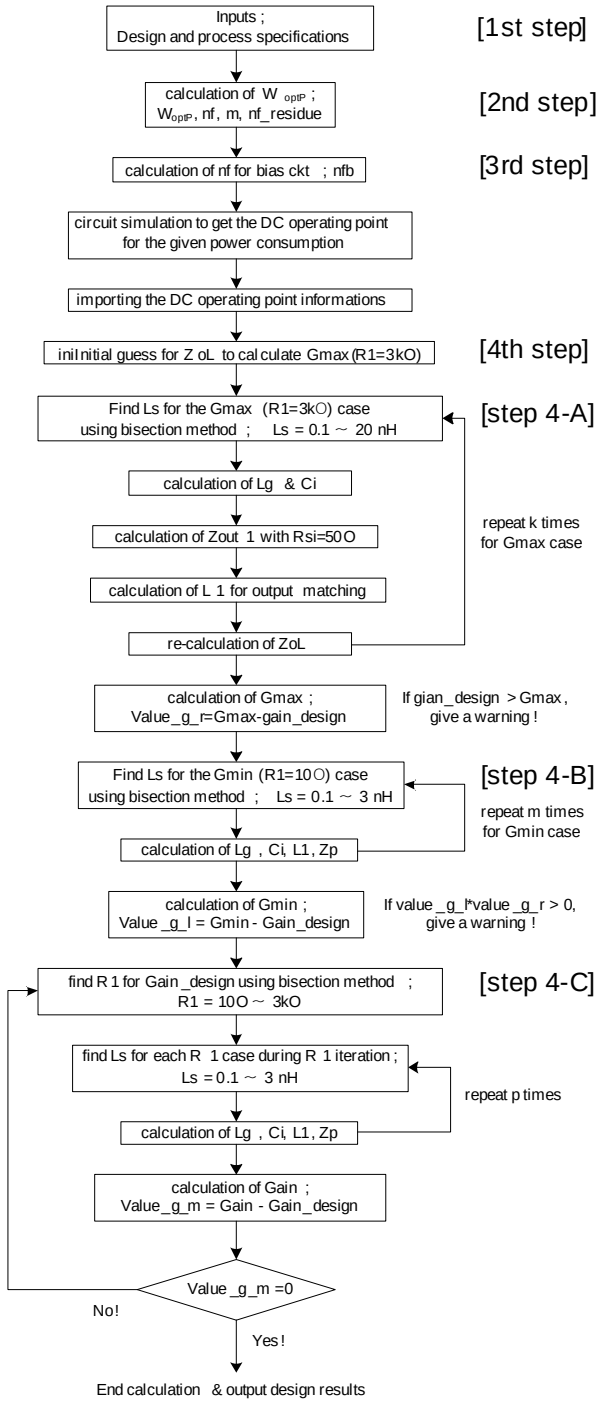


Figure 4. Automatic sizing algorithm.

4.2. 2nd Step: Calculation of Optimum Transistor Width

The next step is to calculate the transistor channel width W for optimum noise performance. The power-constrained noise optimization device width W_{optP} [12] is adopted as W in this work. W_{optP} is calculated according to the last rough equation in (18).

$$W_{optP} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_{si} Q_{sp}} \approx \frac{1}{3\omega L C_{ox} R_{si}} \quad (18)$$

As shown in (18), W_{optP} increases continuously as the frequency decreases. Therefore it may be necessary to define a maximum value for W considering lower frequency design. We suggest to limit W below 1000 μm.

If W_F and nf_max are defined, the finger number nf is first calculated as W/W_F, and the number of the maximum-fingered units m is calculated as the integer value of nf/nf_max, and the residual finger number nf_residue is determined as the residue to give an information for the transistor layout. Then the final W is determined by $W = W_F \times (m \times \text{nf\_max} + \text{nf\_residue})$. We note that W_F and nf_max are usually defined in most of recent processes.

4.3. 3rd Step: Calculation of Bias Circuit Design Variables and Getting DC Operating Point

The next step is to determine the bias circuit variable values and to get the dc operating point information.

The finger number for the bias transistor nfb and the drain bias resistance R_{DB} in **Figure 1** should be determined. By limiting the bias circuit current around 100 μA, for example, we can determine nfb by nfb = (100 μA/I_{DD}) × nf. For the decoupling resistor R_B, we can simply use 5 kΩ, which is a reasonable value.

The next procedure is to determine R_{DB}, which, however, is very difficult to determine by calculation. Since I_{DD} is sensitive to the value of R_{DB}, it should be manually determined to give the specified I_{DD} value by dc circuit simulations. This procedure is one obstacle against full design automation in this work. However, it is an essential procedure since it provides the accurate operating point information to proceed with the remaining part of the design automation. The needed operating point information include the values of g_m, g_{ds}, C_{gs}, C_{sg}, C_{gd}, C_{dg}, C_{ds}, C_{sd}, C_{js}, and C_{jd} of M_1 and M_2 in **Figure 1**, which should be imported into the automatic sizing algorithm.

4.4. 4th Step: Iterations to Determine Design Variable Values

There are three main iteration loops in the automatic sizing algorithm as shown in **Figure 4**. The 1st loop finds G_{max}, which corresponds to the case with the upper limit of R_1, which is chosen arbitrarily large enough as 3 kΩ in this work. We note that this value is smaller than 10 kΩ compared to the 50 Ω resistive load case in [11] since it is easier to get a higher gain in the capacitive load case. To find G_{max}, we need to find all the design variable values for the G_{max} case simultaneously. Iteration is needed since the input and output matching designs affect each other. The 2nd loop finds G_{min}, which corresponds to the case with the lower limit of R_1, which is arbitrarily chosen small as 10 Ω in this work to allow a larger allowable gain range. This iteration is also needed for the same reason explained for the G_{max} case. The 3rd loop finds the proper R_1 value for the desired gain Gain_design by the bisection method, which lies within the lower and upper boundaries G_{min} and G_{max}, and its inner loop finds the corresponding design variable values for the present gain value during iteration similarly as in the 1st and 2nd iteration loops.

A. Iterations to Solve for the G_{max} Case

As explained above, Z_{in1} is affected by output matching design, and Z_{out} is affected by input matching design. Therefore we need some iteration to determine L_s. Since Z_{in2} is affected by Z_o, which is unknown yet, we need an initial guess for Z_o to find the 1st L_s value. As shown in **Figure 4**, an initial guess for $Z_{oL} = Z_o//(1/sC_L)$ is given as $200/g_{m2}$, which is shown to be large enough for all possible situations in the procedure, to solve for Z_{in2} by (2). We note that the initial guess is much larger than that for the resistive load case, which is due to the larger magnitude of the output node impedance.

The impedance seen at the gate of M_1 is equal to Z_{in1}, which is derived in (3). By setting the real part of Z_{in1} $\text{Re}(Z_{in1})$ equal to R_{si} for input impedance matching, we can find L_s. However this equation $\text{Re}(Z_{in1}) = R_{si}$ is too complicated to get the solution directly with the other present design variables values given, and therefore L_s is solicited numerically within the lower and upper boundaries of 0.1 nH and 20 nH. We use the bisection method for this purpose.

The next procedure is to calculate L_g and C_i, which nullify the imaginary part of Z_{in1} $\text{Im}(Z_{in1})$ in **Figure 2**. Z_{in1} is usually capacitive to give a negative value for $\text{Im}(Z_{in1})$, and therefore L_g can be calculated using the equation $\text{Im}(Z_{in1}) - 1/(\omega C_i) + \omega L_g = 0$, where C_i is simply a large dc blocking capacitor. We first calculate L_{g1}, which nullifies $\text{Im}(Z_{in1})$ using $\text{Im}(Z_{in1}) + \omega L_{g1} = 0$. Although C_i is larger the better, considering the layout size, $1/(\omega C_i) = \omega L_{g1}/10$ is used to determine C_i. L_g is then recalculated using $\text{Im}(Z_{in1}) - 1/(\omega C_i) + \omega L_g = 0$.

Depending on to the operating frequency and the desired gain, Z_{in1} may happen to be inductive, or this situation can happen in the middle of the iterations. For this case, a nominal single bond wire inductance of 1 nH is

assumed for L_g and $\mathrm{Im}(Z_{\mathrm{in1}}) - 1/\omega C_i + \omega L_g = 0$ is used to calculate the required C_i value.

In the next procedure, the design variable L_1 should be determined, which gives rise to a maximum gain.

The total admittance YY at the output (v_o) node in **Figure 2** is equal to $Y_{\mathrm{out1}} + 1/(sL_1) + sC_t$. By recognizing a maximum voltage output is obtained at the output resonance condition, the required L_1 value is the one which gives rise to a zero imaginary value of YY. This ends up with the L_1 expression as

$$L_1 = \frac{1}{\omega\left[\mathrm{Im}\left(Y_{\mathrm{out1}}\right) + C_t\right]}. \tag{19}$$

Now the 1st set of the design variable values are ready to update Z_{oL} and the remaining iterations are performed to find the final design variable values for the $G_{\max}$ case. It was found that the iteration number for this loop should be larger than 10.

Right after the iteration loop, A_1, gZ_{out2}, A_2, and gZ_{out1} are calculated using (9), (8), (11), and (10), respectively, and $G_{\max}$ is calculated using (14).

If the $G_{\max}$ value is smaller than the desired gain, the routine gives a warning and stops.

B. Iterations to Solve for the $G_{\min}$ Case

The 2nd loop finds the design variable values for the $G_{\min}$ case. The same iteration as above with the last Z_{oL} value as an initial guess is performed to find $G_{\min}$ using (14) again.

C. Iterations to Solve for the Gain_design Case

The 3rd loop finds the proper R_1 value for the desired gain Gain_design using the bisection method while the inner loop finds the corresponding design variable values for the present gain value. This inner iteration loop is exactly same as the 1st and 2nd loops. After all the design variables are determined for the present gain value, the gain is calculated using (25) again. If the calculated gain is equal to Gain_design within the allowed tolerance, the calculation stops to output the final set of the design variable values, which include W, nf, m, nf_residue, nfb, L_s, L_g, C_i, R_1, and L_1.

5. Verifications

The automatic sizing algorithm explained in Section 4 was coded using Matlab (Version 7.9.0.529) assuming usage of a 90 nm commercial CMOS process. The design variable sets for seven different operating frequencies ranging from 0.5 GHz to 5 GHz were synthesized, and verifications were done by one-time Spectre circuit simulations with the corresponding BSIM4.5.0 MOSFET model [13] for the assumed process.

The process specifications include L = 75 nm, W_F = 3 μm, and nf_max = 64, where 75 nm for L is the effective channel length in this process. The maximum transistor width was set as $W_{\max}$ = nf_max × m × W_F = 64 × 5 × 3 μm = 960 μm, which is below 1000 μm as we suggested.

When the output is terminated by a capacitor, we encounter a difficulty to monitor the output matching and power gain in measurement. Therefore it is customary to connect a dummy source follower output stage for measurement purpose as shown in **Figure 5**. We note that the situation of the output node of M_2 in this case is similar to the one in an LNA connected directly to a mixer in a same chip, which is the capacitive load case we are discussing here. Therefore, for the simulation setup for verification, we also added the source follower to monitor the output matching and power gain as shown in **Figure 5**. The output impedance of the source follower was adjusted to around 50 Ω regardless of the operating frequency, which is same with the assumed value of R_{so}. The dc blocking capacitor at the output was set very large as 1000 pF to eliminate any effect on the circuit in simulations.

To select the design specification value for C_t, we monitored the admittance Y_{11} seen at the input of the source follower in **Figure 5** by circuit simulations, which were done separately but maintaining the same bias point setup and the same output termination as those in the whole circuit simulation. **Table 1** shows the calculated parallel resistance and capacitance values calculated from the simulated Y_{11} values for the frequency range from 0.3 GHz to 5 GHz. From the results in **Table 1**, we concluded that the equivalent circuit of the source follower can be approximated by a simple capacitor of 93 fF since the parallel R_p values are large enough with fortune.

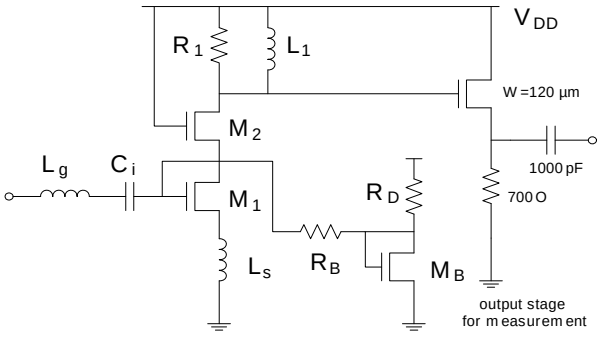


Figure 5. LNA circuit for verification in case of the capacitive output termination.

Table 1. Equivalent parallel R and C values of the source follower stage in Figure 5 as a function of frequency.

f [GHz]	0.3	1	2	3	4	5
C_p [fF]]	92.9	93.2	93.0	92.9	92.8	92.7
R_p [kΩ]	11,400	253	59.8	26.3	14.8	9.4

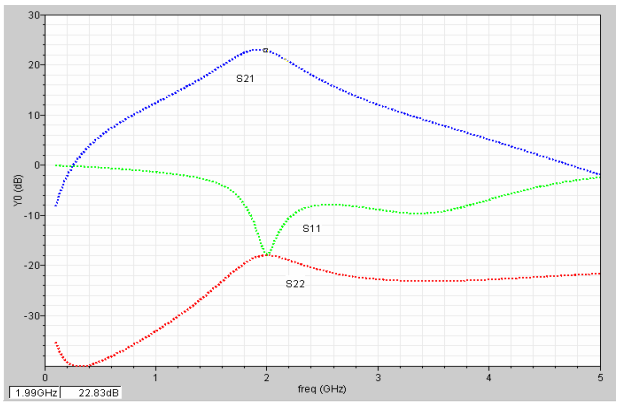
This situation coincides with the design objective we are focusing on here, which is the design of LNA with a capacitive load.

Verifications were done with the same automatic sizing algorithm explained in Section 4.

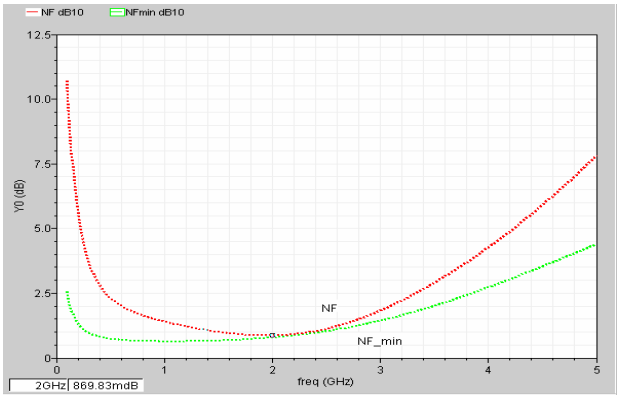
Design specifications include I_D = 5 mA, V_{DD} = 1.2 V, Gain_design = 25 dB, R_{si} = 50 Ω, and C_t = 93 fF. We ignored the loss in the source follower stage to regard S_{21} of the whole circuit as the power gain of the LNA without the source follower. Therefore we can expect the power gain will be slightly larger than the simulated S_{21} values.

We did not include the power consumed in the source follower stage as the total power consumption since it is used only for measurement purpose.

As an example of the verifications, **Figure 6** shows the simulated LNA characteristics without any tuning for the operating frequency of 2 GHz, when the corresponding set of the design variable values obtained using the automatic sizing algorithm are used for the simulation. The synthesized design variable values are R_{DB} = 9.9 kΩ, W = 576 μm (m = 3, nf_residue = 0), nfb = 4, L_s = 1.4693 nH, L_g = 6.868 nH, C_i = 10.14 pF, R_1 = 631.4 Ω, and L_1 = 11.713 nH. As expected with the source follower output stage adopted, S_{22} stays low for the whole frequency range.



(a)



(b)

Figure 6. Simulated (a) *S* parameter and (b) Noise characteristics for f = 2 GHz and Gain_design = 25dB: S_{21} = 22.74 dB, NF = 0.870 dB, NF_{min} = 0.790 dB, S_{11} = −17.8 dB, S_{22} = −18.0 dB.

Table 2 summarizes the simulated results of the designs for for Gain_design of 25dB for the frequency range from 0.5 GHz to 5 GHz.

In **Table 2**, the loss in the source follower seems negligible as desired, which is evident from the result for the 0.8 GHz design. We can see that the input and output matchings are reasonably good in the lower frequencies, but is not good enough in the higher frequencies, especially in the output matching. This may be caused by approximating the equivalent circuit of the source follower by a single capacitor of 93 fF in the syntheses by neglecting the smaller parallel resistance in higher frequencies shown in **Table 1**. If this is the case, we can say this discrepancy is caused by assigning the load improperly, which is not related to the adequacy of the synthesis algorithm. The S_{21} values in **Table 2** are smaller than the desired gain of 25 dB in the higher frequency range. However we believe that the result is pretty good for the first-cut quick design.

Table 3 summarizes the synthesized available gain ranges with the corresponding R_1 values for each design. For the operating frequency below 1 GHz, the synthesized device width is constrained as 960 μm, which is set as maximum, and decreases with frequency as expected.

Table 2. Simulation summary for the desired gain Gain_ design of 25 dB.

f [GHz]	W [μm]	S_{21} [dB]	S_{11} [dB]	S_{22} [dB]	NF [dB]	NF_{min} [dB]
0.5	960	22.6	−19.0	−55.1	1.13	0.564
0.7	960	24.30	−21.1	−35.4	0.792	0.562
0.8	960	24.76	−21.1	−30.5	0.727	0.569
1	960	24.51	−19.6	−24.9	0.698	0.610
2	576	22.74	−17.8	−18.0	0.870	0.790
3	384	22.20	−16.5	−14.2	1.040	0.931
4	291	21.56	−14.9	−11.3	1.160	1.040
5	231	20.96	−13.9	−9.5	1.340	1.180

Table 3. Synthesis summary for the available gain ranges with the corresponding R_1 values.

f [GHz]	W [μm]	S_{21} [dB]	R_1 [Ω]
0.5	960	13.8 - 30.0	10.1 - 735
0.7	960	11.0 - 27.3	10.2 - 632
0.8	960	9.8 - 26.8	10.1 - 734
1	960	8.0 - 28.3	10.2 - 2.72 k
2	576	5.9 - 27.8	10.2 - 1.54 k
3	384	5.2 - 27.7	10.4 - 1.90 k
4	291	4.3 - 27.4	10.4 - 2.17 k
5	231	4.1 - 27.3	10.4 - 2.41 k

6. Conclusions

The analytical expressions for the principle parameters were derived using the ac equivalent circuit of the single-ended narrow-band cascode CMOS LNA with a capacitive load. Based on the expressions, the automatic sizing algorithm was developed by adopting the power-constrained noise optimization criteria. The algorithm was coded using Matlab, and could provide a set of design variable values within seconds. One-time Spectre simulations without any tuning assuming usage of a commercial 90 nm CMOS process were performed to confirm that the automatic sizing program can synthesize the aimed first-cut design with a reasonable accuracy for the frequency range reaching up to 5 GHz.

This work showed in detail how the accurate automatic sizing can be done in an analytical approach. The approach can be applied to a common source LNA more easily since the derivation of principal parameters will be simpler with a fewer gain stages. It can be also applied to a differential LNA easily since the derivation will be basically same.

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