Circuits and Systems, **2012, 3, 187-191**
http://dx.doi.org/10.4236/cs.2012.32025 Published Online April 2012 (http://www.SciRP.org/journal/cs)

An Enhanced Bulk-Driven Folded-Cascode Amplifier in 0.18 µm CMOS Technology

Arash Ahmadpour[1,2], Pooya Torkzadeh[2]
[1]Department of Electronic Engineering, Islamic Azad University, Lahijan Branch, Lahijan, Iran
[2]Department of Electronic Engineering, Islamic Azad University, Science and Research Branch, Tehran, Iran
Email: ar.amp@liau.ac.ir, torkzadeh_oloom@yahoo.com

Received March 4, 2012; revised April 3, 2012; accepted April 10, 2012

ABSTRACT

A new configuration of Bulk-Driven Folded-Cascode (BDFC) amplifier is presented in this paper. Due to this modifying, significant improvement in differential DC-Gain (more than 11 dB) is achieved in compare to the conventional structure. Settling behavior of proposed amplifier is also improved and accuracy more than 8 bit for 500 mV voltage swing is obtained. Simulation results using HSPICE Environment are included which validate the theoretical analysis. The amplifier is designed using standard 0.18 µm CMOS triple-well (level 49) process with supply voltage of 1.2 V. The correct functionality of this configuration is verified from –50˚C to 100˚C.

Keywords: Bulk-Driven Folded-Cascode (BDFC) Amplifier; DC-Gain; Bulk-Driven (BD); Folded-Cascode (FC); CMOS

1. Introduction

Design of high-performance integrated circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages, especially in analog part. This requires traditional analog circuit solutions to be replaced by new approaches to get the best performance and more flexible mixed-mode structure strategies that are compatible with future standard CMOS technology trends. This combination of the analog and digital parts should be done in an optimal way and the optimization process is application dependent [1-4]. The main bottleneck in analog circuits is the operational amplifier. Meanwhile, fully differential amplifiers have better performance compared to the single ended amplifiers. The single-stage amplifiers are inherently less prone to instability; most applications use the amplifier in a closed-loop feedback configuration which can result in instability. This possible instability is likely to manifest under high frequency operation. However, single-stage amplifiers suffer of lower voltage gain compare to the multi-stage amplifiers, especially in low-voltage applications and future deep sub-micron technologies. However multi-stage amplifiers introduce more low frequency poles and available compensation techniques limit the amplifier's speed; nevertheless, they consume much more power. On the other hand, achieving high gain/swing performance is hardly possible for single-stage amplifiers [5].

Fully differential folded-cascode (FC) amplifier is being used in many low-voltage and high bandwidth applications and does not suffer from "mirror pole" limitations. This structure is utilized in many cases and exhibits a superior performance because of its special features like potentially high gain, single parasitic pole, wide bandwidth, acceptable limitation of the common mode (CM) voltage range [5-8]. Besides, bulk-driven (BD) amplifiers or complex gain enhancement techniques are other techniques that have been already introduced to boost the voltage gain of amplifiers. Recently, a number of techniques for increase in the gain of BD amplifiers have been reported [9-11]; but for a sufficient gain, most of them utilize multi-stage or gain-boosting structures. This paper presents the design of a modified structure of single-stage BDFC amplifier that has significant performance in comparison with the conventional BDFC amplifier. It is shown that the proposed amplifier has higher DC-Gain, without degrading of the frequency and transient responses, due to the action of the new merge circuit topology. The proposed structure is done in 0.18 µm triple-well CMOS process for switched-capacitor applications. The design procedures of this paper are organized as follows. Section 2 analyses the small signal of conventional and proposed BDFC amplifiers and introduce the bias and common-mode feedback (CMFB) structures. Section 3 presents the simulation results. Finally the conclusion is given in Section 4.

Copyright © 2012 SciRes.

2. Bulk-Driven Amplifier Circuits

2.1. Conventional Bulk-Driven Folded-Cascode Amplifier

A typical PMOS BDFC amplifier in differential mode capable of operating with low supply voltage is depicted in **Figure 1**. Because of high performance and wide applications, the detailed analysis of this structure has been explained in [5,6]. NMOS and PMOS transistors ac currents are derived by:

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + g_{ds} v_{ds} \tag{1}$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + g_{ds} v_{sd} \tag{2}$$

where g_m, g_{mb}, and g_{ds} are gate transconductance, bulk transconductance, and output conductance, respectively. By using Equations (1) and (2) and considering $V_{i-} = -V_{i+}$ and $V_{o-} = -V_{o+}$, the differential DC-Gain of corresponding amplifier is calculated by:

$$A_{v1} = -g_{mb1} \cdot R_{out} = -g_{mb1} \cdot \left(R_{o1} \| R_{o2} \right) \tag{3}$$

$$\begin{aligned} R_{out} &= \left[1 + r_{ds5} \left(g_{m5} + g_{mb5} \right) \left(r_{ds1} \| r_{ds3} \right) \right] \\ &\quad \| \left[r_{ds7} + r_{ds9} \left(1 + r_{ds7} \left(g_{m7} + g_{m7} \right) \right) \right] \\ &\approx \left[g_{m5} r_{ds5} \left(r_{ds1} \| r_{ds3} \right) \right] \| g_{m7} r_{ds7} r_{ds9} \end{aligned} \tag{4}$$

By applying good approximations, the differential DC-Gain of this amplifier is calculated as:

$$A_{v1} \approx -g_{mb1} \times \frac{g_{m5} r_{ds5} \left(r_{ds1} \| r_{ds3} \right) \times g_{m7} r_{ds7} r_{ds9}}{g_{m5} r_{ds5} \left(r_{ds1} \| r_{ds3} \right) + g_{m7} r_{ds7} r_{ds9}} \tag{5}$$

In a typical 0.18 μm CMOS process, a voltage gain about of 39 dB and unity gain bandwidth (UGBW) of approximately 14.5 MHz with phase margin of 89.7˚ for a capacitive load of 1pF is achievable (bias current of branches is 40 μA). To increase the DC-Gain of conventional FC amplifier, a new technique is proposed in Section B.

2.2. Proposed Structure

The To achieve high DC-Gain in amplifier, the bulk terminals of transistors M_5 to M_8 is used in new configuretion, which NMOS and PMOS devices are in opposite phases. These transistors are auxiliary transistors which increases the output resistance, so DC-Gain will boost. **Figure 2** shows the proposed amplifier without bias and CMFB circuits. Using Kirchhoff's Current Law at the node V_{o+}, the KCL Equation becomes:

$$i_{sd1} + i_{ds5} = i_{ds3} \tag{6}$$

therefore, using Equations (1) and (2), result in:

$$-g_{mb1} \cdot v_{i+} = \frac{v_{D1}}{r_{ds1} \| r_{ds3}} + \frac{v_{D9}}{r_{ds9}} \tag{7}$$

considering $i_{ds5} = i_{sd7} = i_{sd9}$ and $V_1 = -V_2$, and also using Equations (1) and (2), result in:

$$\begin{aligned} &\left[r_{ds7} + r_{ds9} + r_{ds7} \cdot r_{ds9} \left(g_{m7} + g_{mb7} \right) \right] \cdot v_{D9} \\ &= g_{mb7} \cdot r_{ds7} \cdot r_{ds9} \cdot v_1 + r_{ds9} \cdot v_{o+} \end{aligned} \tag{8}$$

$$\begin{aligned} &r_{ds9} \cdot \left(1 + r_{ds5} \left(g_{m5} + g_{mb5} \right) \right) \cdot v_{D1} - r_{ds5} \cdot v_{D9} \\ &= g_{mb5} \cdot r_{ds5} \cdot r_{ds9} \cdot v_1 - r_{ds9} \cdot v_{o+} \end{aligned} \tag{9}$$

$$\begin{aligned} &r_{ds7} \cdot \left(1 + r_{ds5} \left(g_{m5} + g_{mb5} \right) \right) \cdot v_{D1} \\ &+ r_{ds5} \cdot \left(1 + r_{ds7} \left(g_{m7} + g_{mb7} \right) \right) \cdot v_{D9} \\ &= \left(g_{m5} - g_{mb5} \right) \cdot r_{ds5} \cdot r_{ds7} \cdot v_1 + \left(r_{ds5} + r_{ds7} \right) \cdot v_{o+} \end{aligned} \tag{10}$$

using (8) to (10), Equations are obtained as follows:

$$\begin{aligned} &r_{ds7} \cdot r_{ds9} \cdot g_{mb7} \cdot \left(1 + r_{ds5} \left(g_{m5} + g_{mb5} \right) \right) \cdot v_{D1} \\ &= r_{ds5} \cdot \left(1 + r_{ds7} \left(g_{m7} + g_{mb7} \right) \right) \cdot v_{D9} \end{aligned} \tag{11}$$

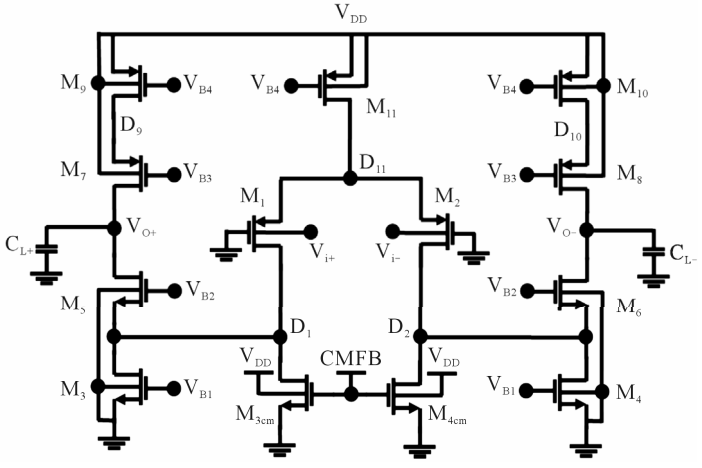

Figure 1. Conventional folded-cascode amplifier.

Copyright © 2012 SciRes.

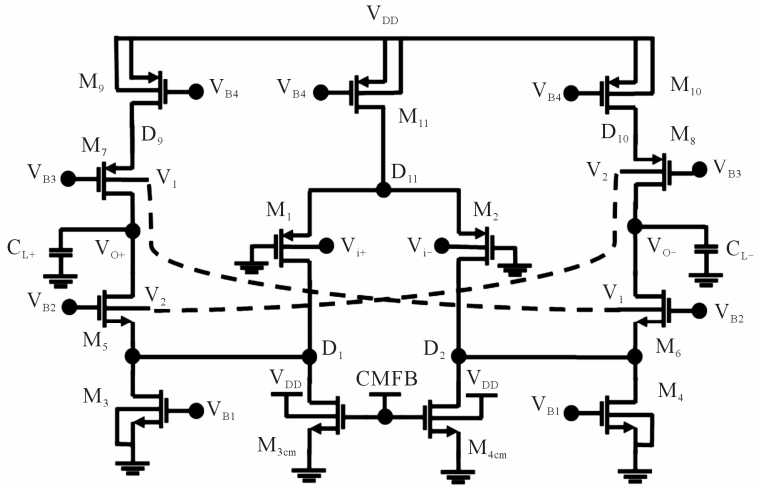

Figure 2. Proposed folded-cascode amplifier.

$$g_{mb7}\cdot r_{ds7}\cdot\left(1+r_{ds5}\left(g_{m5}+g_{mb5}\right)\right)\cdot\left(g_{mb5}\cdot r_{ds9}-1\right)\cdot v_{D1} = \left(g_{mb5}\cdot r_{ds5}+g_{mb7}\cdot r_{ds7}\right)\cdot v_{o+} \quad (12)$$

$$r_{ds5}\cdot\left(1+r_{ds7}\left(g_{m7}+g_{mb7}\right)\right)\cdot\left(g_{mb5}\cdot r_{ds9}-1\right)\cdot v_{D9} = r_{ds9}\cdot\left(g_{mb5}\cdot r_{ds5}+g_{mb7}\cdot r_{ds7}\right)\cdot v_{o+} \quad (13)$$

substituting (11) to (13) into (7) results in:

$$A_{v2} = -K_1\cdot g_{mb1}\cdot R'_{out} = -K_1\cdot g_{mb1}\cdot\left(R'_{o1}\left\|R'_{o2}\right.\right) \quad (14)$$

$$\begin{aligned} R'_{out} &= \left[K_2\cdot\left(r_{ds1}\left\|r_{ds3}\right.\right)\left(1+r_{ds5}\left(g_{m5}+g_{mb5}\right)\right)\right] \\ &\quad\left\|\left[r_{ds5}\left(1+r_{ds7}\left(g_{m7}+g_{m7}\right)\right)\right]\right. \\ &\approx\left[K_2\cdot g_{m5}r_{ds5}\left(r_{ds1}\left\|r_{ds3}\right.\right)\right]\left\|g_{m7}r_{ds5}r_{ds7}\right. \end{aligned} \quad (15)$$

where K_1 and K_2 is

$$\begin{cases} K_1 = \dfrac{\left(g_{mb5}\cdot r_{ds9}-1\right)}{\left(g_{mb5}\cdot r_{ds5}+g_{mb7}\cdot r_{ds7}\right)} > 1 \\ K_2 = g_{mb7}.r_{ds7} \end{cases} \quad (16)$$

rewriting (14), so

$$A_{v2} \approx -g_{mb1}\times\frac{\left(g_{mb5}\cdot r_{ds9}-1\right)}{\left(g_{mb5}\cdot r_{ds5}+g_{mb7}\cdot r_{ds7}\right)} \times\frac{\left[g_{mb7}r_{ds7}\cdot g_{m5}r_{ds5}\left(r_{ds1}\left\|r_{ds3}\right.\right)\right]\times g_{m7}r_{ds5}r_{ds7}}{\left[g_{mb7}r_{ds7}\cdot g_{m5}r_{ds5}\left(r_{ds1}\left\|r_{ds3}\right.\right)\right]+g_{m7}r_{ds5}r_{ds7}} \quad (17)$$

It is clear that with increasing the K_1 and K_2, the output resistance will be boosted. A significant enhancement in the total value of A_{v2} is obtained conesquently. Indeed K_1 will be controlled by choosing appropriate biases and sizes of M_5 to M_8, especially controlling the bulk terminals of V_1 and V_2 of these transistors. However, $g_{mb5}r_{ds9}$ must be greater than 1, because excluding it might take K_1 to zero and decrease the DC-Gain, so before fabrication, the proposed amplifier must be simulated in the corners of fabrication process and wide temperature ranges. In this design procedure, $K_1 = 1.33$ and $K_2 = 9.12$ are obtained, respecttively. Bias circuit and CMFB block which utilized in the conventional and proposed structures is shown in **Figures 3** and **4**, respectively.

3. Simulation Results

In this section, simulation results of the proposed amplifier are shown and are compared with the conventional structure. Amplifiers have been designed in a typical 0.18 μm CMOS process with the same capacitor load and power consumption and then simulated by HSPICE environment using level 49 parameters. A closed-loop configuration with 1 pF capacitors is used to study the linearity and step response of the amplifiers, which is shown in **Figure 5**. With the mentioned value of capacitors, closed-loop gain of the amplifiers is approximately 0 dB.

HSPICE AC simulation results of the proposed and the conventional FC amplifiers are shown in **Figure 6**. The UGBW and phase margin of both structures are approximately equal. As demonstrated in **Figure 6**, the proposed amplifier achieves a DC-Gain about 50 dB which is 11 dB higher than DC-Gain of the conventional amplifier in the same power supply and process. It is considerable that by choosing a greater amount of both K_1 and K_2 in Equation (16) higher DC-Gain can be achieved. Total Harmonic Distortion (THD) of both amplifiers for input CM voltage up to 1.2 Vp-p was tested. For 50 KHz and 1.2 Vp-p input frequency, THD of conventional and proposed structures were –37.97 dB and –42.2 dB, respectively. **Figure 7** shows THD comparison of proposed and conventional amplifiers in different CM voltage swing. As demonstrated of these tests, the conventional FC amplifier achieves higher linearity in lower

Copyright © 2012 SciRes.

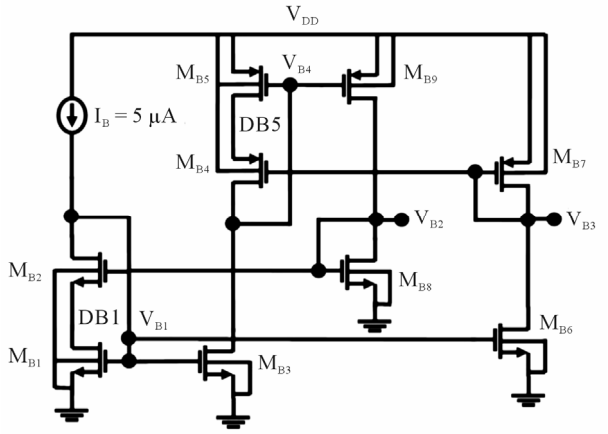

Figure 3. Bias circuit for both amplifiers.

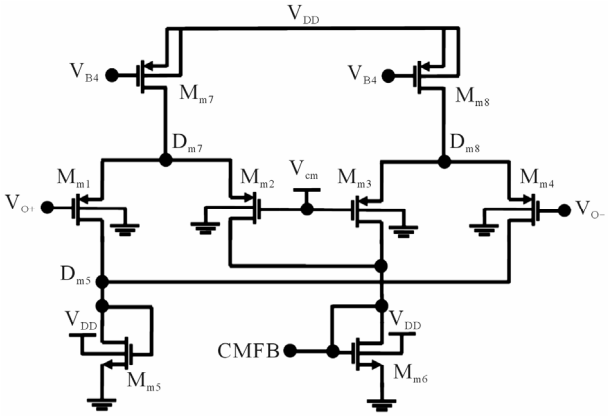

Figure 4. CMFB circuit for both amplifiers.

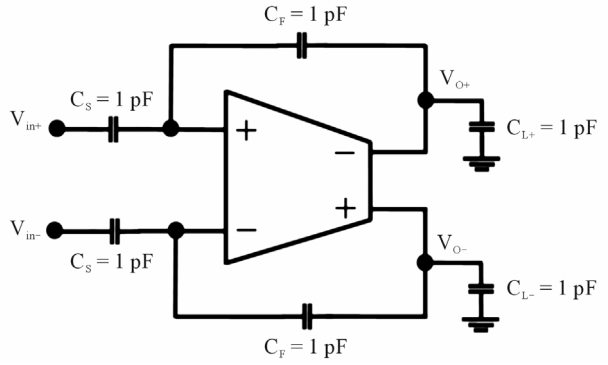

Figure 5. Closed-loop configuration.

output voltage amplitudes. However, in higher output voltage amplitudes, both amplifiers have acceptable linearity and eliminate undesirable harmonics. The accuracy of the amplifiers for different input step voltage amplitudes in unity gain configuration was also tested. The result of the step response simulation for 500 mV amplitude is illustrated in **Figure 8**, which demonstrate that the accuracy of the proposed amplifier is more than 8 bit for up to 500 mV output voltage swing.

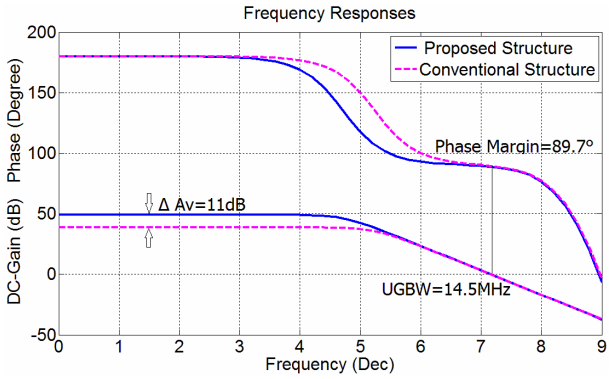

Figure 6. Open-loop frequency response of amplifiers.

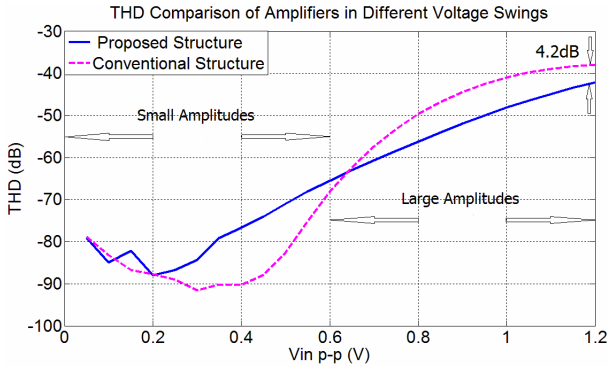

Figure 7. THD comparison of amplifiers in different voltage swing.

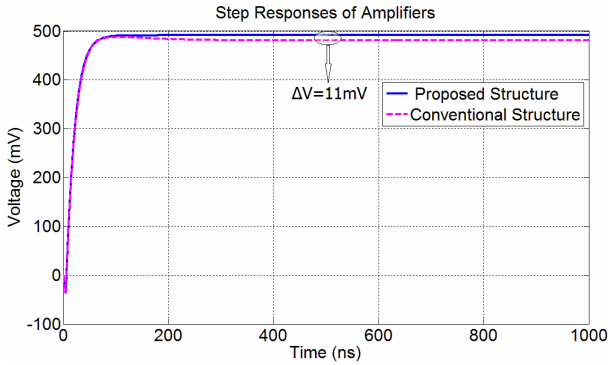

Figure 8. Step response of amplifiers for Vop-p = 500 mV.

Figure 9 illustrates the effective input transconductance of amplifiers as a function of the input CM voltage. It is obvious that both designs function correctly for rail-to-rail input CM voltage values with acceptable variations. Finally, the simulated performance of both amplifiers and its comparison with previous structures are summarized in **Table 1**. In order to compare the relative performance of structures, a new figure of merit (FOM) is used as follows:

$$\mathrm{FOM} = 20\log\left\{\left(\frac{\mathrm{UGBW}\times C_L}{P_{diss}}\right)\times\left(\frac{A_V\times V_{inp\text{-}p}}{THD}\right)\right\} \quad (18)$$

Copyright © 2012 SciRes.

Table 1. Comparisons of characteristics of proposed amplifier with conventional and previous amplifiers.

Parameters	Conventional-BDFC	Proposed-BDFC	[7]	[8]	[9]	[10]	[11]
Technology	0.18 µm	0.18 µm	0.5 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Configuration/ Number of St.	Bulk-Driven Single-Stage	Bulk-Driven Single-Stage	Gate-Driven Single-Stage	Gate-Driven Single-Stage	Bulk-Driven Gain-Boosting	Bulk-Driven Two-Stage	Gate-Driven Single-Stage
V_{DD} (V)	1.2	1.2	3.3	1.8	0.8	0.5	1.2
DC-Gain (dB)	39	50	60	67	68	63	50.9
UGBW (MHz)	14.5	14.5	320	920	8.12	0.57	489.8
Phase-Margin(°)	89.7	89.7	82	67	89	50	77.2
THD (dB)	–37.97 (@1200 mV)	–42.2 (@1200 mV)	–58 (@26 mV)	NA	NA	–57.7 (@500 mV)	NA
Power (µW)	375	375	7500	3900	94	26	661.2
FOM (dB)	170	185	180	NA	NA	226.5	NA

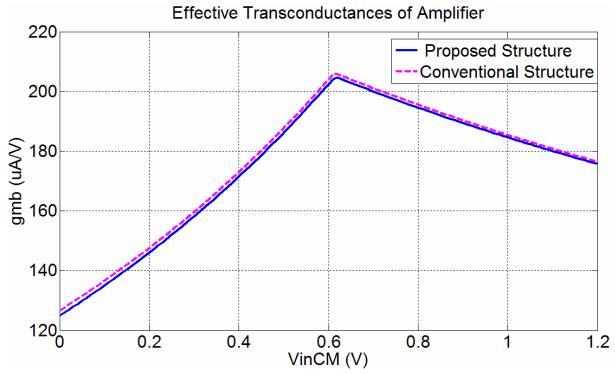

Figure 9. Effective bulk-transconductance of amplifiers from rail-to-rail.

The unit of proposed FOM is $(\text{MHz}\times\text{pF}\times\text{mV})/\text{mW}$, which this form the benchmark for the comparison with the results from this work.

4. Conclusions

In this paper, a novel approach to increase the DC-Gain of conventional BDFC amplifier is presented. With the presented method the DC-Gain of proposed amplifier increased more than 11 dB. All transistors in both amplifiers have same size and both designs consume 375 µW with 1 pF capacitive load.

Accuracy in the closed-loop configuration of amplifier in higher output voltage swings is the main advantage of the proposed structure. Step response simulations demonstrate that the accuracy of the proposed amplifier is more than 8 bit for up to 500 mV output voltages swing. Moreover, THD simulations show that proposed amplifier achieves reasonable linearity in comparison with conventional structure in different voltage swings, especially in large input signal swing.

REFERENCES

[1] S. Chatterjee, Y. Tsvidis and P. Kinget, "Ultra-Low Voltage Analog Integrated Circuits," *IEICE Transactions on Electronics*, Vol. E89-C, No. 6, 2006, pp. 673-680.

[2] S. Yan and E. Sanchez-Sinencio, "Low-Voltage Analog Circuit Design Techniques: A Tutorial," *IEICE Transactions*, Vol. E00-A, No. 2, 2000, pp. 179-196.

[3] J. Ramirez-Angulo, R. G Carvajal and A. Torralba, "Low Supply Voltage High Performance CMOS Current Mirror with Low Input and Output Voltage Requirements," *IEEE Transactions on Circuits and Systems-II Express Briefs*, Vol. 51, No. 3, 2004, pp. 124-129. doi:10.1109/TCSII.2003.822429

[4] ITRS, "The International Technology Roadmap for Semconductors," 2008. http://public.itrs.net

[5] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw Hill, New York, 2001.

[6] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits," 4th Edition, John Wiley & Sons, New York, 2001.

[7] S. M. R. Hasan and N. Ula, "A Novel Feed-Forward Compensation Technique for Single-Stage Fully-Differential CMOS Folded-Cascode Rail-to-Rail Amplifier," *Electrical Engineering*, Vol. 88, No. 6, 2006, pp. 509-517. doi:10.1007/s00202-005-0306-2

[8] B. Alizadeh and A. Dadashi, "An Enhanced Folded-Cascode Op-Amp in 0.18 µm CMOS Process with 67 dB DC-Gain," *IEEE International Conference, Faible Tension Faible Consummation*, 30 May-1 June 2011, pp. 87-90.

[9] J. Rosenfeld, M. Kozak and E. G. Friedman "A Bulk-Driven CMOS OTA with 68-dB DC-Gain," *Proceedings of IEEE International Electronics Circuits Systems*, Tel-Aviv, 13-15 December 2004, pp. 5-8.

[10] M. Trakimas and S. Sonkusale, "A 0.5 V Bulk-Input OTA with Improved Common-Mode Feedback for Low-Frequency Filtering Applications," *Analog Integrated Circuits and Signal Processing*, Vol. 59, No. 1, 2009, pp. 83- 89. doi:10.1007/s10470-008-9236-z

[11] R. Assaad and J. Silva-Martinez, "Enhancing General Performance of Folded-Cascode Amplifier by Recycling Current," *Electronics Letters*, Vol. 43, No. 23, 2007, pp.

Copyright © 2012 SciRes.

1243-1244. doi:10.1049/el:20072031

Copyright © 2012 SciRes.