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A New Approach to Complex Bandpass Sigma Delta Modulator Design for GPS/Galileo Receiver

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ABSTRACT

In this paper, new complex band pass filter architecture for continuous time complex band pass sigma delta modulator is presented. In continuation of paper the modulator is designed for GPS and Galileo receiver. This modulator was simulated in standard 0.18 µm CMOS TSMC technology and has bandwidth of 2 MHz and 4 MHz for GPS and Galileo centered in 4.092 MHz. The dynamic range (DR) is 56.5/49 dB (GPS/Galileo) at sampling rate of 125 MHz. The modulator has power consumption of 4.1 mw with 3 V supply voltage.

Keywords: Continuous Time; Quadrature; Sigma Delta; MOS; Modulator; OTA

1. Introduction

IN recent years, continuous time (CT) sigma delta modulators have attracted increasingly due to low power consumption, low supply voltage, high sampling frequency and high bandwidth in comparison with similar discrete time sigma delta modulators [1-3]. Moreover, because of placing sampler inside loop filter, charge injection effect and nonlinear sampling switched on resistances are significantly suppressed. In addition, the continuous time loop filter attenuating out of band high frequency interferers before sampling act as an anti-alias filter. The CT sigma delta converters have found in such applications as wireless communications systems (zero and low-IF receivers), signal processing, readouts powerless biological signal, in micromachined consumer and professional audio, industrial weight scales and precision measurement devices. Low-IF receivers often use quadrature mixer with complex signals (I/Q) as shown in **Figure 1**. In the conventional low-IF receivers, analog signal convert to digital by use of two lowpass ADCs, the structure of lowpass ADCs in these receivers lead to interference problems that performed by 1/f noise and DC offset. Even, use of the real bandpass ADC structures in low-IF receivers can be problematic for demanding image rejection requirements and low power consumption although the interferences can be fall outside the signal band. Hence, the quadrature sigma delta modulator is state of the art alternative for the complex analog to digital conversion of quadrature signals in low-IF receivers. In the recent years several successful literatures have been presented, that illustrate the new methods in quadrature bandpass sigma delta design [4,5]. This paper proposes novel design architecture in a bandpass quadrature sigma delta modulator with a lower order and a lower frequency sampling, resulting in low power consumption, the prevention of susceptibility to instability and for goal of smaller chip area. The proposed sigma delta is realized by replacing the lowpass loop filter by complex band pass filter in a lowpass sigma delta, which has been implemented in chain of integrators with feed forward summation (CIFF) topology. The lossy integrators of the design have OTA-C structure with improvement in OTA circuit.

2. Basic Principle of Proposed Complex Filter

Single loop sigma delta architecture often use of several topologies for loop filter, such as chain of integrators with weighted feedforward summation (CIFF) [6], and chain of integrators with distributed feedback (CIFB) [7], resulting in stability and realization considered transfer functions. CIFF topology has several benefits in compared to CIFB. In the CIFF topology the swing of output integrators is lower than CIFB. Consequently, it is better

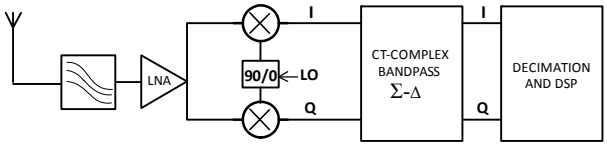

Figure 1. Low-IF receiver structure using complex sigma-delta.

selection for low power, low voltage and wideband modulator implementation. On the other hand, this feature cause to increasing input resistance of integrators, then the unpleasant gain bandwidth effect can be reduced in modulator. Also the CIFF topology have single feedback DAC, which is due to degradation in excess loop delay and clock jitter effects in compared with CIFB. In the proposed design CIFF topology is selected for the complex loop filter architecture of quadrature sigma delta. The transfer function of complex filter is output current to input voltage ratio. So it is transconductance transfer function. For realizing the novel transfer function of complex filter design, one of method is transferring of lowpass filter characteristics from DC to determined center frequency by crass coupling two lowpass filters. So in the first steps we establish the lowpass filter structure. **Figure 2** shows the selected lowpass filter with CIFF topology. At the output node, the summation of output feedforward paths is formed with no extra active component circuit. Use of current summation at output node lead to degradation of power consumption and be rising linearity. In the **Figure 2**, as shown, the output current is collected by summation of transconductance feedforward branches are denoted as gmi (gm1 and gm2). In addition, just as said, the conventional method too shifting transfer function of low pass filter to new center frequency is crass coupling integrators in quadrature paths (I/Q), which is realized the complex filter as shown in **Figure 3**.

Figure 3 is half structure of the proposed complex filter. As exhibited in **Figure 3**, crass coupling branches are implemented by transconductances that are denoted as gci, and the basic duty of them is movement poles to center frequency. Furthermore, for the goal of wideband conversion, zeroes of transfer function must be moved to around of center frequency too. This work can be accomplished by feedforward summation coefficients (gmi). In order to optimization of zeros placement, local feedback transconductances are applied, that are named by gbi in **Figures 2-3**.

3. Implementation

3.1. Operational Transconductance Amplifier (OTA)

Figure 4 shows the optimized OTA from [8]. It can operate in both weak and strong inversion regions and has several benefits, wide common-mode input range, high CMRR and wide linearity limits.

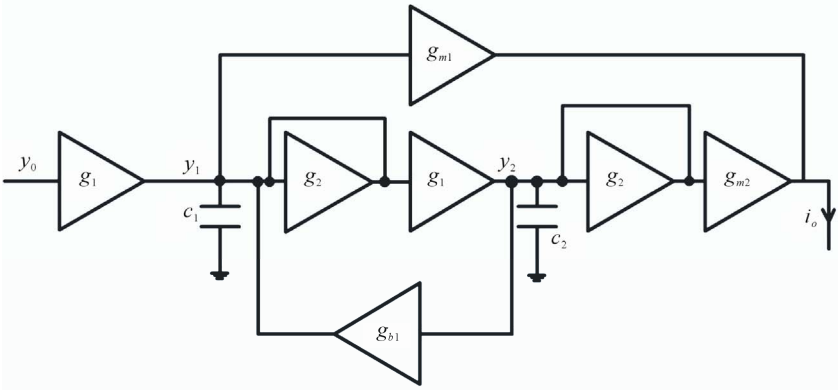

Figure 2. Low-pass filter scheme with CIFF topology.

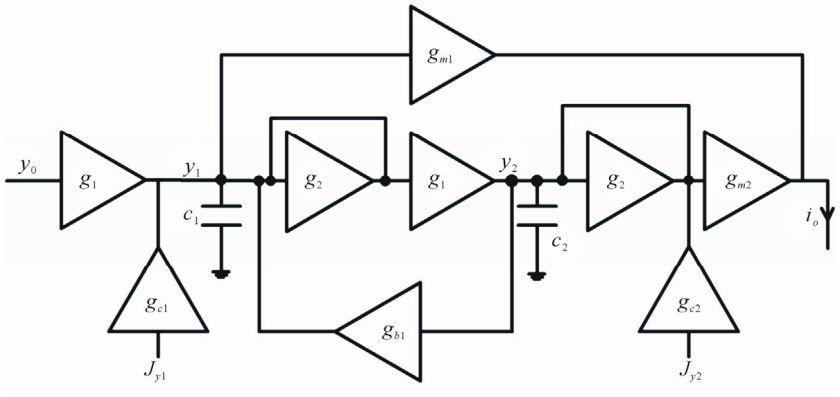

Figure 3. The half structure of the proposed complex filter.

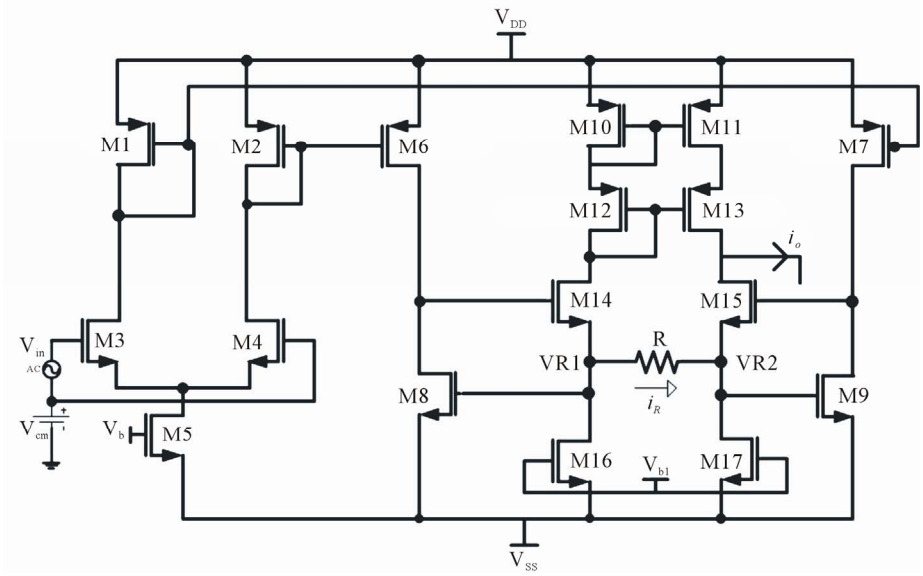

Figure 4. Circuit diagram of the employed OTA.

As shown in **Figure 4**, input common-mode (V_{cm}) and differential signals (V_{in}) can be transfer to sides of resistor (R) by transistors M1-M9 with following equations [8]:

$$VR1 = V_{CM} - V_s + \frac{V_{in}}{2} \tag{1}$$

$$VR2 = V_{CM} - V_s - \frac{V_{in}}{2} \tag{2}$$

where V_s is voltage of source M1 and M2. From (1) and (2), i_R can be obtained by

$$i_R = \left(\frac{1}{R}\right)V_{in} \tag{3}$$

In circuit schematic of OTA in **Figure 4**, M10-M13 are operating as current mirrors. Thus, the output current is given by

$$i_o = 2i_R = \left(\frac{2}{R}\right)V_{in} \tag{4}$$

Above equation indicates the inverse relation between transconductance of OTA and resistor values. Therefore, we can change the transconductor by switching the resistor. This advantage can able us for multi-mode implementation by use of digital calibration logic and external pins.

3.2. Proposed Complex Filter for GPS/Galileo Receivers

The proposed complex sigma delta modulator can be switched between two satellite navigation systems, for GPS and Galileo. In this receivers, the ADC must support a bandwidth of 2/4 MHz (GPS/Galileo) and the minimum signal to noise ratio (SNR) of 42 dB with an OSR = 64/32 (GPS/Galileo). The center frequency must be tuned in f_c = 4.092 MHz. **Figure 5** shows the proposed two order complex filter schematic for the GPS/Galileo modulators, which is useful to low power, low resolution and low data rate. As can be seen in **Figure 5**, the OTA-C lossy integrators are used for degradation in excess loop delay and mismatch loop delay sensitivity [9]. Furthermore the lossy integrators are used for securing of stability. In this figure Y_0 and Q_0 are input voltages of complex filter in the quadrature lines, also i_o and i_Q are output currents of complex filter in the quadrature lines. If $g_{c1} = g_{c2}$, the transfer function is:

$$H_{CF} = \frac{kw_0\sqrt{A}\left(S + \frac{w_0}{Q} - jw_C\right) + Aw_0^2}{\left(S + \frac{w_0}{Q} - jw_C + jw_0\right)\left(S + \frac{w_0}{Q} - jw_C - jw_0\right)} \tag{5}$$

where $w_0 = \frac{\sqrt{g_1 g_{b1}}}{C}$, $w_C = \frac{g_{c1}}{C}$, $Q = \frac{\sqrt{g_1 g_{b1}}}{g_2}$, $A = \frac{g_{m2} g_1}{g_{b1}}$ and $k = \sqrt{\frac{1}{g_{m2}}} g_{m1}$, Parameters of complex filter can be distinguished from the specification the quadrature sigma delta in GPS/Galileo receiver. So the placement of pols of complex filter can be introduced by zeros of the equivalent noise shaping transfer function (NTF). In addition, the crass coupling coefficients can be determined from center frequency of the GPS/Galileo center frequency, and finally the required bandwidth for the GPS/Galileo sigma delta corresponds to bandwidth and order of complex filter. So the imaging of pols can be determined by $w_C \pm w_0 = w_C \pm 0.5 w_B$, this relation results:

$$\frac{\sqrt{g_1 g_{b1}}}{C} = 0.5 w_B \quad (6)$$

The fully proposed circuit of complex filter for GPS/ Galileo bandpass quadrature sigma delta has been shown in **Figure 5**. That is determined the transconductors and capacitances according to **Table 1**.

3.3. Quantizer

Figure 6 shows circuit diagram of the applied quantizer. The quantizer consists of a one bit comparator, followed by a D-latch [9]. Two differential amplifiers with diode loads by transistors M1-M10 are used as pre-amplifier and front-end of comparator. Also cross coupled amplifier as a track-and-latch (by transistors M11-M16) is employed for back-end of clocked regenerative comparator. **Figure 7** shows circuit diagram of D flip-flap that composed by two back-to-back not gate (transistors M1-M4) for memory cell and another not gate for voltage compatibility of the output (transistors M5, M6). In this Figure q and $\overline{q}$ are output nodes.

3.4. Dac

Figure 8 shows the 1 bit D/A converter that employs two voltage sources and two switches, whose voltages are directed via switches that are controlled by the output of the quantizer. When the switch q turns on, the positive reference voltage connects to the output node and when switch q turns off, the negative reference voltage connects to the output node. In this Figure q and $\overline{q}$ are input nodes and $V_{D/C}$ is output node.

4. Simulation Result

The proposed second order complex bandpass sigma-delta modulator circuit was simulated by HSPICE in 0.18 μm CMOS TSMC technology. V_{dd} = 1.5 V, V_{ss} = –1.5 V and V_{ref} = ±0.9 V was chosen. Two sinusoidal quadrature signals with amplitude of 0.5 V_{ref} and frequency of 4 MHz were applied for input of modulator. The sampling frequency was set 125 MHz the oversampling ratios (OSR), are 64/32(GPS/Galileo). The bandwidth is switched for GPS/Galileo by change of transcondutor values in local feedback loop and lossy integrators, as shown in **Table 1**, as well as the bandwidth can be tuned by switchable integrating capacitors and center frequency can be tuned by crass coupling transcondutor values, which can be change by replacing resistor of proposed OTA whit logic switches and external pins. The output data of the modulator were collected, and then 50 kHz fast Fourier transformation (FFT) with hanning window was used to evaluate SNR and power spectral density (PSD). **Figure 9** shows the power spectrum of the GPS modulator and **Figure 10** shows Signal-to-Noise vs. input amplitude for the GPS/Galileo receiver, this figure

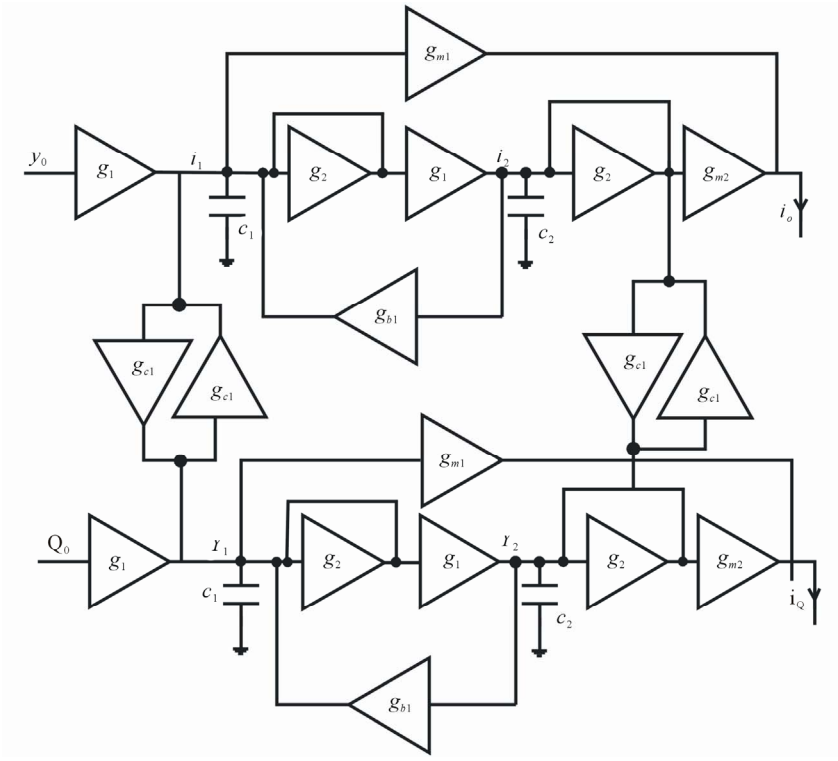

Figure 5. Fully schematic of the proposed complex filter.

Table 1. Component values of the proposed complex filter.

GPS	Galileo
$g_1 = 36$ µ	$g_1 = 72$ µ
$g_2 = 3.5$ u	$g_2 = 7$ u
$g_{m1} = 148$ µ	$g_{m1} = 148$ µ
$g_{m2} = 90$ µ	$g_{m2} = 45$ µ
$g_{b1} = 1.08$ µ	$g_{b1} = 4.32$ µ
$g_{c1} = 51$ µ	$g_{c1} = 51$ µ
$C = 2$ pf	$C = 2$ pf

shows that the maximum SNR (including distortion) for the GPS and Galileo modulators are 52 dB and 47 dB respectively, therefore the bit resolution of proposed modulator is 8.3 bit and 7.5 bit respectively. Furthermore we can determine the dynamic range of modulators from **Figure 10**; these values are 56.5 dB and 49 dB for the GPS and Galileo modulator respectively. Simulation results showed the power consumption of less than 4.1mW. The characteristics of the modulator for the GPS/Galileo are summarized in **Table 2**. Also this design compare with two same recent works too. As seen in the last row of table, the figure of merit was used for comparison of

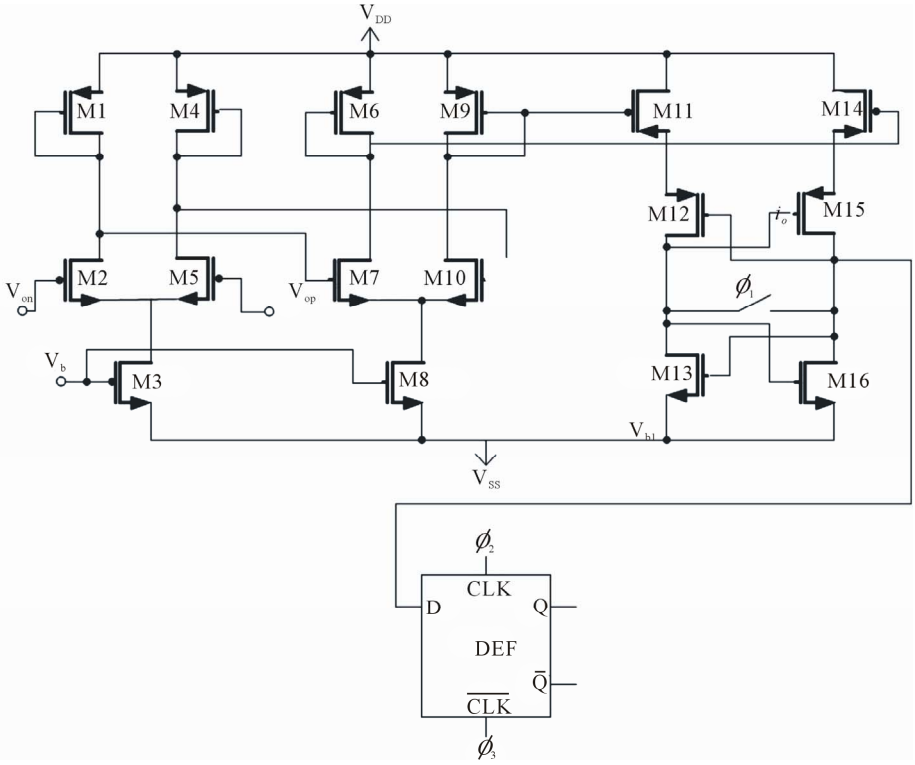

Figure 6. Circuit diagram of the applied quantizer.

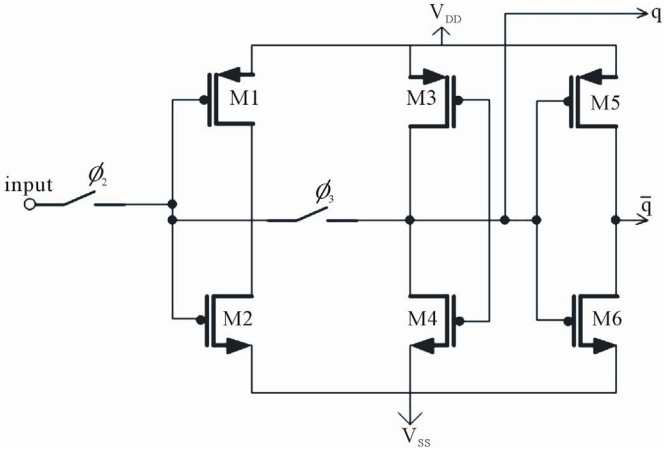

Figure 7. Circuit diagram of D flip-flap.

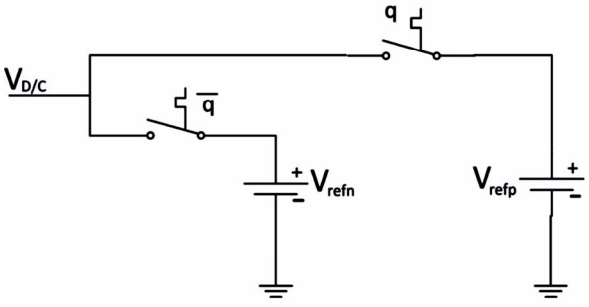

Figure 8. Circuit diagram of the 1bit D/A converter.

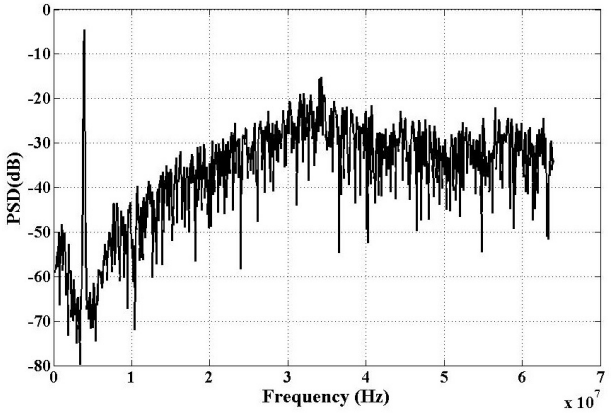

Figure 9. Power spectrum of the modulator.

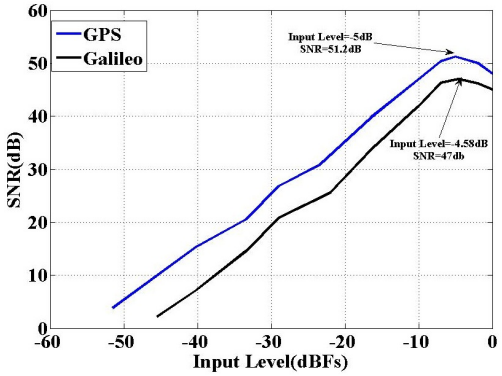

Figure 10. Signal-to-Noise vs. input amplitude of the modulator.

performances that is certifying to preference of this design. This figure of merit is calculated by following formula:

$$FOM = \frac{Power}{2^{\frac{SNDR-1.76}{6.02}} \times 2BW} \quad (7)$$

5. Conclusion

A new continuous time complex bandpass sigma delta modulator for using multi-mode receiver (GPS/Galileo) is presented. The modulator was realized in new structure with CIFF topology and transconductance transfer function. So it was designed for the low power consumption. The proposed complex modulator has 4.1 mw power consumption at ±1.5 supply voltage. It can provide the peak SNR 51.2 dB and 47 dB and a dynamic range of 56.5 dB and 49 dB at Fs = 125 MHz for the GPS and Galileo respectively.

Table 2. Circuit charactristic.

parameter	**Henkel [10]**	**Song-Bok Kim [4]**	**This Design**
Input IF	1 MHz	4.092 MHz	4.092 MHz
Bandwidth	1 MHz	2/4 (GPS/Galileo)	2/4 (GPS/Galileo)
Peak SNR	56.7 dB	52.9/48.4 dB (GPS/Galileo)	51.2/47 dB (GPS/Galileo)
Input DR	63.8 dB	57.5/50.2 dB (GPS/Galileo)	56.5/49 dB (GPS/Galileo)
Input Range	2 V_{p-p}	1.8 V_{p-p}	1.8 V_{p-p}
Power dissipation	21.8 mW	20.5 mW	4.1 mW
Technology	0.65 µm BiCMOS	0.25 µmCMOS	0.18 µm CMOS
FOM	19.5e–12	14.2e–12/11.9e–12 (GPS/Galileo)	3.5e–12/2.8e–12 (GPS/Galileo)

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