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A New CMOS Current Controlled Quadrature Oscillator Based on a MCCII

Ashwek Ben Saied[1,2], Samir Ben Salem[2,3], Dorra Sellami Masmoudi[1,2]
[1]*Computor Imaging and Electronic Systems Group* (*CIEL*), *Research Unit on Intelligent Design and Control of complex Systems* (*ICOS*), *Sfax*, *Tunisia*
[2]*University of Sfax*, *National Engineering School of Sfax* (*ENIS*), *Sfax*, *Tunisia*
[3]*Development Group in Electronics and Communications* (*EleCom*)
Laboratory of Electronics and Information Technology (*LETI*), *Sfax*, *Tunisia*
E-mail: *Achwek.bensaied@gmail.com*, *samir.bensalem@isecs.rnu.tn*, *dorra.masmoudi@enis.rnu.tn*
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Abstract

In this paper, we propose a design of a current controlled Quadrature Sinusoidal Oscillator. The proposed circuit employs three optimized Multi-output translinear second generation current conveyer (MCCII). The oscillation condition and the oscillation frequency are independently controllable. The proposed Quadrature Oscillator frequency can be tuned in the range of [198 - 261 MHz] by a simple variation of a DC current. PSpice simulation results are performed using CMOS 0.35 μm process of AMS.

Keywords: Quadrature Sinusoidal Oscillator, Optimized MCCII

1. Introduction

Controlled Quadrature Sinusoidal Oscillator is a basic signal-generating block frequently needed in communication systems, instrumentation and control systems. In communication it is require for Quadrature mixer and single side band generators.

MCCII based Quadrature oscillator presents a good solution to avoid limitations of Surface Acoustic Wave, such as problems of integration, impedance matching, tuning, linearity, etc.

In order to get controllable characteristics for the proposed Quadrature Qscillator, translinear Multi-output second generation current controlled conveyer based structure seems to be the most attractive [1-3]. In fact, being able to control the output resistance at port X by means of a current source [4-6], one may exploit this in the synthesis of electronically adjustable functions [5-8].

Translinear MCCII family is wathly extended to MOS submicron technologies going towards VLSI design. Indeed, reaching sub-micron technologies, the MOS transistor becomes able to achieve high transit frequencies [1,7,9,11]. These Multi-output conveyors are employed in different RF controllable applications such as oscillators, quadrature oscillator and filters [1,2,7,11].

In this paper, we are interested in the design of MCCII based Quadrature Oscillator. This paper is organized as follows: in section II, we present the MCCII based Quadrature oscillator architecture [1]. Then After presenting the inconvenient of this oscillator, we present the general characteristics of Multi-output second generation translinear current conveyor in section III. In section IV, we give the proposed Controlled Quadrature Oscillator. Finally, the proposed structure is designed and simulated using PSPICE.

2. The Controlled Quadrature Oscillator

Parven Beg [1] presents a novel single resistance controlled sinusoidal quadrature oscillator shown in **Figure 1**. This architecture uses only two CMOS multioutput CCIIs along with the grounded resistors and capacitors.

The corresponding oscillation condition is given by:

$$s^2 + s\left[\frac{1}{R_1} - \frac{1}{R_2}\right]\frac{1}{C_2} + \frac{1}{C_1 C_2 R_2 R_3} = 0 \quad (1)$$

It leads to the following condition

$$R_1 = R_2 \quad (2)$$

and following oscillation frequency:

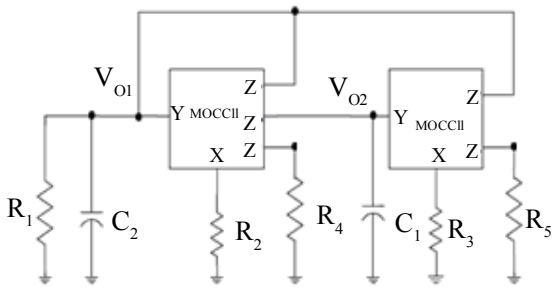

Figure 1. Quadrature oscillator implementation proposed by Parven Beg.

$$f_0 = \frac{1}{2\Pi\sqrt{C_1 C_2 R_3 R_2}} \tag{3}$$

From Equation (3), we get a variable frequency oscillator. The oscillation frequency can be adjusted independently without modification of the oscillation condition by varying R_3 [1]. However, to avoid tuning R_3 after integration, one can change this external resistance by an internal active controllable one corresponding to the X port parasitic resistance of the MCCII.

CMOS Implementation of the MCCII

The MCCII can be represented by the symbol of **Figure 2**. The port relations of the MCCII can be characterized by the following expression:

$$I_Y = 0,\ V_X = V_Y + I_X R_X,\ I_{Zi+} = I_X \quad \text{and} \quad I_{Zi-} = -I_X$$

where, R_X denote the parasitic resistance at the X input terminal of the MCCII and i = 1, 2, 3. The plus and minus sign of the current transfer ratio represent the positive and negative types of the MCCII outputs

The terminal characteristic of the MCCII can be described by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z3+} \\ I_{Z1-} \\ I_{Z2-} \\ I_{Z3-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & -1 & 0 \\ 0 & -1 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{4}$$

The MCCII implementation is given in **Figure 3**. Assuming the same gain factors for both NMOS and PMOS transistors, the parasitic impedances are described by the following expressions (5)

$$Ry = \frac{1}{I_o * (\lambda_N + \lambda_P)} \tag{6}$$

$$Rzi = \frac{1}{I_o * (\lambda_N + \lambda_P)} \qquad (i = 1+, \cdots, 3+ \text{ or } 1-, \cdots, 3-) \tag{7}$$

We notice that the optimization process can be done in the same way for other simulation conditions [7,9,10]. **Table 1** shows the optimal device scaling that we get after applying the optimization approach.

Figure 4 shows the simulated parasitic resistance at port X (R_X) in the optimized configuration. It can be tuned on more than a decade over [427 Ω, 7.1 kΩ] by varying Io in the range [1 µA - 400 µA]. Such control is very important, since it will be used to replace the resistance R_3 in the Quadrature Oscillator giving in **Figure 3**. **Figure 4** depicts results obtained from both PSPICE software simulations (R_X) and MAPLE theoretical calculus of (R_{Xthe}). We Notice a global agreement between both characteristics.

3. Proposed Oscillator

The basic idea in the improved structure consists on replacing the resistance R_3 by the parasitic resistance on port X. We then use this implementation of MCCII, presenting a variable resistance on port X. The Quadrature oscillator, will be in that case controlled by means of the bias current I_o in the MCCII3.

The proposed Quadrature Sinusoidal Oscillator is presented in **Figure 5**. The modified oscillation condition and oscillation frequency are respectively given by the following expressions:

$$R_1 = R_2 \tag{8}$$

$$f_0 = \frac{1}{2\Pi\sqrt{C_1 C_2 R_{X3} R_2}} \tag{9}$$

From Equation (9), we get a variable frequency oscillator. In fact, the oscillation frequency can be adjusted independently without modification of the oscillation condition by varying R_{X3} (by varying I_{o3} current of the MCCII3). The proposed Quadrature oscillator is simulated for different MCCII3 bias currents. Simulation results are shown in **Figure 6**. When varying the control current between 10 µA and 400 µA, the oscillation frequency is tuned in the range [198 MHz - 261MHz].

$$Rx = \frac{1}{\sqrt{I_o} * \left[\sqrt{2K_N \left(\frac{W}{L}\right)_{NXX} (1 + \lambda_N V_{DS})} + \sqrt{2K_P \left(\frac{W}{L}\right)_{PXX} (1 + \lambda_P V_{DS})} \right]} \tag{5}$$

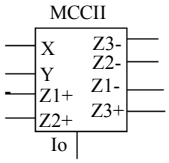

Figure 2. MCCII block.

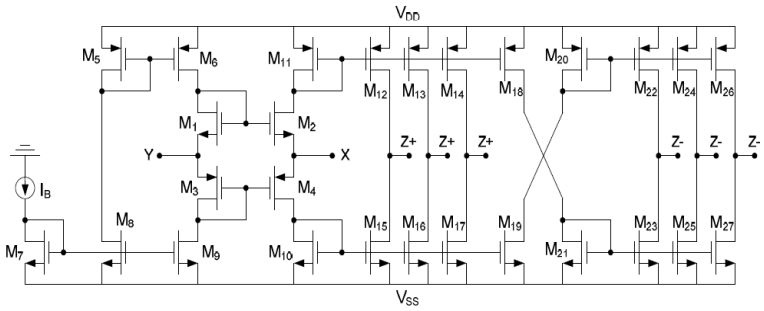

Figure 3. MCCII implementation using translinear loop I_o.

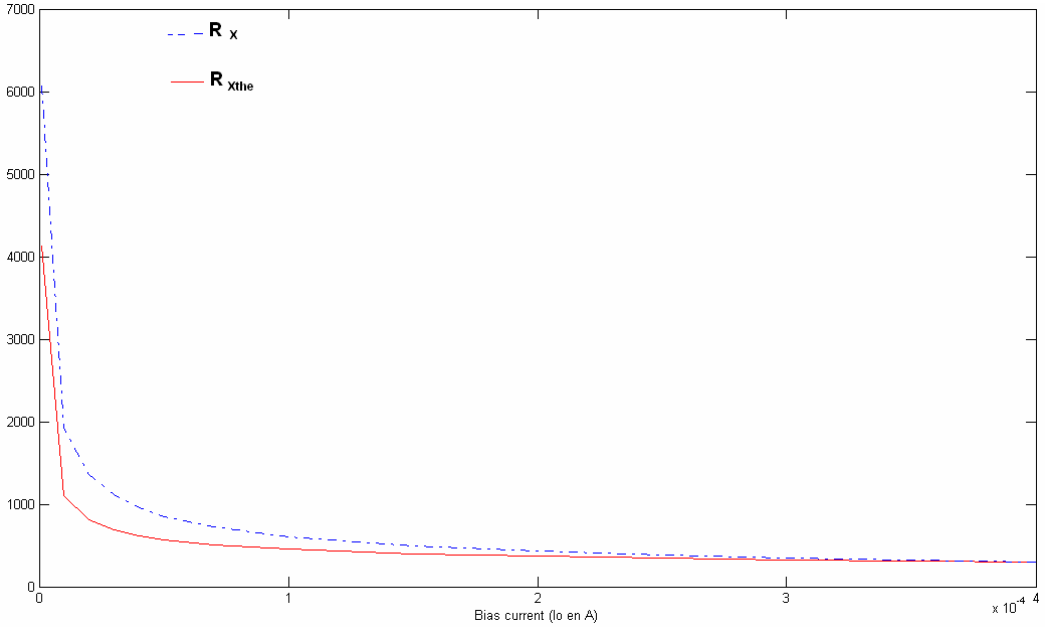

Figure 4. Parasitic resistance at port *X* versus the control current I_o (___R_{xthe}, ---R_X).

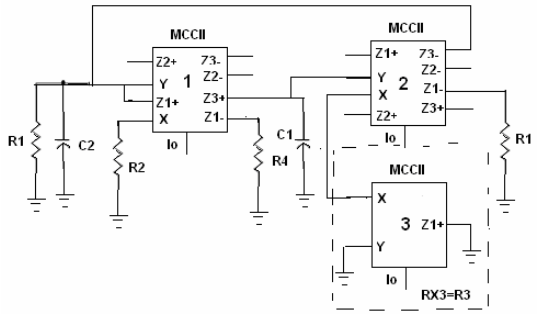

Figure 5. The proposed quadrature oscillator implementation.

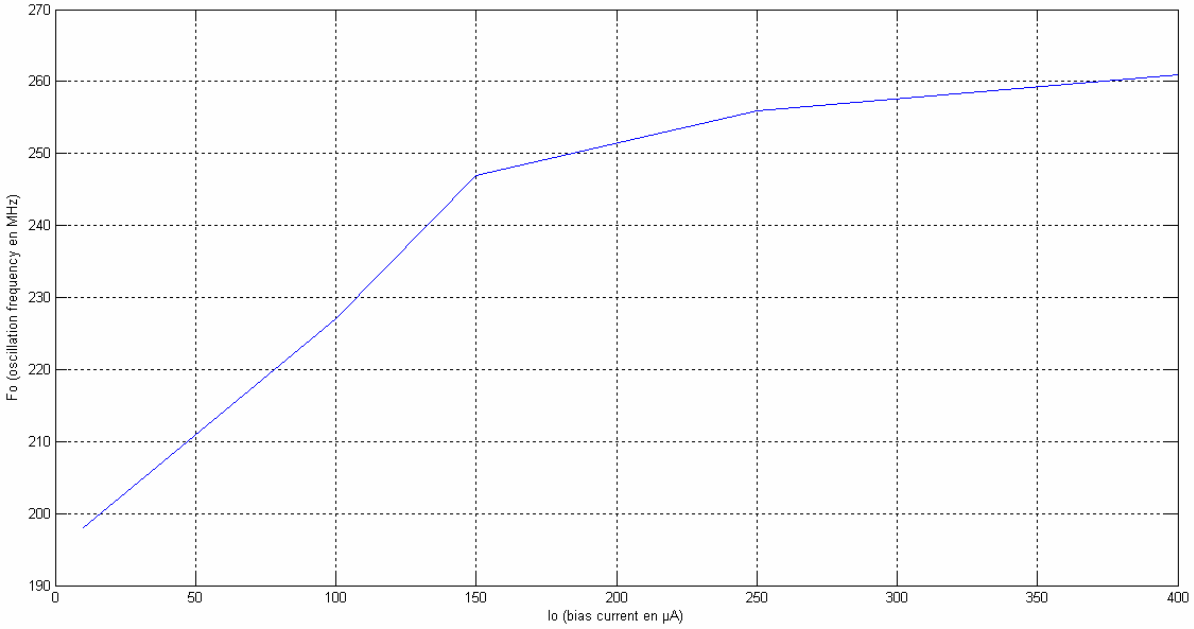

Figure 6. Oscillation frequency versus control current.

Table 1. Device scaling after optimisation process

Device Name	Aspect ratio W/L
M1, M2	12/0.35 (µm)
M3, M4	36/0.35 (µm)
Mxx (in PMOS current mirrors)	18/0.35 (µm)
Mxx (in NMOS current mirrors)	6/0.35 (µm)

The circuit was simulated using $R_1 = R_2 = R_4 = 500\ \Omega$ $R_5 = 1\ \text{K}\Omega$, $R_{X3} = 450\ \Omega$ ($I_{o3} = 100\ \mu\text{A}$), $C_1 = C_2 = 0.2$ pF and $I_{o1} = I_{o2} = 100\ \mu\text{A}$. The obtained oscillation frequency is 225 MHz and the obtained quadrature voltage waveforms are shown in **Figure 7**. Simulations were carried out using 0.35 µm CMOS process parameters.

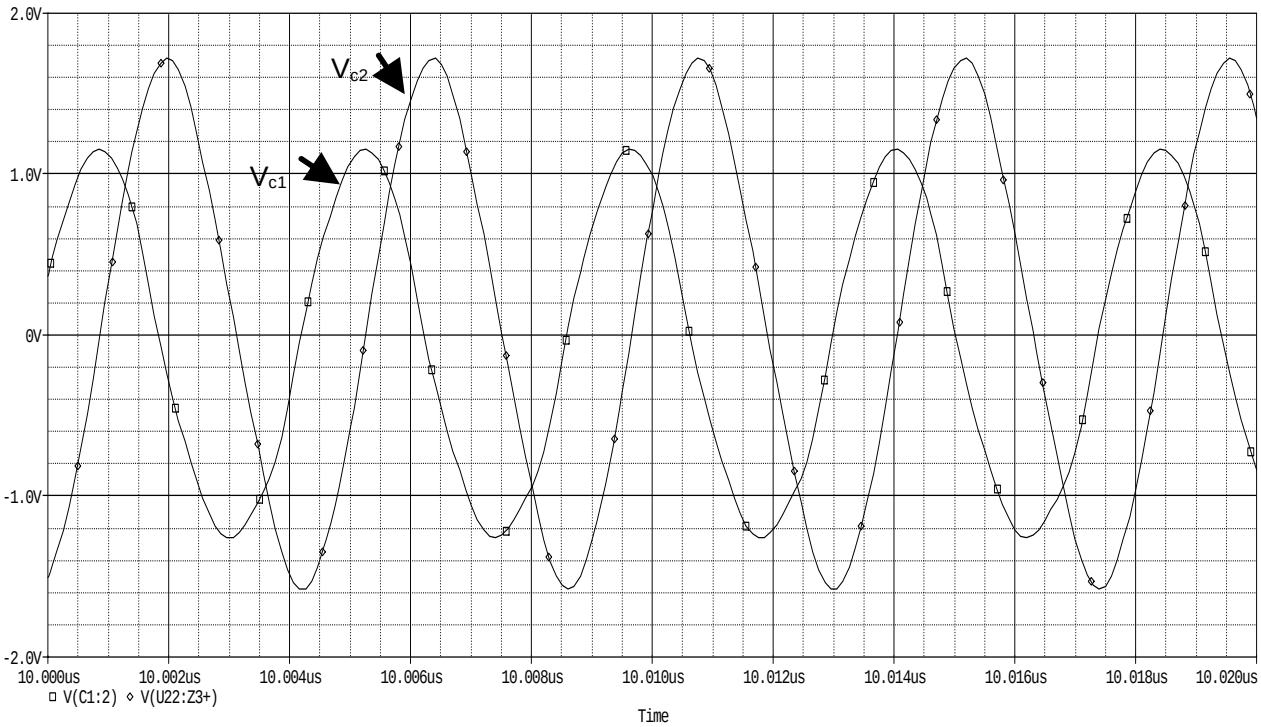

Figure 7. The simulated of Quadrature output waveforms.

4. Conclusions

In this paper, we have proposed a new design of variable frequency current controlled Quadrature oscillators. In order to get high frequency performances of the oscillator, we use an optimized translinear multi-output CCII structure in 0.35 μm CMOS process of AMS. Simulation results show that this Quadrature oscillator provides a control of the oscillation frequency which is independent from the oscillation condition in the range [198 MHz - 261 MHz] by varying the control current in the range [10 μA - 400 μA].

5. References

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