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# Chip Design of a Low-Voltage Wideband Continuous-Time Sigma-Delta Modulator with DWA Technology for WiMAX Applications

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## Abstract

This paper presents the design and experimental results of a continuous-time (CT) sigma-delta ($\Sigma\Delta$) modulator with data-weighted average (DWA) technology for WiMAX applications. The proposed modulator comprises a third-order active RC loop filter, internal quantizer operating at 160 MHz and three DAC circuits. A multi-bit quantizer is used to increase resolution and multi-bit non-return-to-zero (NRZ) DACs are adopted to reduce clock jitter sensitivity. The NRZ DAC circuits with quantizer excess loop delay compensation are set to be half the sampling period of the quantizer for increasing modulator stability. A dynamic element matching (DEM) technique is applied to multi-bit $\Sigma\Delta$ modulators to improve the nonlinearity of the internal DAC. This approach translates the harmonic distortion components of a nonideal DAC in the feedback loop of a $\Sigma\Delta$ modulator to high-frequency components. Capacitor tuning is utilized to overcome loop coefficient shifts due to process variations. The DWA technique is used for reducing DAC noise due to component mismatches. The prototype is implemented in TSMC 0.18 um CMOS process. Experimental results show that the $\Sigma\Delta$ modulator achieves 54-dB dynamic range, 51-dB SNR, and 48-dB SNDR over a 10-MHz signal bandwidth with an oversampling ratio (OSR) of 8, while dissipating 19.8 mW from a 1.2-V supply. Including pads, the chip area is 1.156 mm$^2$.

## 1. Introduction

Sigma-delta modulation techniques have been extended in moderate and high accuracy analog/mixed-signal IC applications, such as analog-to-digital data converters (ADCs), digital-to-analog data converters (DACs), frequency synthesizers, and power amplifiers [1]. Moreover, $\Sigma\Delta$ modulators are widely used in receivers because of their ability to provide high-resolution with relatively low precision components and low power consumption [2,3]. Oversampling $\Sigma\Delta$ ADCs trade digital signal processing complexity for relaxed requirements on the analog components compared to Nyquist-rate ADCs [4]. Due to the over-sampling characteristics, $\Sigma\Delta$ modulators are limited on the application of voice band or lower frequency signals. As the ICs process is improved, recently it makes many researches transfer to wider bandwidth applications gradually, such as GSM, WCDMA, Bluetooth, WiFi, and WiMAX [5]. With the progress of wireless communication, ADCs need higher OSR in order to achieve higher speed and resolution in the system. When OSR is programmable, increasing OSR leads to higher power consumption due to the increased speed requirement for the integrators and comparators in $\Sigma\Delta$ modulators. Due to the requirements of low supply voltage and low power dissipation in the mobile communications, the low order $\Sigma\Delta$ modulators of lower SNR are not suitable for wide bandwidth applications. Therefore, the high order multi-bit $\Sigma\Delta$ modulator circuit is design to increase the SNR.

While most of current commercial $\Sigma\Delta$ ADCs for wireless applications were implemented by using switched capacitor (SC) techniques which are also known as discrete-time (DT) $\Sigma\Delta$ ADCs [6-8], mainly due to mature design methodologies and robustness, more and more continuous-time (CT) $\Sigma\Delta$ ADCs were reported and showed impressive performance. Compared with DT counterparts, the CT $\Sigma\Delta$ ADCs have two main advan-

tages. First, the inherent anti-aliasing characteristics of the CT ΣΔ ADCs reduce the performance requirement of the anti-aliasing filter further and hence reduce the power consumption of the transceiver. Second, the bandwidth requirement of the operational amplifiers (op amps) in CT ΣΔ ADCs is much lower than that of the op amps in DT ones for a given sampling rate, so the CT ΣΔ ADCs are more suitable for broadband applications. Hence we propose a low-voltage, lower power consumption and high resolution CT ΣΔ modulator. Our target is to design a 10 MHz input signal bandwidth and 160MHz sample-rate ΣΔ modulator implemented in TSMC 0.18 μm CMOS process.

This paper begins with a brief summary of the innovative CT ΣΔ circuit design. Section 2 introduces the system architecture of the wideband CT ΣΔ modulator. Section 3 describes the design of building blocks of the modulator, while Section 4 presents the measured results of the prototype. Section 5 summarizes the paper.

## 2. System Circuit Architecture

As high sampling frequency will restrict our design techniques, low OSR is more suitable for the bandwidth of 10 MHz structure. In order to achieve better resolution and reduce quantization noise, at least a third-order noise-transfer function is indispensable. **Figure 1** shows the proposed CT ΔΣ modulator architecture which consists of a 4-bit internal quantizer, operating at 160 MHz with an OSR of 8, and a third-order single-loop filter. In order to decrease power consumption and maintain a good alias filter characteristic, a combination of feedforward and feedback stabilized loop filters [9] is adopted. The 4-bit quantizer, including the NRZ feedback DAC is connected to the output of the loop filter. The quantizer delay is set to half of the sampling period. This large delay is compensated exactly by an additional feedback path $K_{3fb}$.
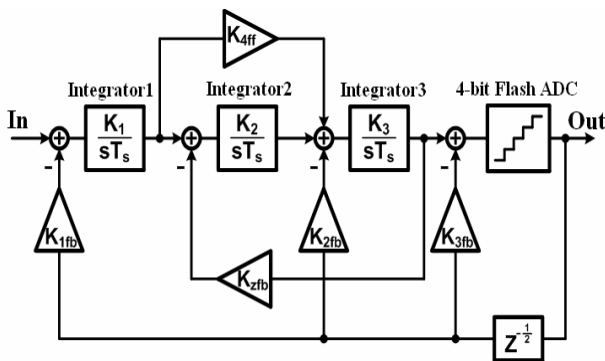


**Figure 1. Continuous-time ΣΔ modulator architecture.**

A possible design technique for CT modulators is described [10,11]. Specifying a DT modulator and trying to find the equivalent CT modulator between s-plane and z-plane can use the impulse-invariance transform expressed as:

$$Z^{-1}\{H(z)\} = L^{-1}\{R_D(s)H(s)\}\Big|_{t=n \cdot T_s} \quad (1)$$

where $R_D(s)$ is the Laplace transform of impulse response of the DAC and $H(z)$ is the DT loop filter. Equation (1) is adopted to compensate the impairments of the circuit such that the resulting CT domain modulator still matches with the specified DT modulator. The followings outline the procedure used to determine the direct feedback coefficients such that quantizer delay is canceled exactly. First, a noise-transfer function (NTF) in the z-domain is chosen, then the loop transfer function $H_{loopz}(z)$ is derived as follows:

$$H_{Loopz}(z) = \frac{1 - NTF(z)}{NTF(z)}. \quad (2)$$

Using the discrete-to-discrete (d2d) function in the MATLAB control system toolbox can easily transform $z$ into $z^{1/2}$ shown in (3):

$$H'_{LoopZ}\left(z^{\frac{1}{2}}\right) = \frac{b'_{n-1}z^{\frac{n-1}{2}} + \cdots + b'_1 z^{\frac{1}{2}} + b'_0}{z^{\frac{n}{2}} + a'_{n-1}z^{\frac{n-1}{2}} + \cdots + a'_1 z^{\frac{1}{2}} + a'_0}. \quad (3)$$

After multiplying $z^{1/2}$ in the formula, a constant term $b'_{n-1}$ can be easily separated from the transfer function $L_{filterD}\left(z^{1/2}\right)$ of the loop filter as follows:

$$L_{filterD}\left(z^{\frac{1}{2}}\right) = \frac{b'_{n-1}z^{\frac{n-1}{2}} + \cdots + b'_1 z^{\frac{1}{2}} + b'_0}{z^{\frac{n}{2}} + a'_{n-1}z^{\frac{n-1}{2}} + \cdots + a'_1 z^{\frac{1}{2}} + a'_0} \cdot z^{\frac{1}{2}} \quad (4)$$

Using the discrete-to-continuous (d2c) function in the MATLAB tool box converts this transfer function $L_{filterD}\left(z^{1/2}\right)$ to continuous time. A possible loop filter is then defined in the CT domain is RC loop filter.

## 3. Continus-Time ΣΔ Modulator Implementation

### 3.1. Continuous-Time ΣΔ Modulator Circuit

The 4-bit CT ΣΔ modulator circuit including the excess loop delay compensation is shown in **Figure 2** [12]. The modulator consists of a 4-bit internal quantizer, operating at 160 MHz with an OSR of 8, and a third-order single-loop filter. The loop filter is realized as an active RC filter. Due to the low supply voltage and the high-linearity requirement two-stage op amps with CT common mode feedback (CMFB) are used. The 4-bit quantizer is connected to the DWA circuit followed by the feedback

DAC. When multi-bit quantizer is used for better quantization resolution, in-band tones are often observed due to the element mismatch in the feedback DAC. To solve the mismatch problem, dynamic element matching is used in the circuit design. The RC time constant in the circuit dominating the entire NTF pole function, will keep stable and therefore the circuit phase margin will also be stable. Due to the process variation, the capacitor tuning circuit is used in this modulator. The DAC1 and DAC2 circuits provide the first and second feedback paths $K_{1fb}$ and $K_{2fb}$, respectively. The third $K_{3fb}$ is the feedback path around the 4-bit quantizer and its output is connected to the DAC2 output. In order to reduce the loop filter capacitive loading effects, all the comparators inside flash ADC input transistors must be the minimum-size.

General "zero-order" feedback path requires additional summing amplifier and return-to-zero (RZ) DAC contains additional logic control circuits. However, this will cause additional loop delay, increase power consumption and complicate the circuit. Therefore, to improve these drawbacks, in this work, a feedback path is directly connected to the last integrator input, and then the additional summing amplifier is eliminated. Obviously this way reduces power consumption and excess loop delay.

## 3.2. Loop Filter

There are three types of commonly used CT integrators: active-RC integrators, Gm-C integrators and MOSFET-C integrators. In this design, an active-RC integrator is chosen for the three stages of the third-order loop filter because it has high linearity and easy interface with DACs compared to Gm-C integrators. If active-RC integrators were used, resistive loading increases the power requirements due to the need for buffer stages. A higher frequency range is additionally demanded in connection with a high linearity, the active-RC filters are the preferred structure. The third-order noise shaping loop filter is realized by an active-RC op amp circuit as shown in **Figure 2**. The advantages of this implementation are high linearity and high output signal swing, and it also provides a good virtual ground for the modulator feedback DACs. This eases design, especially with low supply voltages. **Figure 3** show the architectures of the 1.2-V fully differential op amp [13] and the corresponding CMFB circuit is shown in **Figure 4**. The op amp shown in **Figure 3** is a two-stage that consists of a folded cascode input stage, a common source output stage and a CT CMFB which is similar to a transimpedence amplifier.
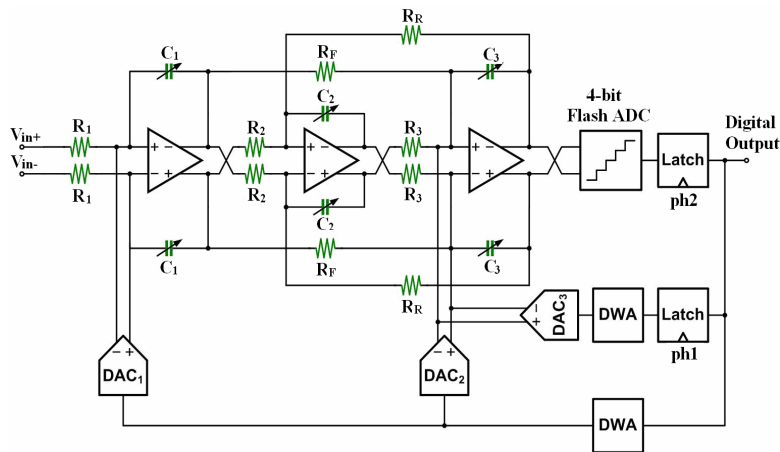


**Figure 2. Four-bit CT ΣΔ modulator architecture.**
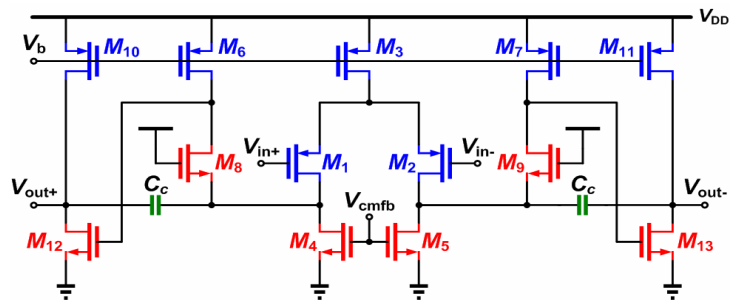


**Figure 3. Fully differential 1.2-V op amp circuit.**

As shown in **Figure 4**, two resistors with values equal to $2R_1$ are used to sense the output common mode voltage and produce a current $I_1$. This current is compared with $I_2$, which is set by the desired common-mode voltage ($V_{DD}/2$) and the resistor $R_1$. The difference between $I_1$ and $I_2$ is then converted into a control voltage labeled as $V_{cmfb}$ by transistors M$_3$, M$_6$ and M$_9$. The control voltage will then be used to adjust the V$_{GS}$'s of M$_4$ and M$_5$, such that the output common-mode voltage is stabilized to about $V_{DD}/2$. The CMFB circuit has advantages of allowing rail-to-rail output swing. Furthermore, it does not need any level shift or attenuation on the common mode signal, unlike other CT CMFB circuits that use differential pairs.

## 3.3. Four-Bit Flash ADC

In ΣΔ modulators, the main specifications for the quantizer are offset, speed, area and power consumption requirements. Moreover the quantizer has to operate at the speed required by the oversampling process. Therefore it must be implemented as a flash ADC [14]. The block diagram of the 4-bit flash ADC used in the quantizer is shown in **Figure 5**. It consists of 15 differential comparators, a resistor ladder, and a thermal to binary encoder. These comparators compare the input signal with reference voltages by a resistor ladder biased by the full scale reference. Consequently, the comparator outputs constitute a thermometer code, which is converted to binary by the encoder. Since flash architectures employ comparators, they are susceptible to metastability errors. In order to lower the probability of metastable states, the thermometer-binary decoding can be pipelined so that potentially indeterminate outputs are allowed more regeneration time [15].

The clocked comparator is composed of a preamplifier and a regenerative latch. The schematic is shown in **Figure 6**. The comparator utilizes the advantages of the low

kickback noise in static comparators and the high regeneration speed in dynamic comparators. On one hand, keeping the preamplifier continuously biased throughout the conversion period significantly reduces the kickback disturbance; on the other hand, the dynamic flip-flop in the latch circuit will shorten the regeneration and reset time [16].
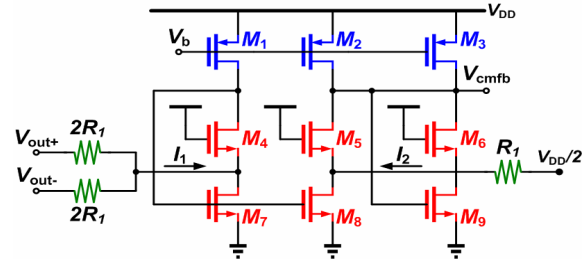


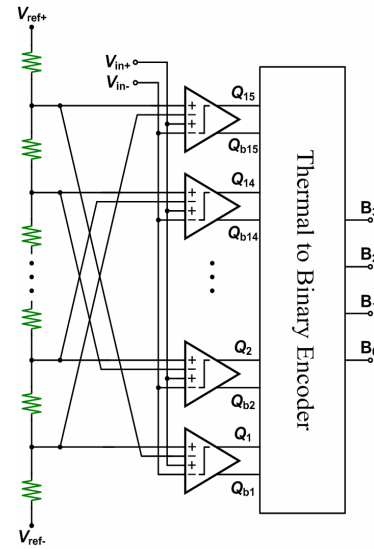**Figure 4. Continuous-time CMFB circuit.**



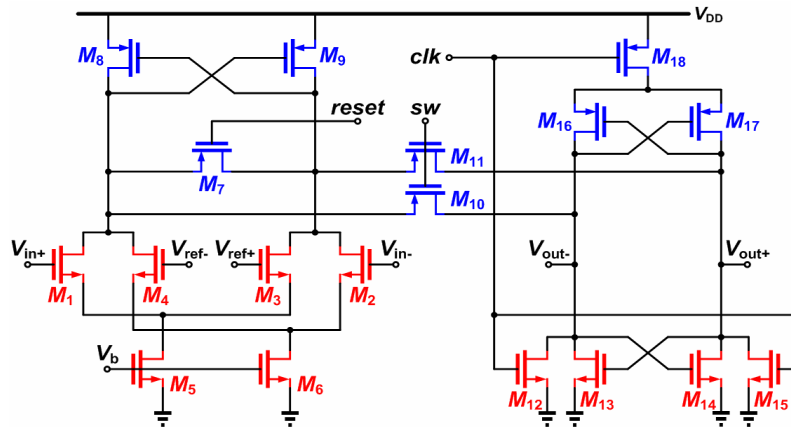**Figure 5. Four-bit quantizer and encoder structure.**



**Figure 6. Schematic of the comparator circuit.**

### 3.4. Feedback DACs

As shown in **Figure 7**, a multi-bit current-steering DAC, feeds current to the virtual grounds of the active-RC integrators, therefore good DAC linearity can be achieved. The improved DAC linearity is another advantage of active-RC integrators when compared to Gm-C integrators [17].

The CMFB circuit for the DAC along with the differential pairs connects to the op amp input. This DAC feedback circuit requires a 0.6-V voltage as a reference voltage, and this may operate in the virtual ground voltage. The reference voltage is connected by an external power supply. Two current sources inject common-mode currents to prevent a common-mode offset from appearing at the amplifier virtual grounds. The dynamic performance of current-steering DAC's is limited by the feedthrough of the control signals to the output lines. The coupling of the switching control signals to the output lines through the parasitic gate-drain capacitance of the switching transistors is also a source of glitches. The lower part of **Figure 7** is the simplified representation of the current-steering DAC. In this work, to minimize the feedthrough to the output lines, the drain of the switching transistors is isolated from the output lines by adding two cascaded transistors [18].

### 3.5. DWA Circuit

Combining ΣΔ modulators with multi-bit quantization is an effective means to achieve a high dynamic range and a wide bandwidth. The major obstacle in designing multi-bit ΣΔ modulators is that good component matching is required for internal DAC linearity. Good attenuation of DAC noise due to component mismatches can be provided by the DWA algorithm, which ideally can achieve a first-order DAC noise shaping. For DWA to be more useful in multi-bit SDM's, the DAC baseband tones must be removed. Conventionally, the problem is circumvented by adding dither. However, adding dither contributes additional noise to the base-band, degrades SNR and possibly destabilizes the modulator. A low- complexity high-speed circuit is proposed for the implementation of a DWA technique without adding dither, used for reducing DAC noise due to component mismatches [19].

The block diagram of the DWA logic is shown in **Figure 8**. The input of the DWA logic is connected to the four-bit quantizer output. The DWA logic converts the quantizer output code to the control signals, $S_i$, i = 0, 1,···, 15, for the element selection of 4-bit DAC. A 4-bit adder and a 4-bit register produce two indexes which are converted to two sets of 16-bit thermometer codes by two binary to thermometer decoders. When the carry signal of the adder is low, the output control signals are the mutual XOR of the two 16-bit thermometer codes. When the carry signal is high, the control signals are the mutual XNOR of the two 16-bit codes. The DWA algorithm selects DAC components cyclically one by one. No unit is reselected before all the others are selected.

### 3.6. Time Constant Tuning Circuit

CMOS technologies usually do not have tight control over absolute values of $R$ and $C$, so an automatic $RC$ time constant tuning circuit is needed to ensure the ΣΔ modulator stability and SNR performance over large $RC$ time constant variations. Therefore, a discrete capacitor tuning scheme is employed to calibrate the time constant of the active-$RC$ integrators. The adjustable capacitor array is shown in **Figure 9**.
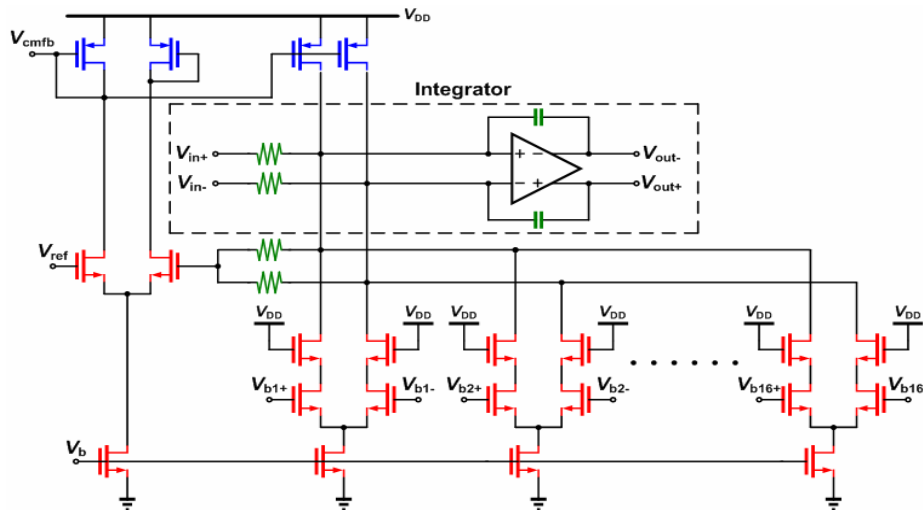


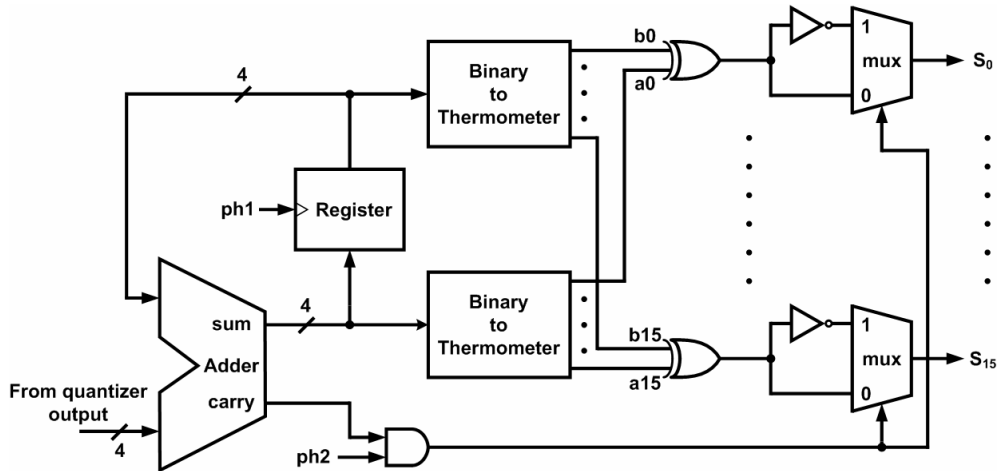**Figure 7. A multi-bit current-steering DAC schematic.**

**Figure 8. The block diagram for the DWA realization.**
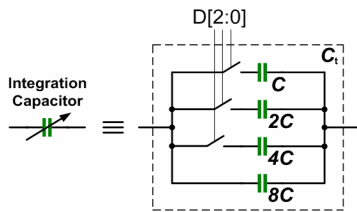


**Figure 9. Tunable capacitor array.**

The capacitors in the arrays are binary-weighted except the "always-in-use" capacitor which is equal to the most significant bit (MSB) capacitor, 8C. This sizing method provides constant tuning steps with the least number of capacitors. The 3-bit digital control codes are fed externally to choose which capacitors to use.

## 4. Measurement Results

The proposed third-order multi-bit CT $\Sigma\Delta$ modulator in this paper is implemented in TSMC 0.18-μm CMOS process. Post-processing was performed using MATLAB before tapout. The modulator samples signals at 160 MHz with 10 MHz signal bandwidth and oversampling ratio of 8 and operates with a 1.2 V supply voltage. The total power consumption is 19.8 mW. **Figure 10** shows the modulator die microphotograph including the wire bounding pads. The CT $\Sigma\Delta$ modulator is essentially a mixed-signal system which includes integrator, quantizer, and digital circuits. To achieve high resolution and linearity, caution should be taken in the layout design to reduce the effects of mismatch, parasitic and digital noise coupling to analog blocks. The total chip area including bonding pads is $0.9 \times 1.284$ mm$^2$.

The DWA circuit is located on the left of the chip. The noisy clock generator is placed in the bottom right-hand side to prevent interference with the weakly sensitive
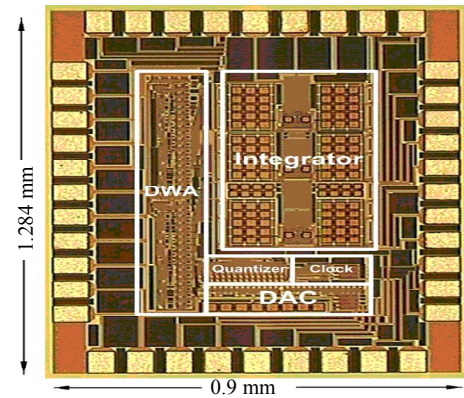


**Figure 10. Microphotograph of the CT $\Sigma\Delta$ modulator.**

analog blocks. A single-to-differential circuit converts the single-ended input signal to a balanced differential signal input to the ADC. The output data stream of the modulator was captured using a logic analyzer. **Figure 11** shows the digital outputs of the CT $\Sigma\Delta$ modulator measured by the logic analyzer for an input sinusoid at 3 MHz. The output spectrum density of the CT $\Sigma\Delta$ modulator analyzed by logic analyzer for an input sinusoidal signal of 3 MHz is shown in **Figure 12**. A peak SNDR of 48 dB which corresponds to a 7.7-bit within a bandwidth of 10 MHz is measured. The measured SNR and SNDR versus input signal level of the CT $\Sigma\Delta$ modulator for an input sinusoid at 3 MHz are plotted in **Figure 13**. The measured input peak dynamic range is 54 dB. **Figure 14** summarizes the measured SNR and SNDR for varying input frequencies. The SNR and SNDR fall to 46 dB and 43 dB respectively for a 9 MHz input signal. Because the integrator is basically a low pass filter, the modulator acts as low-pass filtering characteristic. When input frequency is increased, the SNR/SNDR values will be decreased.
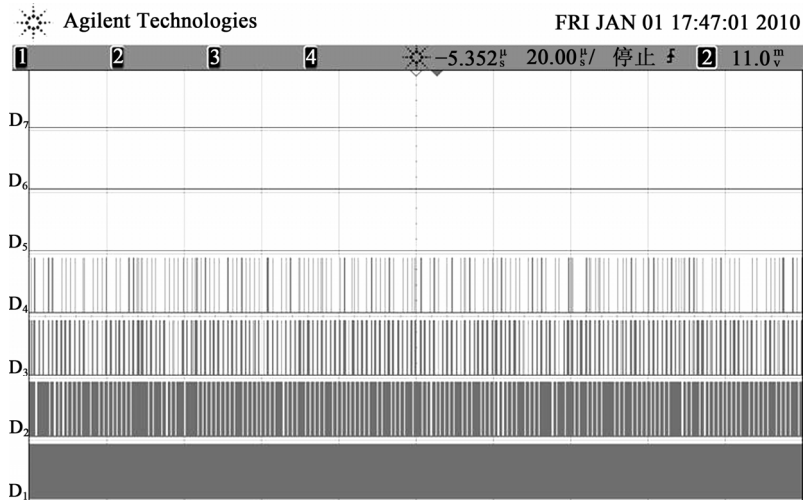
*CS*

**Figure 11. Measured digital output of the CT ΣΔ modulator at *f* = 3 MHz.**
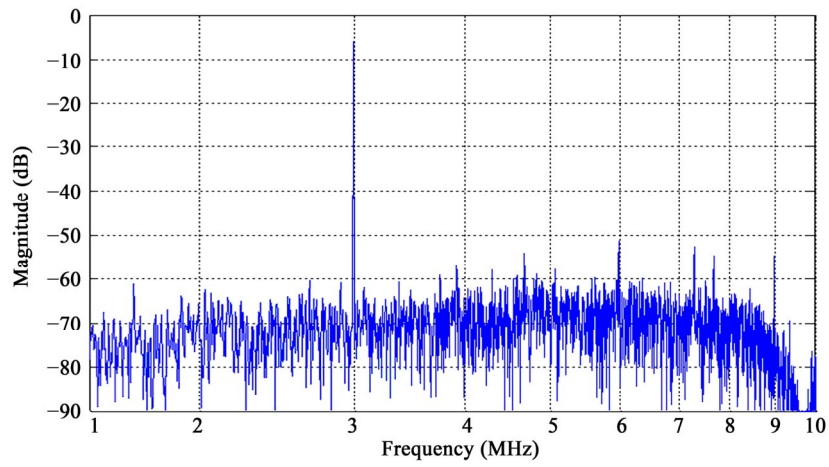


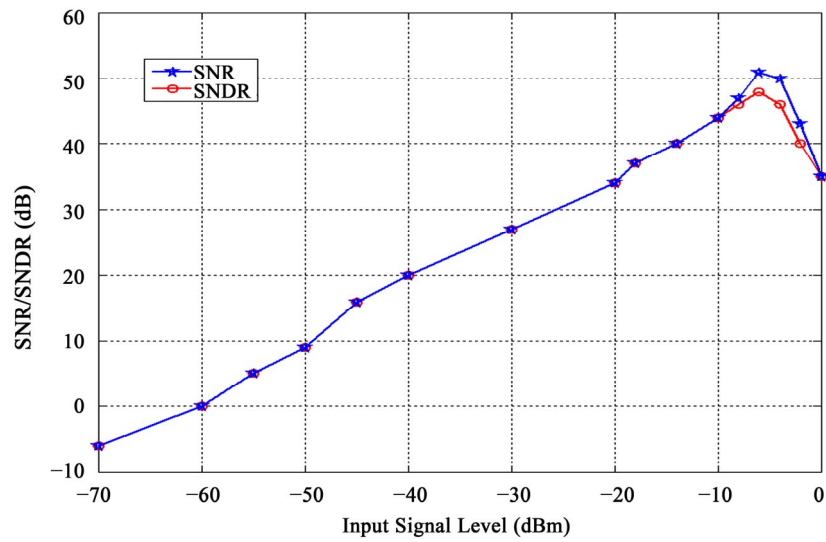**Figure 12. Measured output spectrum density.**



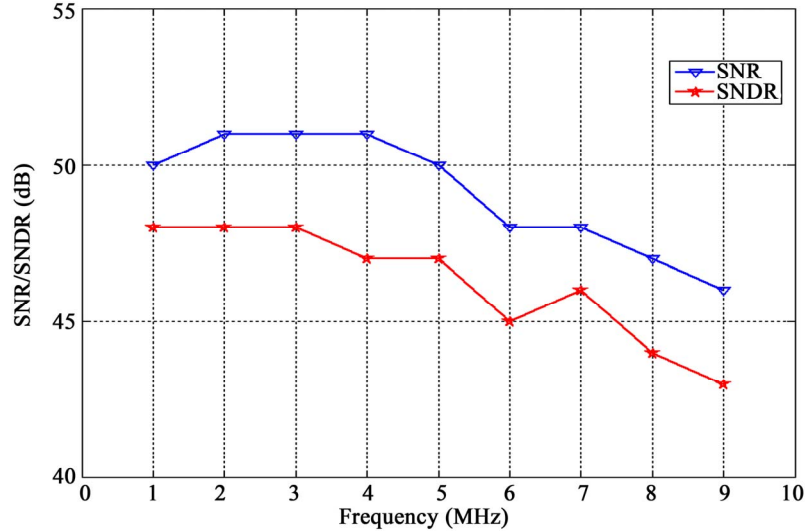**Figure 13. Measured SNR and SNDR vs. input signal level.**

**Figure 14. Measured SNR and SNDR vs. input frequency.**

The performance parameters of this chip are summarized in **Table 1**. In this work, we use the design strategy for low-power CT ΣΔ modulator proposed by [20]. This concept is based on the figure of merit (FOM) which takes the overall power consumption, the dynamic range, and the signal bandwidth into account to find the most power-efficient ΣΔ modulator implementation with respect to these design parameters.

The FOM used is defined as

$$FOM = \frac{P}{2^B \cdot 2f_B}, \qquad (5)$$

where $P$(mW) represents the power consumption, $B$ is number of bits and $f_B$(MHz) is the bandwidth. The performance comparisons with other literatures are shown in **Table 2**. The smaller the FOM value is, the better the overall performance is. From this comparison table, it is confirmed that the proposed modulator with low voltage operations can achieve a wide bandwidth and lower power consumption.

**Table 1. The performance summary of the CT ΣΔ modulator.**

| Parameters | Measured results |
|---|---|
| Sampling Frequency | 160 MHz |
| Signal Bandwidth | 10 MHz |
| SNR | 51 dB |
| SNDR | 48 dB |
| ENOB | 7.7 bits |
| Dynamic Range | 54 dB |
| Power Supply | 1.2 V |
| Power Dissipation | 19.8 mW |
| Chip Area | 1.156 mm$^2$ |
| Process | TSMC 0.18 um CMOS |

**Table 2. Performance comparisons with other literatures.**

| Parameter | This work | [21] | [22] | [23] | [24] |
|---|---|---|---|---|---|
| Technology | 0.18 um | 0.18 um | 0.18 um | 90 um | 0.13 um |
| Voltage (V) | 1.2 | 1.8 | 1.2 | 1.2 | 2.5 |
| BW (MHz) | 10 | 10 | 7.5 | 1.92 | 100 |
| SNR (dB) | 51 | 63 | 71 | 66.4 | 58.9 |
| SNDR (dB) | 48 | 56 | 67 | 62.4 | 53.1 |
| ENOB (Bits) | 7.7 | 9 | 10.8 | 10.1 | 8.5 |
| Power (mW) | 19.8 | 122.4 | 89 | 12.5 | 350 |
| FOM (pJ/Conv.) | 4.76 | 11.95 | 3.33 | 2.97 | 4.83 |

## 5. Conclusions

A low-voltage, low-power and wide bandwidth CT ΣΔ modulator has been implemented in a TSMC 0.18-um technology. The low-complexity high-speed implementation of the DWA technique for the reduction of baseband tones is used in this modulator. The excess loop delay set to half the sampling period of the quantizer has been used to avoid degradation of modulator stability in this architecture. All integration capacitors are tunable to overcome time constant variation. In addition, CT ΣΔ modulator provides a significant amount of inherent anti-aliasing, which is especially important when OSR is minimized in order to maximize the input bandwidth. The CT ΣΔ modulator itself occupies just 1.16 mm$^2$ and consumes 19.8 mW. The modulator achieves a SNR of 51 dB and SNDR of 48 dB over 10 MHz signal bandwidth**.**

## 6. Acknowledgements

## 7. References

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the chip fabrication and technical supports with the number of T18-98D-158.