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ΔI_{DDQ} Testing of a CMOS Digital-to-Analog Converter Considering Process Variation Effects*

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Abstract

In this paper, we present the implementation of a built-in current sensor (BICS) which takes into account the increased background current of defect-free circuits and the effects of process variation on ΔI_{DDQ} testing of CMOS data converters. A 12-bit digital-to-analog converter (DAC) is designed as the circuit under test (CUT). The BICS uses frequency as the output for fault detection in CUT. A fault is detected if it causes the output frequency to deviate more than ±10% from the reference frequency. The output frequencies of the BICS for various (MOSIS) model parameters are simulated to check for the effect of process variation on the frequency deviation. A set of eight faults simulating manufacturing defects in CMOS data converters are injected using fault-injection transistors and tested successfully.

Keywords: I_{DDQ} Testing, DAC, BICS, Sub-Micron CMOS IC, ΔI_{DDQ} Testing, Process Variation, Background Current

1. Introduction

Quiescent current (I_{DDQ}) testing has become an effective and efficient testing method for detecting physical defects such as gate-oxide shorts, floating gates (open) and bridging faults [1] in circuits. Conventional I_{DDQ} testing is based on the fact that quiescent current in a defect free circuit is less compared to the quiescent current of the circuit with defects. Several available I_{DDQ} test methodologies can be classified into two groups, external (off-chip) and internal (on-chip) I_{DDQ} testing. External I_{DDQ} testing monitors power supply current through the power pins of the integrated circuit package while internal I_{DDQ} testing monitors power supply current through the built-in current sensors (BICS) [2]. On-chip built-in current sensors are advantageous over off-chip current sensors for detecting the defective quiescent current due to better discrimination and higher testing speeds [3].

Currently, in VLSI circuits designed in sub-micron/deep sub-micron CMOS processes, the gap between the defective and defect-free quiescent current is narrowing due to increasing background current [4-6]. Process variation also impacts digital, analog/mixed-signal integrated circuits fabricated in sub-micron/deep sub-micron CMOS technology. Process variation affects the threshold voltage of the circuit and thus the effective leakage current in the circuit. Hence, designing BICS for submicron CMOS process is becoming difficult. However, problems related with I_{DDQ} testing in digital VLSI circuits designed in submicron CMOS processes are well known and have been researched extensively [7]. Many new testing techniques have been proposed and presented in literature to minimize the effect of increased background current and the impact of process variation on the I_{DDQ} measurements to improve defect detectability. Among those, delta I_{DDQ} (ΔI_{DDQ}) testing is particularly attractive because the differential measurement suppresses the impact of the background current. Vazquez and de Gyvez [8,9] have reported a ΔI_{DDQ} BICS which has both on-chip and off-chip components. Most of these new testing techniques to improve the effectiveness of I_{DDQ} testing have been successfully implemented for digital circuits. However testing of analog circuits using I_{DDQ} in submicron CMOS is still a problem due to variation in design parameters from one specific application to other. Hence, in testing of analog circuits the tolerance on the circuit parameters has to be taken into account because it can cause a significant difference between the quiescent

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current of a manufactured circuit and its nominal value. A simple pass/fail test is not a good measure for fault detection. Mixed-signal types of circuits such as data converters are even more difficult to test using I_{DDQ}. We have extensively researched and presented the ΔI_{DDQ} testing for sub-micron CMOS mixed-signal circuits in our previous work [10,11]. In this work, effects of process variation on ΔI_{DDQ} testing for CMOS data converters are studied and presented.

Here we present the design and implementation of a built-in-current sensor for delta I_{DDQ} testing in a 0.5 µm n-well CMOS process for a 12-bit digital-to-analog converter (DAC) to study the effects of process variation. The paper is organized as follows: Section 2 describes the proposed sensor and its circuit implementation, Section 3 describes 12-bit DAC which is being used as the circuit under test (CUT), Section 4 presents the results and discussion and Section 5 gives the conclusion.

2. Built-in Current Sensor for Delta I_{DDQ} Testing

2.1. Proposed Design

The proposed sensor combines the concepts of multi-parameter testing and delta I_{DDQ} testing to detect defective currents and is based on Keating-Meyer approach for I_{DDQ} testing [12] and is a modification of I_{DDQ} measurement (MEAS) block of delta I_{DDQ} BICS by Vazquez and de Gyvez [8,9]. Multi-parameter testing helps in suppressing the high background current while delta I_{DDQ} testing helps in decreasing I_{DDQ} variance. **Figure 1** [8,9] summarizes the sensor's operation; it has two curves corresponding to low and high leakage. After applying an input pattern to the CUT, the on-chip capacitor is allowed to charge and discharge until it reaches the reference voltage V_{REF}.

The expression associated with this discharge is given by [8-11]

$$I_{DDQ} = C\frac{\Delta V}{\Delta t} \quad (1)$$

where $\Delta V = V_{DD} - V_{REF}$ and C is the total circuit capacitance including the discharging capacitor. The time Δt taken by the decaying voltage of the capacitor to reach V_{REF} is measured as frequency by using a comparator and a voltage controlled oscillator (VCO) as shown in **Figure 2**. The comparator gives an output V_{CTRL}, which is used as an input by the VCO to give the output frequency.

In the design, the BICS is on-chip for better testability and higher testing speeds. The proposed sensor also takes into account the process variation after fabrication and self-adjusts for fault detection. This is done by calculating the output frequency of the VCO and subtracting it from the output frequency of the ring oscillator to obtain the final output frequency.

2.2. Circuit Implementation

Figure 2 shows the circuit diagram of the BICS where p-MOSFET in earlier MEAS block [8,9] has been replaced by two transmission gates TG_1 and TG_2 as switches. The two transmission gates are used to isolate CUT from the BICS depending on the mode of operation (normal mode or test mode). In the normal mode of operation, the supply voltage V_{DD1} is given to CUT and the BICS is isolated, so that there will be no performance degradation in the CUT.

In the test mode of operation, the supply voltage is given to V_{DD}. In this mode, initially transmission gate TG_1 between the supply voltage and the CUT is turned on charging the capacitor to V_{DD}, transmission gate TG_2 between the BICS and the CUT is turned off isolating them during this period. A single clock has been used to turn on and off both TG_1 and TG_2 as shown in **Figure 2**. For fault detection TG_1 is turned off and TG_2 is turned on discharging the capacitor C_1 through the CUT. When TG_2 is turned on, the node X of the capacitor C_1 gets connected to the comparator and the voltage at the node X keeps reducing as the capacitor gets discharged through the CUT. The voltage at node X is compared to the reference voltage through the comparator to give a pulse output. The reference voltage to comparator is

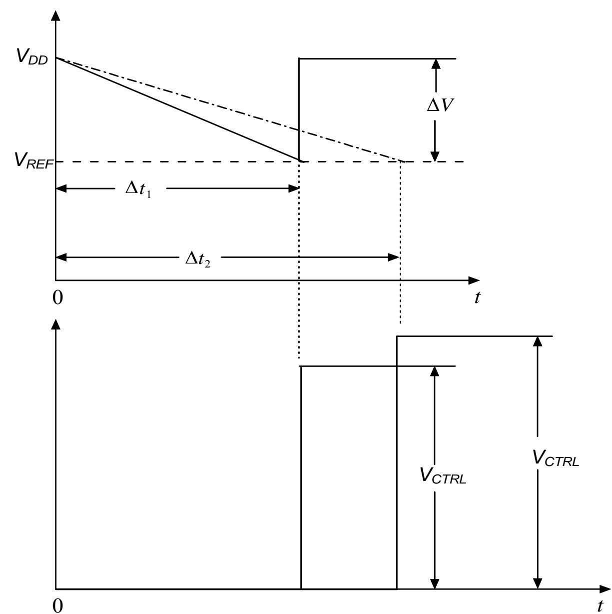

Figure 1. Capacitor discharge transient voltage of the CUT under high and low leakage [8-11]. Solid line: fault free condition, dotted line: faulty condition.

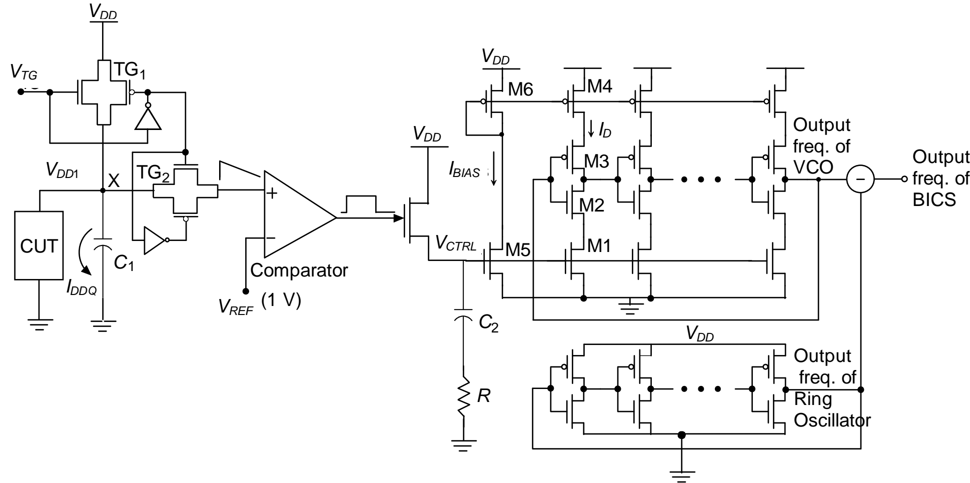

Figure 2. ΔI_{DDQ} built-in current sensor (BICS).

given externally so that the width of the pulse at the output of the comparator can be controlled. The output of the comparator is used as input to the NMOS switch which in turn charges the capacitor C_2 as shown in **Figure 2**.

The voltage across the capacitor C_2, V_{CTRL} depends on the time NMOS switch is on, which in-turn depends on the discharge time of the capacitor C_1. The voltage across the capacitor V_{CTRL} is then given to a VCO. The output of a VCO is a clock signal, whose frequency is dependent on V_{CTRL}. Its operation is similar to that of a ring oscillator. The oscillation frequency of the current starved VCO for n number (an odd number ≥ 3) of stages is given by

$$f_O = \frac{1}{n\left(t_r + t_f\right)} \approx \frac{I_D}{n \cdot \left(C_{out} + C_{in}\right) \cdot V_{DD}} \quad (2)$$

where, t_r and t_f are the rise time and the fall time, respectively, and n is the number of stages. V_{DD} is the power supply voltage. I_D is the biasing current. The biasing current can be adjusted by varying the control voltage, which in turn changes the oscillation frequency. The output frequency of the voltage controlled oscillator is subtracted from the frequencies of the ring oscillator to obtain BICS final output frequency as shown in **Figure 2**. This method helps to overcome the process variation in sub-micron CMOS technology.

3. 12-Bit DAC Design (CUT)

The 12-bit DAC design uses a charge scaling architecture and the block diagram is as shown in **Figure 3** [13]. The DAC converts a 12-bit digital input word to a respective analog signal by scaling a voltage reference. The DAC consists of voltage reference, binary switches, scaling network, an operational amplifier and a sample and hold circuit. The multiplexer circuit connected to the other end of each capacitor, selects the voltage which is either V_{REF} or GND to which the capacitor is charged depending upon the control signal "V_S". Initially, the control signal for all multiplexer switches is set to LOW before giving any specified input so that GND is supplied to the capacitor network and reset. Then the capacitor network is supplied with the digital word by switching the particular multiplexer switch for each bit to the desired value of either V_{REF} for "1" or GND for "0". The capacitors whose ends are connected to V_{REF} are charged to +2 V and those, which are connected to GND, are charged to 0 V. Since the capacitor network is connected in parallel, the equivalent voltage is calculated by,

$$V_{OUT} = \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + B_N 2^{-N}\right) V_{REF} \quad (3)$$

The capacitor at the end of the network is used as a "terminating capacitor". Depending on the capacitors, which are charged to different voltages based on the input digital word, the effective resultant analog voltage is calculated for the respective digital combination. The analog voltage is passed through the op-amp and the sample-and-hold circuit and appears as an analog voltage. The op-amp and comparator used in DAC is designed for 2.5 V operation.

4. Results and Discussion

Figure 4 shows the chip layout of a 12-bit DAC designed for operation at 2.5 V in 0.5 μm n-well CMOS process with eight defects introduced using fault injection transistors (FITs) as switches [14]. The design integrates an on-chip BICS of **Figure 2** for ΔI_{DDQ} testing of physical defects such as shorts in MOSFETs. The DAC

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occupies 504 × 501 μm^2 area of the chip. The BICS occupies 20% (670 × 75 μm^2) of the total chip area.

In testing of analog and mixed signal circuits, the dependence of the power supply current on the circuit parameters has to be considered. This can result in a significant difference between the fabricated (manufactured) circuit and its nominal value. So a fault-free circuit can be considered as faulty and vice-versa [10,11,15]. This problem is overcome in the present work by considering a tolerance limit of ±10% on the fault free output frequency value. It thus takes into account the variations due to significant technology and design parameters. The circuit has been designed using the model parameters T69K [16] and the frequency output of the BICS is called the natural frequency (f_N). The BICS has been simulated with various model parameters to check for the effects of process variation on the deviation of the output frequencies from the natural frequency. The results are presented in **Figure 5**.

From **Figure 5**, it can be observed that the deviation of the output frequency of the BICS is less than ±10% for all the model parameters except T5CX [16], T51T [16], T3CU [16] thus falling within the tolerance limit. To check the robustness of the BICS against the process variation, the output frequencies obtained by BICS for the different model parameters have been modified by ± 10 % and their deviation with the natural frequency have also been calculated and shown in **Figure 5**. It can be observed from **Figure 5** that even with the variation of the output frequencies obtained by BICS by either +10% or –10%, the deviation is within ±10% of the natural frequency. Thus, the CUT can be designed using one set of model parameters and the same natural frequency value can be used for fault detection after fabrication using the BICS.

The CUT is then simulated after introducing faults using fault injection transistors one by one. **Table 1** summarizes the output frequency of the BICS along with their deviation from the natural frequency.

Fault-1 simulates a physical short between drain and source of one of the transistors in multiplexer part of the circuit of **Figure 3**, Fault-2 simulates a physical short between drain and source of one of the transistors in multiplexer part of the circuit of **Figure 3**, Fault-3 simulates a physical short between gate and source of one of the transistors of the op-amp part of the circuit of **Figure 3**, Fault-4 simulates a physical short between drain and source of one of the transistors of the op-amp part of the circuit of **Figure 3**. Fault-5 simulates a gate-substrate short in one of the transistors of the op-amp part of the circuit of **Figure 3**. Fault-6 simulates a gate-drain short of one of the transistors of the op-amp part of the circuit of **Figure 3**, Fault-7 simulates a source-substrate short of one of the transistors of the sample-and-hold circuit part of the circuit of **Figure 3** and Fault-8 simulates an inter-gate short between two transistors in the unit gain op-amp of the sample-and-hold circuit part of the circuit of **Figure 3**. From **Table 1** it can be noted that the deviation is greater than ±10% and thus detecting the introduced faults.

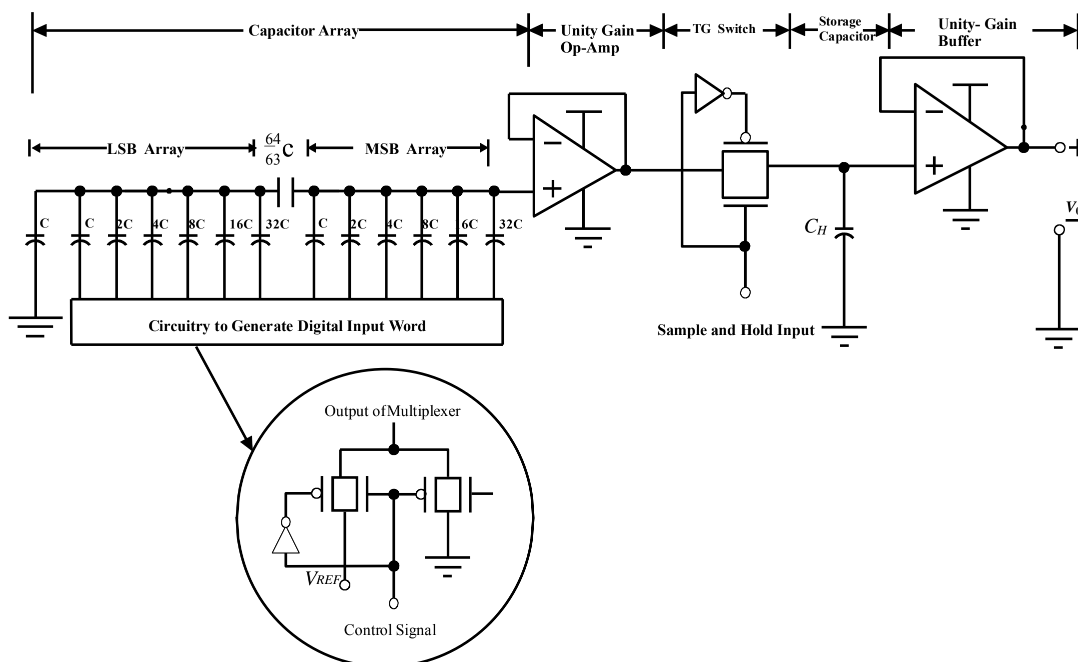

Figure 3. Schematic of a 12-bit charge scaling DAC.

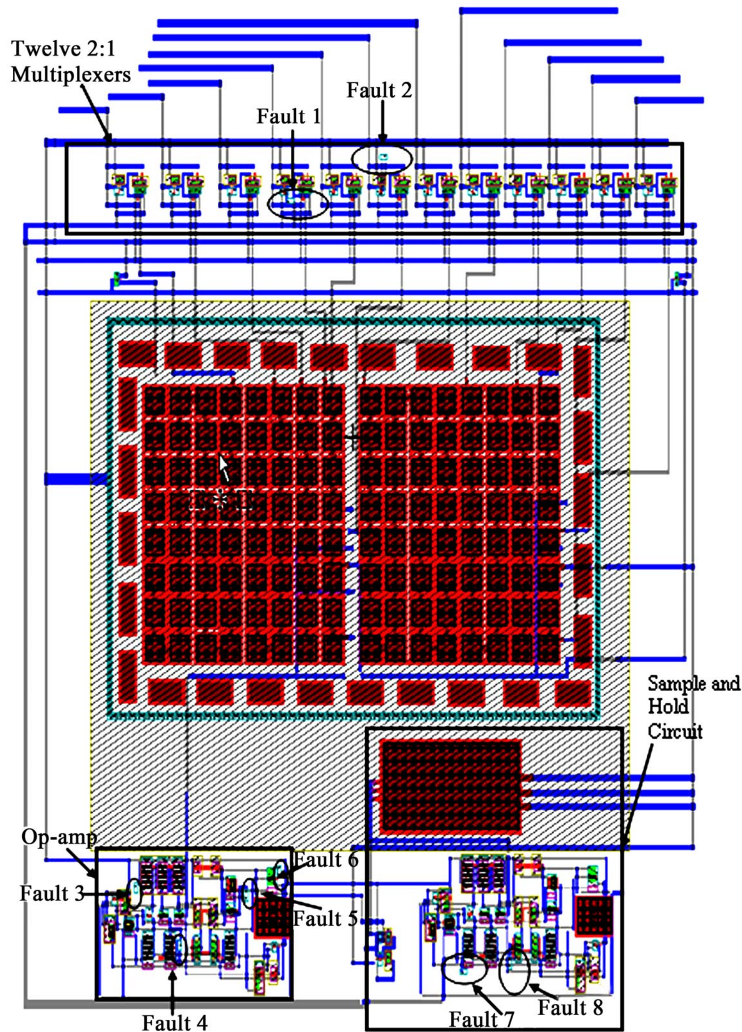

Figure 4. Chip layout of 12-bit DAC and BICS with induced faults.

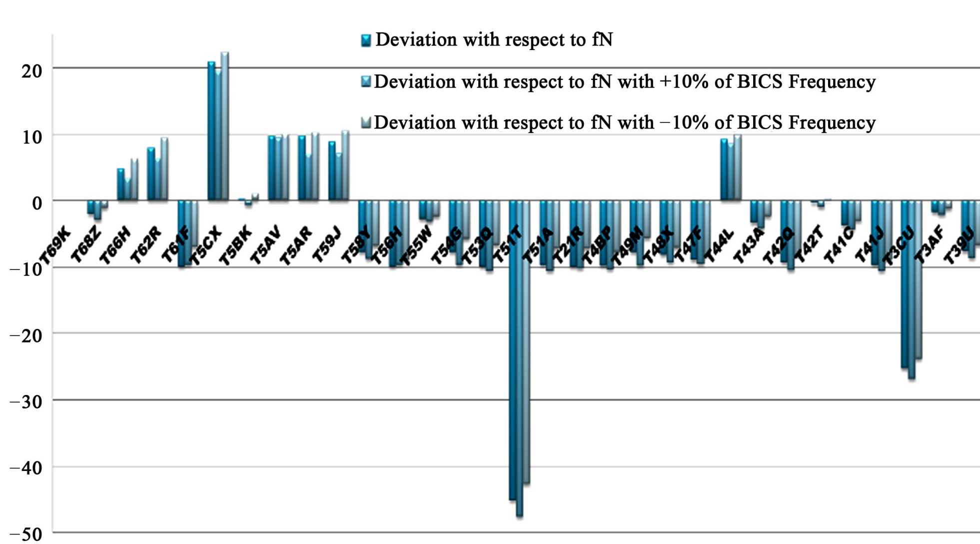

Figure 5. Deviation of BICS output frequency to natural frequency (f_N).

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Table 1. Deviation of BICS output frequency from natural frequency with induced faults.

Fault	Output Freq. of VCO (MHz)	Freq. of Ring Oscillator (MHz)	Output Freq. of the BICS (kHz)	Deviation (%)
No Fault	2.632	2.632	0	0
Fault 1	3.226	2.632	594.227	22.58
Fault 2	3.125	2.632	493.421	18.75
Fault 3	2.326	2.632	−305.998	−11.63
Fault 4	2.222	2.632	−409.357	−15.56
Fault 5	2.326	2.632	−305.998	−11.63
Fault 6	2.941	2.632	309.597	11.76
Fault 7	2.326	2.632	−305.998	−11.63
Fault 8	2.222	2.632	−409.357	−15.56

5. Conclusions

We have proposed and implemented a BICS for CMOS data converters fabricated in 0.5 µm n-well CMOS process. The circuits are designed to overcome the problem of increase in absolute value of quiescent current due to increasing background current. It also overcomes the variation in the value of quiescent current due to the change in threshold voltage and leakage current caused by process variation in the circuit. Thus, the increase in quiescent current caused due to defect can be estimated accurately in sub-micron CMOS data converters. The process variation effects on the ΔI_{DDQ} testing of the data converters are considered and simulated for various model parameters. The deviation of the output frequency of the BICS is observed to be less than ±10% for the model parameters and more than ±10% for various faults introduced in the data converter circuit using fault-injection transistors.

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